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NEC Electronics Inc.

μPB6100 (TTL-2) SERIES BIPOLAR TTL GATE ARRAYS

Revision 1 **March 1985**

Description

The μPB6100 series features three high-speed, low-power, TTL-compatible gate arrays using advanced bipolar technology. The μPB6101, μPB6102, and μPB6103 have 256, 598 and 918 internal cells, respectively. All devices are available in a variety of package types.

Gate arrays are intended for customers seeking cost effective alternatives. By using gate arrays, customers can reduce component count and board size so that they can be more competitive in the markets they serve. NEC's gate array program allows a customized IC to be developed quickly and at a small fraction of the cost of a full custom development program.

NEC's comprehensive CAD support system and master slice system significantly reduce the time and expense normally associated with semicustom devices. Normal turn-around time, after logic validation, is only 8 to 10 weeks. Advanced CAD tools such as logic simulation, automatic placement and routing, delay simulation, and test program generation ensure accurate error-free designs of all NEC gate arrays.

Features

- ☐ High speed — 2.5 ns/gate
- ☐ Low power — 1.4 mW/gate
- ☐ Quick turn-around time — 8 - 10 weeks
- ☐ Fully supported by advanced CAD
  - — Logic simulation
  - — Automatic placement and routing
  - — Test program generation
  - — Delay simulation
- ☐ Direct access to CAD simulation
  - — Customers can use the local network through their own terminal to an NEC design center for logic simulation
- ☐ Four types of output buffers available
  - — Totem-pole
  - — Open-collector
  - — Three-state
  - — Bidirectional
- ☐ Wide choice of DIP, flat, and PGA (pin-grid-array) packages to suit unique applications

Configuration Data

	μPB6101	μPB6102	μPB6103
Number of cells (Note 1)	256	598	918
Configuration	16 rows x 16 columns	26 rows x 23 columns	34 rows x 27 columns
Number of input buffers	42	64	64
Number of output buffers	30	52	64

Note: 1. A cell consists of two transistors and four resistors as shown in figure 2.

Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{CC}	+7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Output voltage, V_O	
Open-collector	−0.5 to +7.0 V
Except open-collector	−0.5 to +5.5 V
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated outside the Recommended Operating Conditions below. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value
Power supply voltage	V_{CC}	5.0 V ±0.5 V
Operating temperature	T_{OPT}	0 to +85°C
"H" level output current	I_{OH}	−1000 μA max
"L" level output current	I_{OL}	12 mA max

AC Characteristics

$V_{CC} = 5.0$ V: $T_A = +25°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Delay time, gate	t_{PHL}	1.3	1.9	2.7	ns	Fan-out = 3;
	t_{PLH}	1.9	2.7	3.8	ns	L = 3 mm
Delay time, input buffer	t_{PHL}	1.3	1.9	2.7	ns	Fan-out = 3;
	t_{PLH}	1.6	2.3	3.2	ns	L = 3 mm
Delay time, output buffer	t_{PHL}	3.3	4.7	6.6	ns	C_L = 15 pF;
	t_{PLH}	3.8	5.4	7.6	ns	R_L = 500 Ω

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DC Characteristics

T_A = 0 to +85 °C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input clamp voltage	V_{IC}	−1.5			V	V_{CC} = 4.5 V; I_{IL} = −18 mA
High-level output voltage (totem pole)	V_{OH}	2.5	3.4		V	V_{CC} = 4.5 V; I_{OH} = −1 mA
High-level output voltage (three-state)	V_{OH}	2.2	3.3		V	V_{CC} = 4.5 V; I_{OH} = −3.3 mA
Low-level output voltage	V_{OL}		0.3	0.5	V	V_{CC} = 4.5 V; I_{OL} = 12 mA
High-level input current	I_{IH}			20	μA	V_{CC} = 5.5 V; V_I = 2.7 V
High-level maximum input current	I_{IMAX}			100	μA	V_{CC} = 5.5 V; V_I = 7.0 V
Low-level input current	I_{IL}	−100			μA	V_{CC} = 5.5 V; V_I = 0.4 V
High-level input current (open collector)	I_{OH}			100	μA	V_{CC} = 4.5 V; V_O = 5.5 V
Short-circuit output current (except open collector)	I_{OS}	−100		−25	mA	V_{CC} = 5.5 V; V_O = 0 V
Off-state output current (three-state)	I_{OZ}	−20		20	μA	V_{CC} = 5.5 V; V_O = 0.4 V/2.7 V
Off-state output current (bidirectional)	I_{OZ}	−100		40	μA	V_{CC} = 5.5 V; V_O = 0.4 V/2.7 V
Input threshold voltage (hysteresis input)	V_{th+}	0.95	1.45	1.6	V	V_{CC} = 5.0 V
Input threshold voltage (hysteresis input)	V_{th-}	0.55	0.8	0.85	V	V_{CC} = 5.0 V
Hysteresis width	V_{th+} minus V_{th-}	0.4	0.65		V	V_{CC} = 5.0 V

Power Dissipation Data

Parameter	Block Type	Power Dissipation	Unit
Internal gate	F010	1.4	mW
Input buffer	M001	1.9	mW
Output buffer (totem-pole)	B001	2.4	mW
Output buffer (open-collector)	B002	2.4	mW
Output buffer (three-state)	B003	2.5	mW
Output buffer (bidirectional)	B004	4.4	mW
Output buffer (bidir, open-coll)	B007	4.4	mW

Chip Layout

The arrays are divided into three basic areas. The I/O buffers are placed uniformly on the periphery of each device so that there is an equal number on each die edge. At each signal pad location, the pin function can be one of several possible I/O configurations.

The area between the cells and the bonding pads contains all the peripheral circuitry needed to convert external I/O levels to internal logic levels. Power and ground distribution is also handled by the peripheral circuitry.

The center of the die contains rows of continuous gates separated by horizontal routing channels. The density of the array is a factor of the total cell count (row x column).

Figure 1. Chip Layout of Bipolar Gate Array

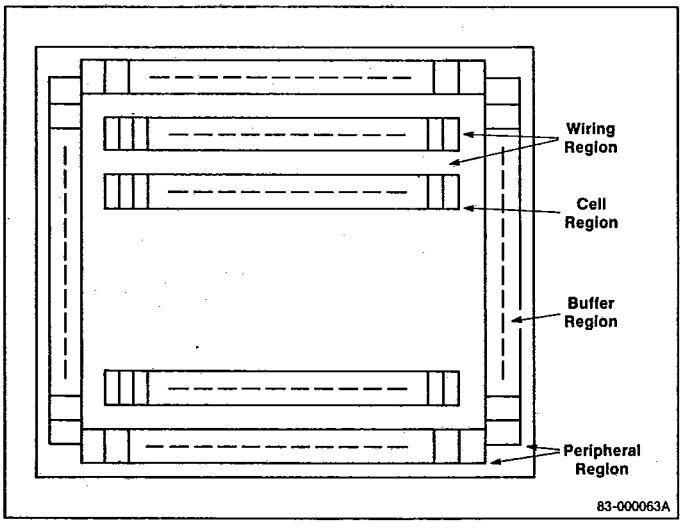

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Figure 2. Example of Gate Configuration (3-Input NAND Gate)

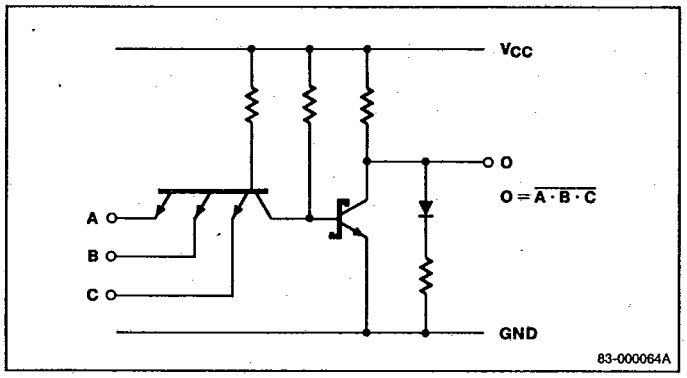


Figure 3. Output Loading Condition For Ordinary Output

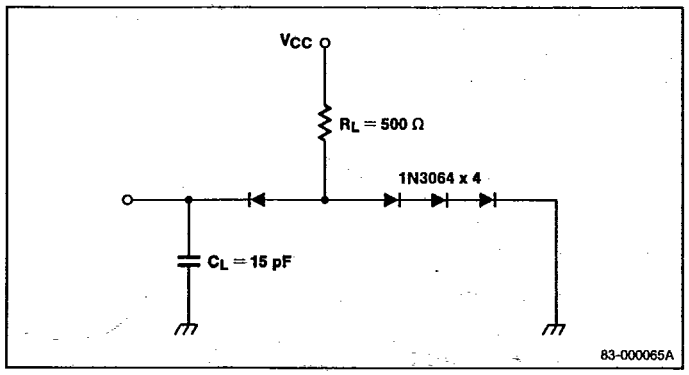
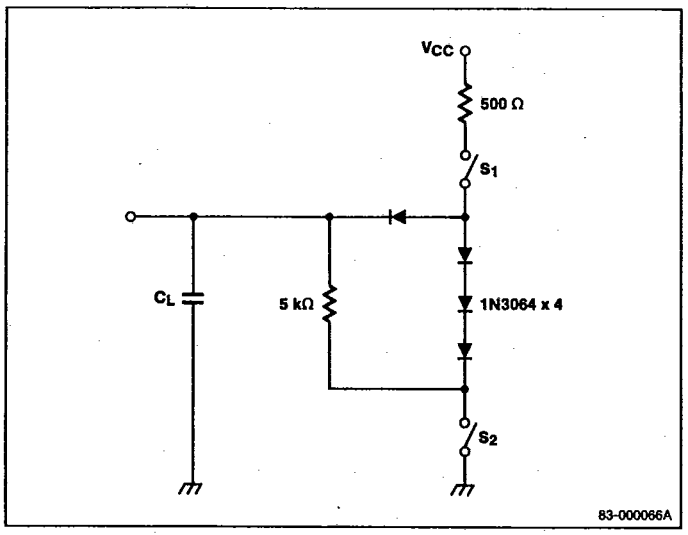


Figure 4. Output Loading Condition For Three-State Output



TTL-2 Block Library List

Block Type	Function	Cells	P_D (mW)
F004	Inverter	1	1.4
F000	2-Input NAND	1	1.4
F010	3-Input NAND	1	1.4
C020	6-Input NAND	2	1.4
C030	9-Input NAND	3	1.4
F011	3-Input AND	2	2.3
C021	6-Input AND	2	2.3
C51A	2-Wide 3-Input AND-OR Inverter	2	2.0
CA40	3-Wide 3-Input AND-OR Inverter	3	2.4
C054	4-Wide 3-Input AND-OR Inverter	4	2.8
F086	Exclusive OR	6	6.7
F074	D-Type Flip-Flop with $\overline{PR}$ and $\overline{CR}$	6	8.4
C109	J-$\overline{K}$ Flip-Flop with $\overline{PR}$	7	9.8
C075	D-Latch with $\overline{CR}$	4	5.0
CC10	Three-State Control	1	1.4
M001	Input Buffer	—	1.9
M010	Input Buffer (Schmitt Trigger)	—	1.9
B001	Output Buffer (Totem-pole)	—	2.4
B002	Output Buffer (Open-collector)	—	2.4
B003	Output Buffer (Three-state)	—	2.5
B004	Output Buffer (Bidirectional)	—	4.4
B007	Output Buffer (Bidirectional) (Open-collector)	—	4.4
V000	0-Level Generator	1	1.4
JWI	Wired AND	—	—
CD05	Delay Gate	4	3.7
CS10	Output Level Shift	1	2.5

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Figure 5. Example of a Logic Drawing

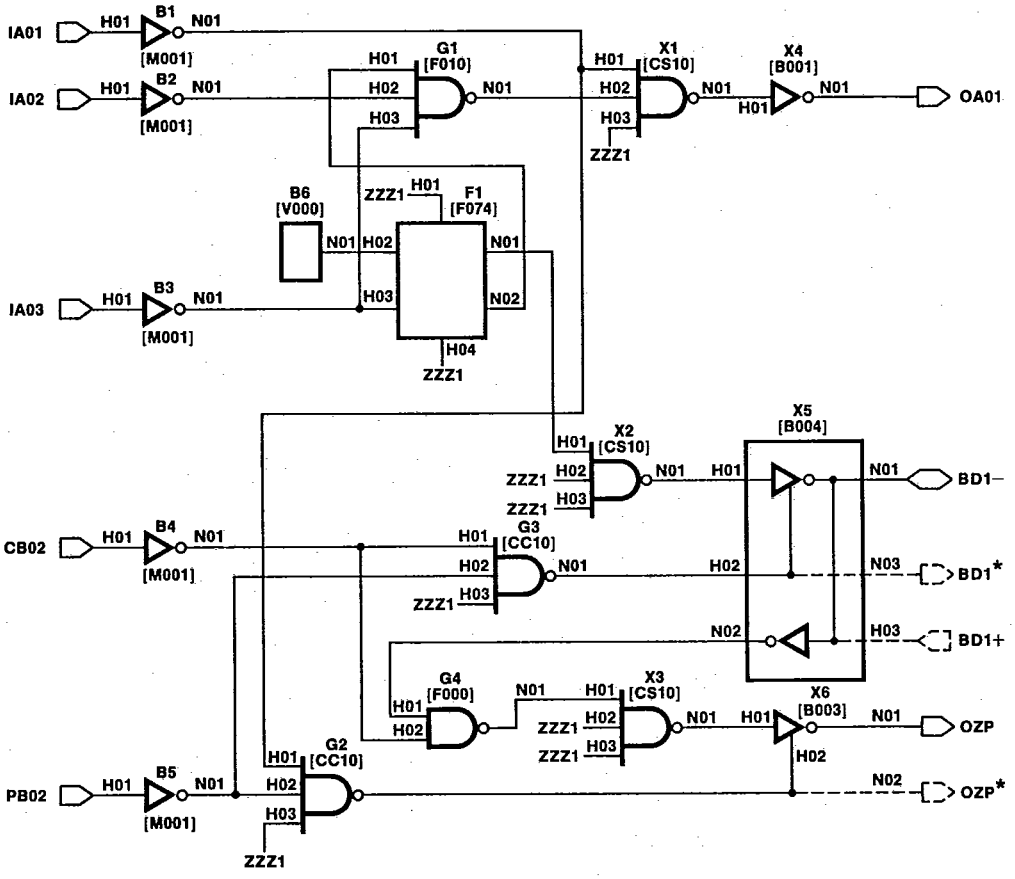
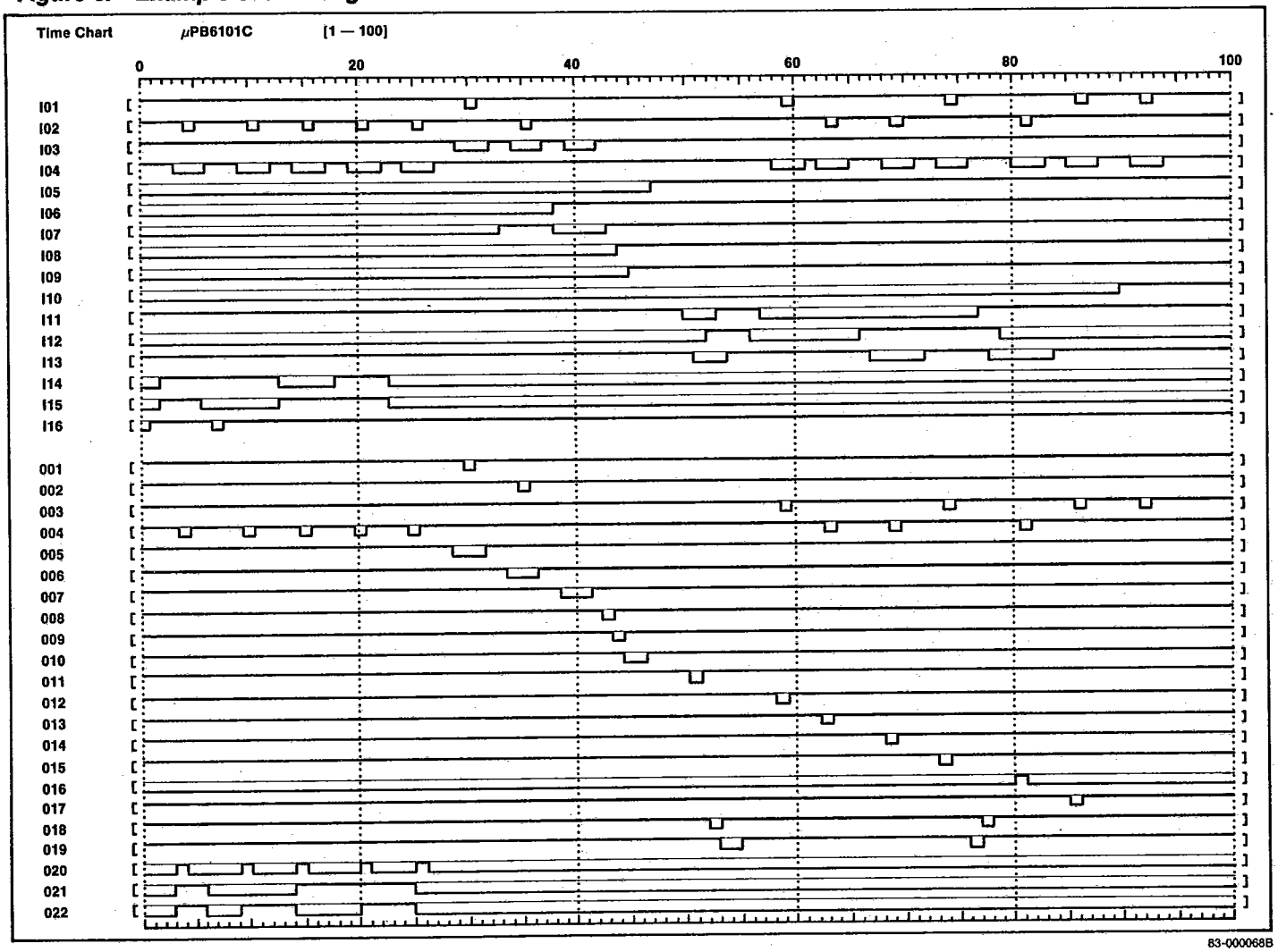


Figure 6. Example of a Timing Chart



Gate Array Development Process

Figure 7 is a flowchart showing supporting data, development steps, and customer/NEC interface options.

Customer/NEC Interface Options

NEC's computer and communications environment allows gate array designers to select the interface most suitable to their needs.

Standard Data. For the simplest interface, the customer provides a circuit diagram and test patterns. The remainder of the development process is NEC's responsibility.

Macro Converted Data. The customer provides a circuit diagram based on the macros in the Block Library plus test pattern data.

File Generated Data. The customer provides a netlist and test pattern file in NEC compatible format. The netlist is a text file describing circuit interconnections. Data may be sent to NEC on magnetic tape or a floppy disk or transmitted via telephone. The formats and procedures for handling these files will be fully specified by the appropriate NEC Design Center.

Graphic PC Generated Data. Using the PC9800 workstation, a customer can easily generate the necessary netlist and test pattern file. The PC9800 workstation supports schematic capture and limited design rule checking.

Workstation Generated Data. For this interface, the customer performs logic simulation using either workstations by Valid Systems, Mentor Graphics, Daisy Systems and others, or the TEGAS-5™ software on a main frame computer. NEC does the final compatibility check. (Separate manuals describe the various workstation interfaces.)

PG Mask Tape Interface. A separate manual will be issued when this interface becomes available.

TEGAS-5 is the trademark of Calma Company.

Development Steps

Design Rule Checking. Once the circuit interconnect data is complete, the first step of the logic validation process is the design rule check. Parameters such as cell usage, power dissipation and fan-out loading are determined and checked.

Unit Simulation [Static Logic Simulation]. Here, any coding errors and data conversion errors are eliminated.

Delay Time Simulation. Before automatic placement and routing, delay time simulation gives an accurate estimate of the expected circuit delays.

Automatic Placement and Routing. NEC's advanced software allows up to 95-percent cell utilization without resorting to manual routing.

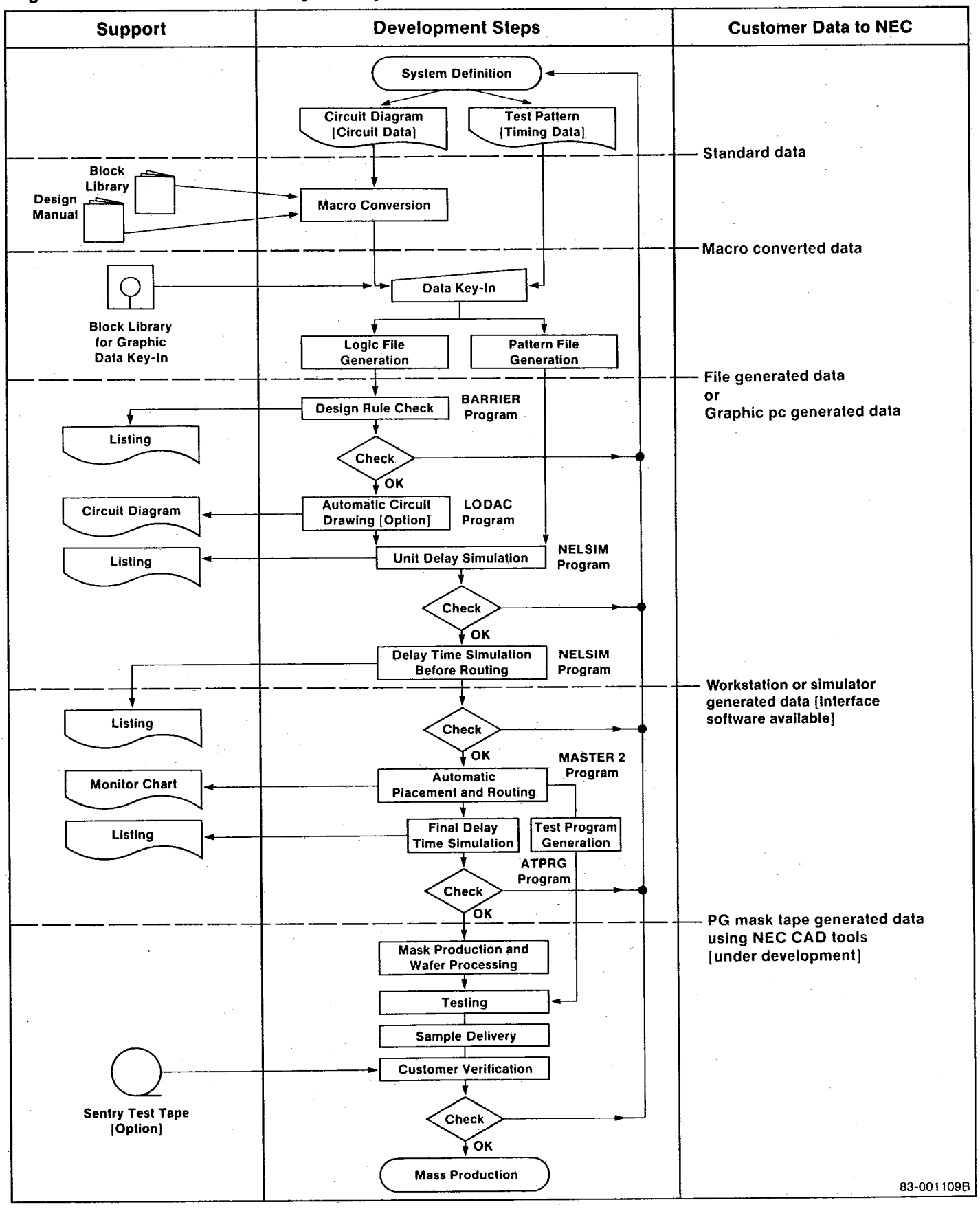
Final Delay Time Simulation. Here, wire lengths are taken into account. Results of this step provide the customer with an accurate circuit analysis.

Production. If the above steps are completed successfully, design enters actual production followed by 100-percent wafer testing.

Packaging. Successfully tested wafers are divided into individual chips, which are then die-bonded onto the customer-specified package. Chips are then wire-bonded and sealed. The dc parameters and logic functions of each chip are checked in the final test.

Prototype Evaluation. Ten engineering samples are delivered to the customer for the system function test. If customer evaluation is satisfactory, the development process is finished. NEC is ready to begin mass production.

Figure 7. Flowchart for Gate Array Development



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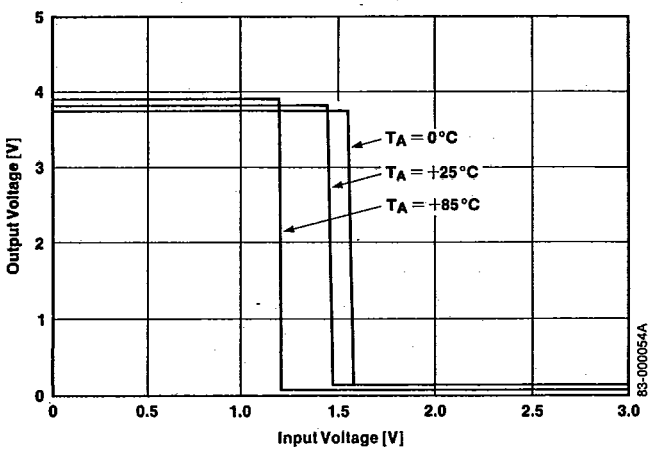
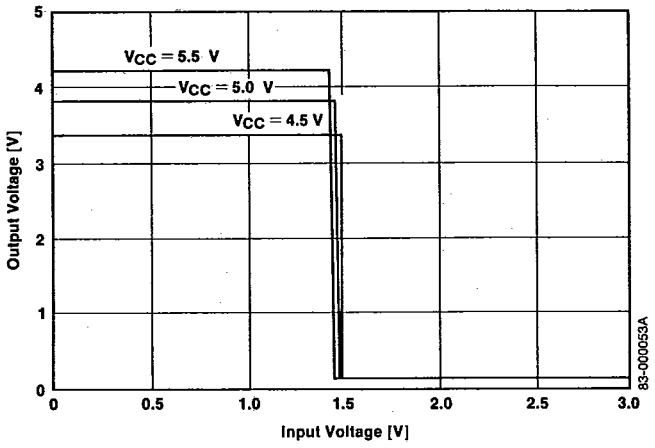
Operating Characteristics

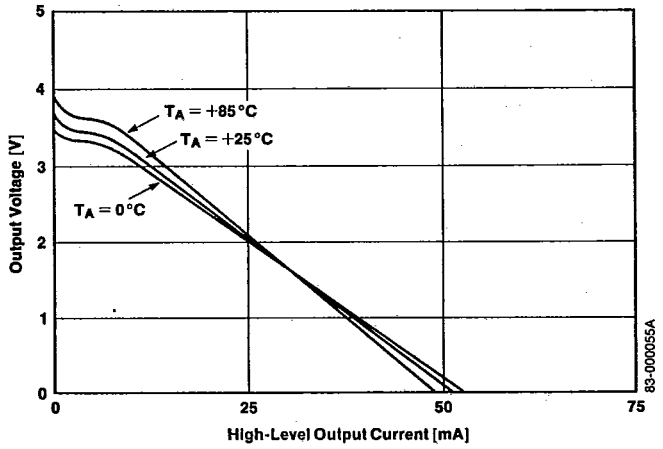
Output Voltage vs Input Voltage [V_{CC} = 5.0 V]



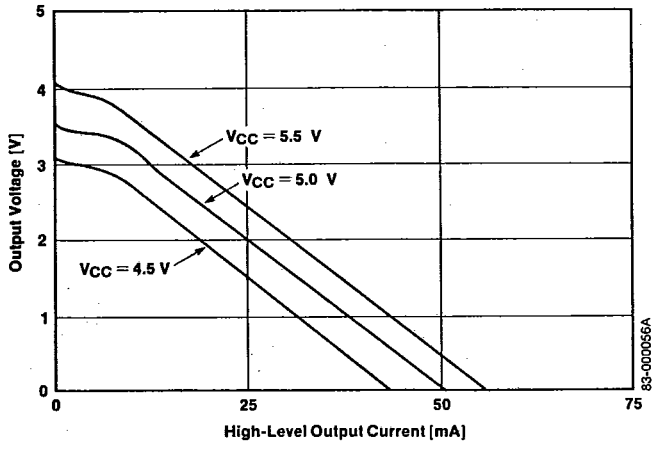
Output Voltage vs Input Voltage [T_A = +25°C]



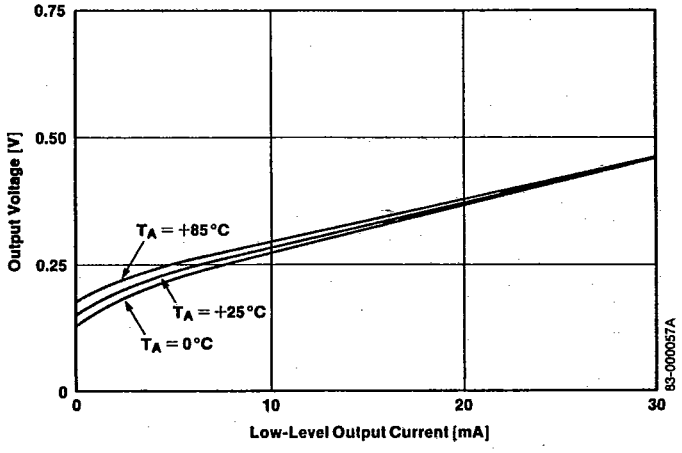
Output Voltage vs High Level Output Current [V_{CC} = 5.0 V]



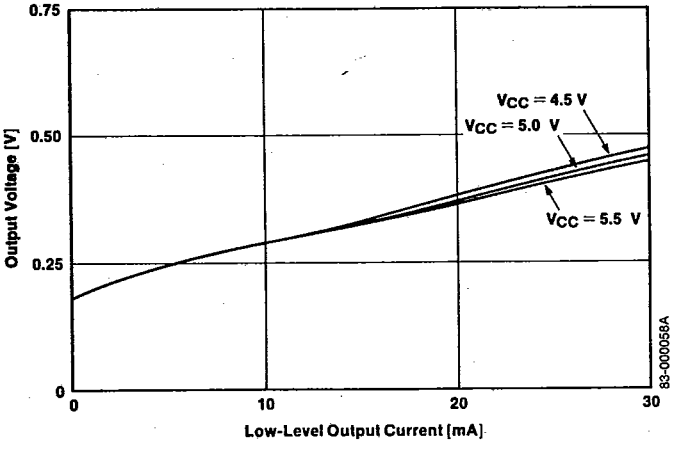
Output Voltage vs High-Level Output Current [T_A = +25°C]



Output Voltage vs Low-Level Output Current [V_{CC} = 5.0 V]



Output Voltage vs Low-Level Output Current [T_A = +25°C]



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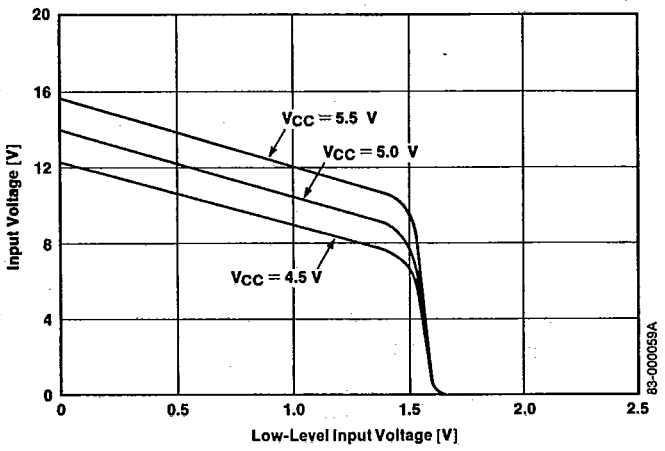
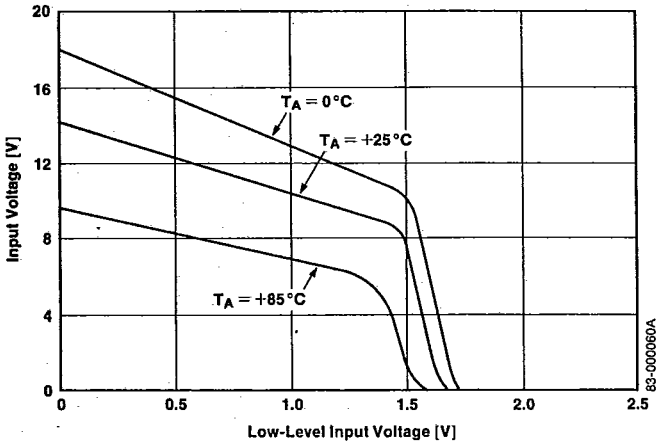
Operating Characteristics (cont)

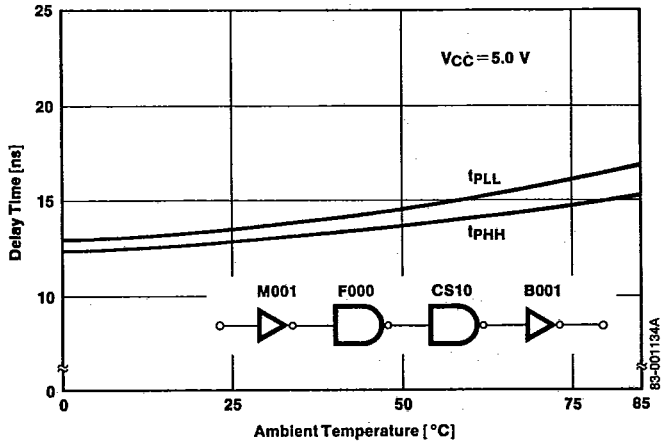
Input Current vs Low-Level Input Voltage [T_A = +25 °C]



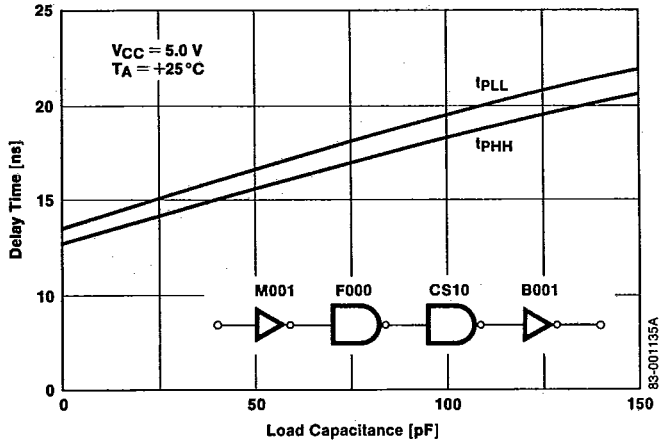
Input Current vs Low-Level Input Voltage [V_{CC} = 5.0 V]



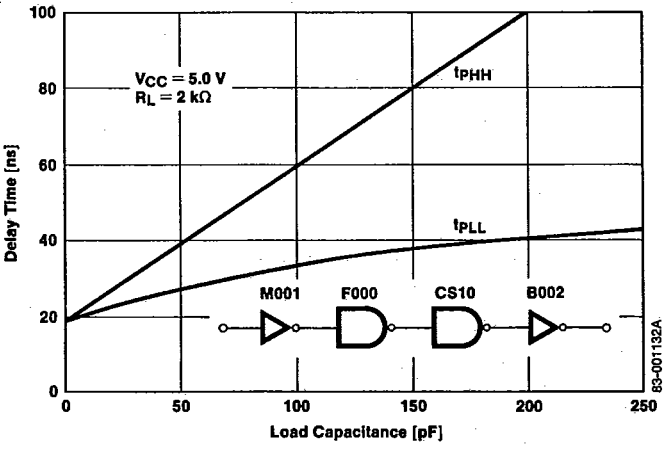
Delay Time vs Ambient Temperature
Output Buffer [Totem-Pole]



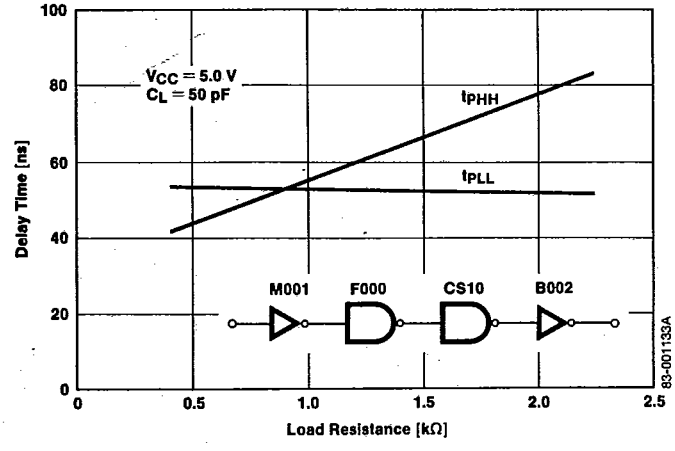
Delay Time vs Load Capacitance
Output Buffer [Totem-Pole]



Delay Time vs Load Capacitance
Output Buffer [Open Collector]



Delay Time vs Load Resistance
Output Buffer [Open Collector]



μPB6100 (TTL-2) SERIES

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Packaging Information

The μPB6100 (TTL-2) gate arrays are available in a wide variety of packages to accommodate unique applications.

Package Pin Counts

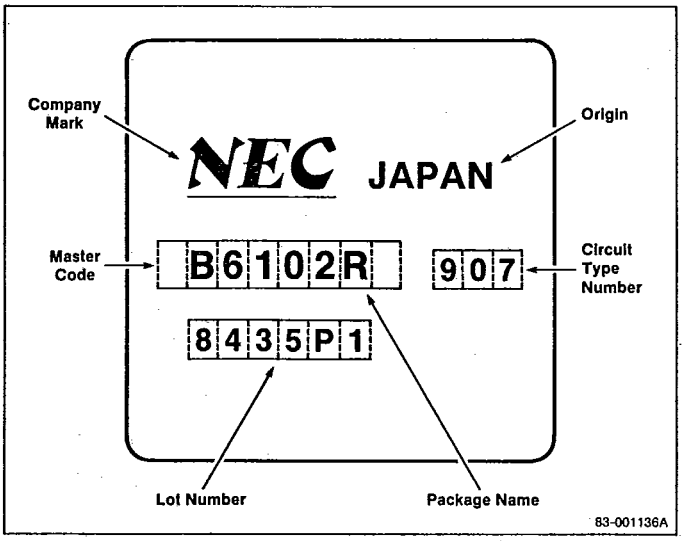
Part Number	Package Pins	
	Minimum	Maximum
μPB6101	16	44
μPB6102	20	72
μPB6103	24	72

Package Availability

	μPB6101	μPB6102	μPB6103
DIP			
16-Pin Plastic	•		
18-Pin Plastic	•		
20-Pin Plastic	•	•	
24-Pin Plastic	•	•	•
28-Pin Plastic	•	•	•
40-Pin Plastic	•	•	•
48-Pin Plastic		•	•
Shrink DIP			
64-Pin Plastic			•
Flat			
44-Pin Plastic	•	•	
52-Pin Plastic		•	
64-Pin Plastic		•	
PGA			
72-Pin Ceramic		•	•

Package Marking

Example of PGA Package



Example of Plastic Package