Signetics

74LS378
Flip-Flop

Hex D Flip-Flop With Clock Enable
Product Specification

Logic Products

FEATURES

- **Ideal for addressable register applications**
- **Six edge-triggered D flip-flops**
- **Buffered common clock**
- **Clock Enable for address and data synchronization applications**
- **See '174 for Master Reset version**

DESCRIPTION

The '378 has six edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is low.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input is also *edge-triggered and must be stable only* one set-up time prior to the LOW-to-*HIGH clock transition for predictable* operation.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS378	40MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS378N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	10LSul

NOTE:
Where a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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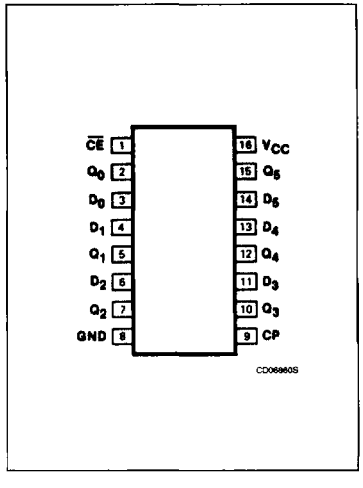
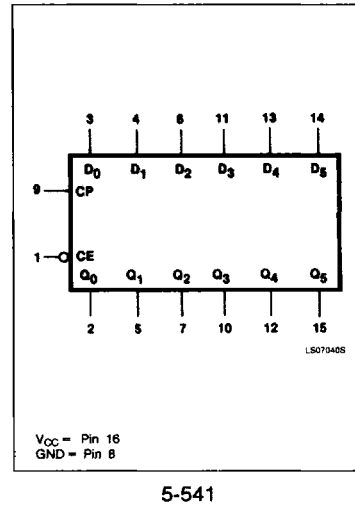
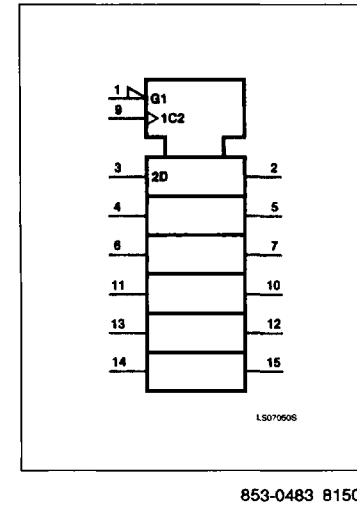
PIN CONFIGURATION



LOGIC SYMBOL

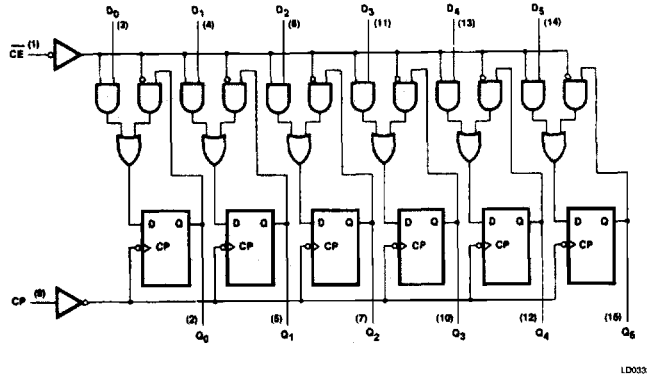


LOGIC SYMBOL (IEEE/IEC)



Flip-Flop | 74LS378

LOGIC DIAGRAM



( ) = Pin numbers
V_{CC} = Pin 16
GND = Pin 8

MODE SELECT — FUNCTION TABLE

OPERATING	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−400	μA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74LS01			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.35	0.5	V
			I_{OL} = 4mA		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			15	24	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With ground to all data inputs and the Clock Enable input and all outputs open, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

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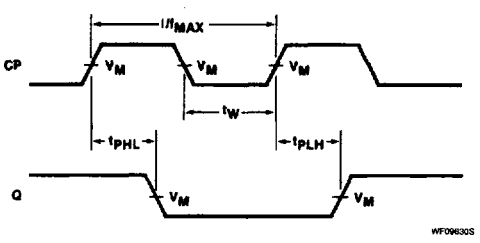
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27	ns

AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

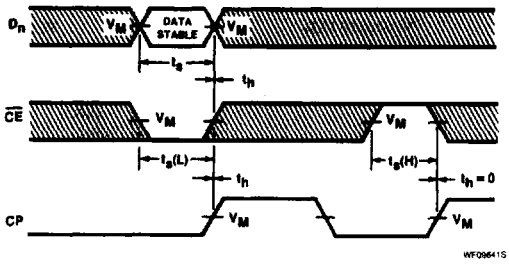
PARAMETER			TEST CONDITIONS	74LS		UNIT
				Min	Max	
t_W(L)	Clock pulse width (LOW)		Waveform 1	20		ns
t_s	Set-up time, Data to CP		Waveform 2	20		ns
t_h	Hold time, Data to CP		Waveform 2	0		0
t_S	Set-up time, $\overline{CE}$ to CP	Active state	Waveform 2	25		ns
		Inactive state		10		ns
t_h	Hold time, $\overline{CE}$ to CP		Waveform 2	5		ns

AC WAVEFORMS



V_M = 1.5V for 74 and 74S; V_M = 1.5V for 74LS.

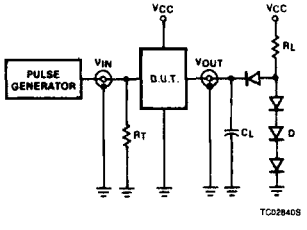
Waveform 1. Clock To Output Delays and Clock Pulse Width



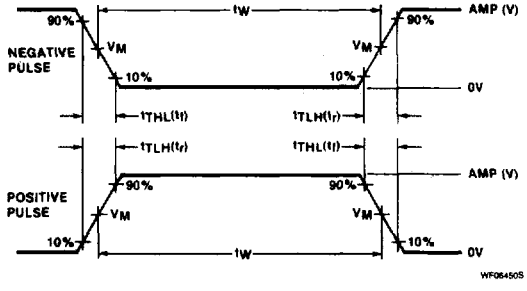
V_M = 1.5V for 74 and 74S; V_M = 1.5V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2. Data And Clock Enable Set-up And Hold Times

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns