

5430/7430 8-Input Positive-NAND Gate

T. I.	Schottky TTL				High-Speed TTL				Low-Power Schottky TTL				Standard TTL				Low-Power TTL			
	Device Type	Package			Device Type	Package			Device Type	Package			Device Type	Package			Device Type	Package		
		C	P	M/CF		C	P	M/CF		C	P	M/CF		C	P	M/CF		C	P	M/CF
FAIRCHILD	SN54S30	J	L	W	SN54H30	J	L	W	SN54LS30	J	L	W	SN5430	J	L	W	SN54L30	J	L	W
MOTOROLA	SN74S30	J	N		SN74H30	J	N		SN74LS30	J	N		SN7430	J	N		SN74L30	J	N	
N. S. C.	FM54S30 / FM9S30	D	P	F	FM54H30 / FM9H30	D	P	F	FM54LS30 / FM9LS30	D	P	F	FM5430 / FM9N30	D	P	F	DM54L30	J	N	F
PHILIPS	FC74S30 / FC9S30	D	P	F	FC74H30 / FC9H30	D	P	F	FC74LS30 / FC9LS30	D	P	F	FC7430 / FC9N30	D	P	F	DM74L30	J	N	F
SIGNETICS					MC3116	L	L	F				MC5430	L	L	F					
SIEMENS					MC3016	L	P	F	SN74LS30			MC7430	L	P	F					
FUJITSU					DM54H30	J	N		DM54LS30			DM5430	J	N		DM54L30	J	N	F	
HITACHI					DM74H30	J	N		DM74LS30			DM7430	J	N		DM74L30	J	N	F	
MITSUBISHI					GJH101/74H30				N74LS30			FJH101/7430								
NEC					S54H30	F	A	W	N74LS30			S5430	F	A	W					
TOSHIBA					N74H30	F	A	W	N74LS30	A		N7430	F	A	W					
					MB604		M		74LS30	M		MB403		M						
									HD74LS30	P		HD7430/HD2508		P						
									M74LS30	P		M53230/M5310		P						
									74LS30	C		μPB204	D	C						
												TD3430A		P						

Electrical Characteristics SN54LS30/SN74LS30  
absolute maximum ratings over operating free-air temperature range

Supply voltage, V <sub>CC</sub>	7V	Operating free-air temperature range	SN54LS	55°C to 125°C
Input voltage	7V		SN74LS	0°C to 70°C
Intermittent voltage	5.5V	Storage temperature range		-65°C to 150°C

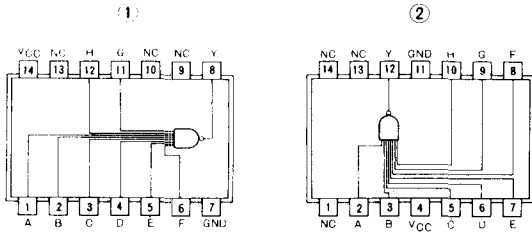
recommended operating conditions

	SN54LS30			SN74LS30			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I <sub>OH</sub>			400			-400	μA
Low-level output current, I <sub>OL</sub>			4			8	mA
Operating free-air temperature, T <sub>A</sub>	55	125	0	70	70	0	°C

electrical characteristics over recommended operating free-air temperature range

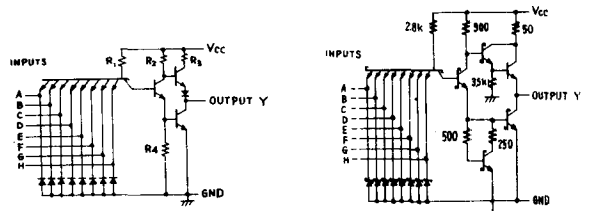
PARAMETER	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V <sub>IH</sub>	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		V
V <sub>I</sub>	Input clamp voltage	V <sub>CC</sub> - MIN, I <sub>I</sub> = 18mA		1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> - MIN, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = MAX	2.7	3.4	V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> - MIN, V <sub>IH</sub> = 2V, I <sub>OL</sub> = 4mA		0.4	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> - MAX, V <sub>I</sub> = 7V		0.1	mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> - MAX, V <sub>IH</sub> = 2.7V		20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> - MAX, V <sub>IL</sub> = 0.4V		-0.4	mA
I <sub>OS</sub>	Short-circuit output current ♦	V <sub>CC</sub> - MAX	54LS Family	20	-100
			74LS Family	20	-100
I <sub>CCH</sub>	Supply current	V <sub>CC</sub> MAX	Total, outputs high	0.35	0.5
I <sub>CCL</sub>	Supply current		Total, outputs low	0.6	1.1
I <sub>CC</sub>	Supply current	V <sub>CC</sub> 5V	Average per gate (50% duty cycle)	0.48	mA
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C		8	15
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	C <sub>L</sub> = 15pF, R <sub>L</sub> = 2kΩ		13	20

Pin Assignments (Top View)



positive logic:  
Y - ABCDEFGH  
NC - No internal connection

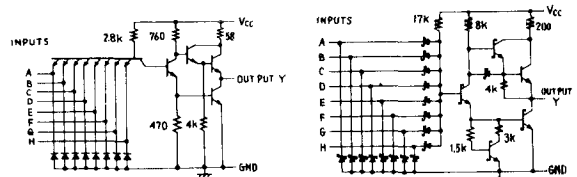
Schematics (each gate)



CIRCUIT	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	R <sub>4</sub>
'30	4k	16k	130	1k
'L30	40k	20k	300	12k

input clamp diodes not on SN54L/SN74L circuits.

'30 'L30 CIRCUITS



'H30 CIRCUIT

'LS30 CIRCUIT

Resistor values shown are nominal and in ohms.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

♦ Not more than one output should be shorted at a time, and for SN54H/SN74H and SN54S/SN74S, duration of short-circuit should not exceed 1 second.