Nuvoton

Advanced Power Control IC

NCT3012S

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1. GENERAL DESCRIPTION

The NCT3012S is Nuvoton's advanced power control IC which is specifically designed for desktop, notebook and any embedded system applications. The NCT3012S provides a mechanism to further lower the total system power consumption while the system is in S5 state. The NCT3012S could block the entire system standby power that comes from the ATX power supplier while the system is in S5 state, and it is fulfilled via the control of the external transistor. The NCT3012S is the only active IC under that circumstance so the total system power consumption is minimized. The system standby power could be resumed by the pushing of the external power button. The NCT3012S is powered by the 5VSB from the ATX power supplier, and communicates with the system through 2-wire System Management Bus (SMBus™) serial interface. The package is 8-pin ESOP green package.

2. FEATURES

2.1 General Description

- IC Communication Interface: I^{2}C® Compatible System Management Bus (SMBus™) Serial Interface
- IC Operation Power Source: 5 Volt VSB Power from ATX Power Supply
- Supports ACPI (Advanced Configuration and Power Interface) Power Sequence
- Supports Programmable Configuration Settings
- Supports Deep S5 Power Saving Control

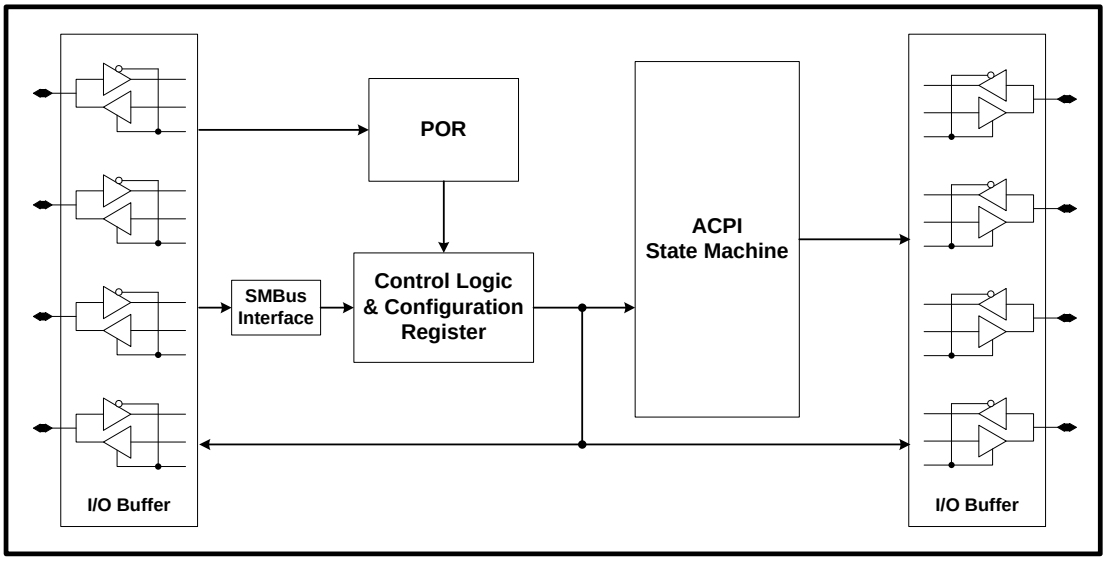
2.2 PACKAGE

- SOP-8 150mil with Exposed Pad Package
- Lead Free (ROHS Compliant) and Halogen Free SOP-8

2.3 APPLICATION

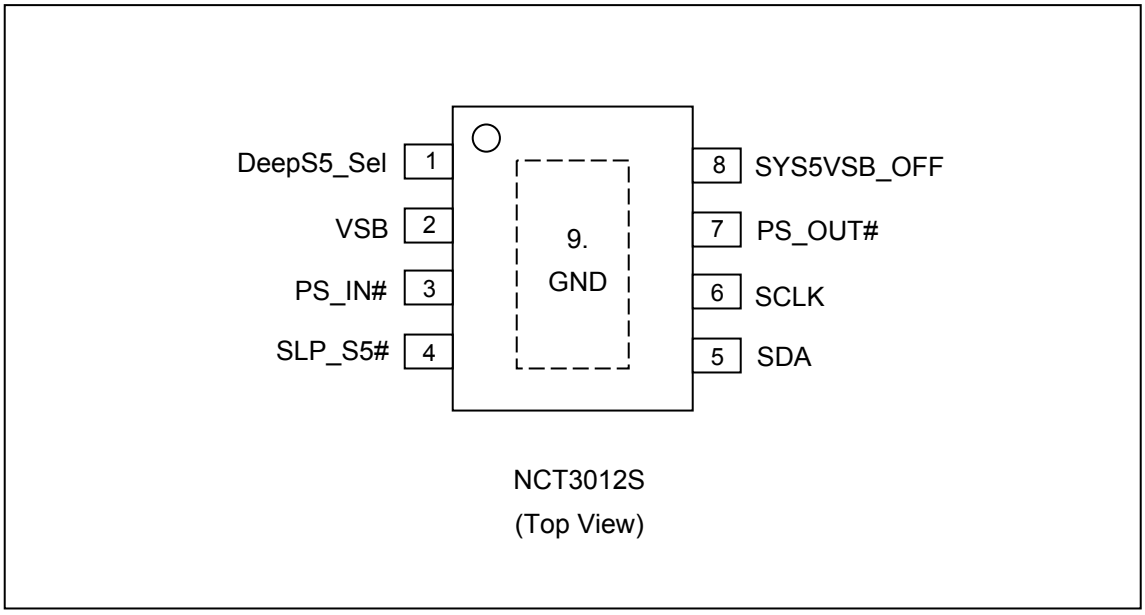
- Desktop and Notebook Computers
- Servers
- Embedded Applications

3. BLOCK DIAGRAM



4. PIN CONFIGURATION

- **NCT3012S PIN CONFIGURATION**



5. PIN DESCRIPTION

● PIN TYPE DESCRIPTION

PIN TYPE	PIN ATTRIBUTE
I/OD_{12TS}	TTL level and schmitt trigger open drain output with 12 mA sink capability
I/O_{12TS}	TTL level and schmitt trigger with 12 mA source and sink capability
I/OD_{12}	Bi-directional pin and open-drain output with 12mA sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
IN_{TS}	TTL level input pin and schmitt trigger
AIN	Input pin (Analog)
AOUT	Output pin (Analog)
IN	Input pin
OUT	Output pin
P	Power or Ground Pin

● NCT3012S PIN DESCRIPTION

PIN	SYMBOL	I/O	POWER WELL	FUNCTION
1	DeepS5_Sel	Strapping	VSB	Function Selection. Strapped by **VSB** ● Strapped to **high** : DeepS5_Sel = 1: System will enter the deep S5 state after 6 sec delays when AC power on. ● Strapped to **low** : (Default) DeepS5_Sel = 0: System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.
2	VSB	P	VSB	5V stand-by power supply for the digital circuits.
3	PS_IN#	IN_{TS}	VSB	Panel Switch Input. (Support 5V and 3V pull-high.)
4	SLP_S5#	IN_{TS}	VSB	SLP_S5# input.
5	SDA	I/OD_{12TS}	VSB	SMBus slave bi-directional Data. (5V or 3V)

6	SCLK	IN_{TS}	VSB	**SMBus Address: 0x6C** SMBus slave clock. Support 100K (5V or 3V)
7	PS_OUT# (DETECT SYS_3VSB)	AIN/ OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state. (Detect Level: 2.95V) The circuit must use 1KΩ resistor and connect to SYS_3VSB or 3VDual power source for power detection.
8	SYS5VSB_OFF	OD_{12}	VSB	This pin is to control system power for entering deeper power saving mode (Deep S3/ S5 State).
9	GND	P	VSB	Ground.

6. CONTROL AND STATUS REGISTER

6.1 Deep Sleep Enable Control Register (DPSENCTRL)

Location: **Address 00_{HEX}**

Type: **Read / Write**

Power Well : **VSB**

Reset: **Power On Reset**

Default Value: **$3C_{HEX}$ / $3D_{HEX}$**

Bit	7	6	5	4	3	2	1	0
Name	Reserved		PSOUT_N_WIDTH[5:4]		PSOUT_N_DLY[3:2]		Reserved	DpS5_En

Bit	Description
7-6	**Reserved, don't change the default value**
5-4	**Deep sleep wake-up PS_OUT# pulse width:** When system wake up from deep sleep mode, system will occur a low pulse via PS_OUT#.: 00: Don't occur low pulse 01: Pulse Width 32ms 10: Pulse Width 64ms 11: Pulse Width 160ms (default)
3-2	**Deep sleep wake-up PS_OUT# delay time :** When system wake up from deep sleep mode, system will occur a low pulse via PS_OUT# after SYS_3VSB ready and wait a delay time.. 00: Delay 5ms 01: Delay 20ms 10: Delay 80ms 11: Delay 160ms (default)
1	**Reserved, don't change the default value**
0	**Deep S5 Enable :** **Default value was determined by pin1 power on strapping.** **Strapping to High, the default value of the bit is set to "1".** **Strapping to Low, the default value of this bit is set to "0".** 0: Disable Deep S5 1: Enable Deep S5

6.2 Deep S5 Delay Time Control (DELAYCTRL)

Location: **Address 15_{HEX}**
Type: **Read / Write**
Power Well : **VSB**
Reset: **Power On Reset**
Default Value: **00_{HEX} / 02_{HEX}**

Bit	7	6	5	4	3	2	1	0
Name	Reserved		Reserved		Reserved		Delay_Time_Control [1:0]	

Bit	Description
7-2	Reserved
1-0	**Delay_Time_Control: Delay (0 /3 /6 /10) seconds to enter deep S5 state** **Default value was determined by pin1 power on strapping.** **Strapping to High, the default value of these two bits is set to "10" (6 seconds).** **Strapping to Low, the default value of these two bits is set to "00" (0 second).** 00: 0 second; 01: 3 seconds; 10: 6 seconds; 11: 10 seconds.

6.3 Chip and Version ID Register (CVID)

Location: **Address 20_{HEX}**
Type: **Read Only**
Power Well : **VSB**
Reset: **Power On Reset**
Default Value: **88_{HEX}**

Bit	7	6	5	4	3	2	1	0
Name	Chip_ID[4:0]					Ver_ID[2:0]		

Bit	Description
7-3	**Chip ID :** 10001 (default)
2-0	**Version ID :** 000 : (default)

7. ELECTRICAL CHARACTERISTIC

7.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power Supply Voltage (VSB)	-0.3 ~ 6.0	V
Input Voltage	-0.3 to VSB+0.3	V
Operating Temperature	0 to + 70	° C
Storage Temperature	-50 to +150	° C

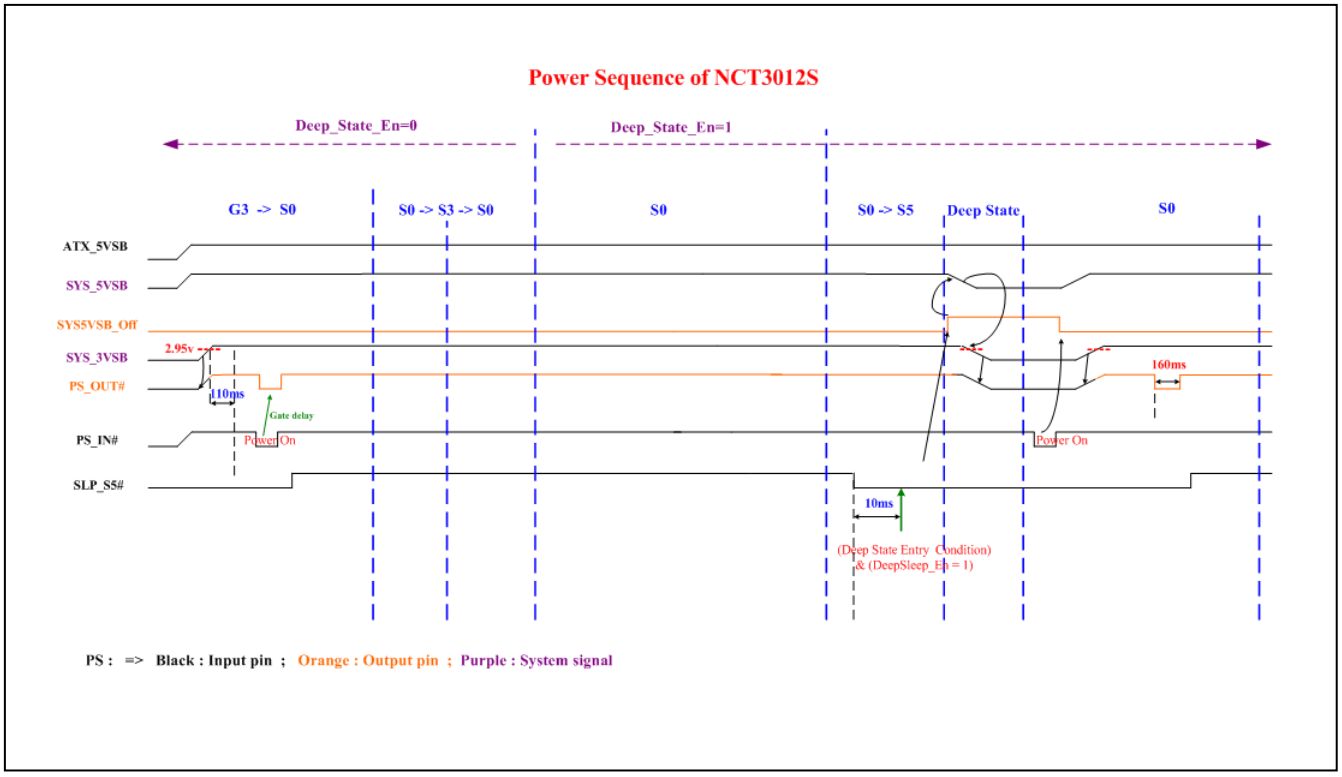
Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 DC CHARACTERISTICS

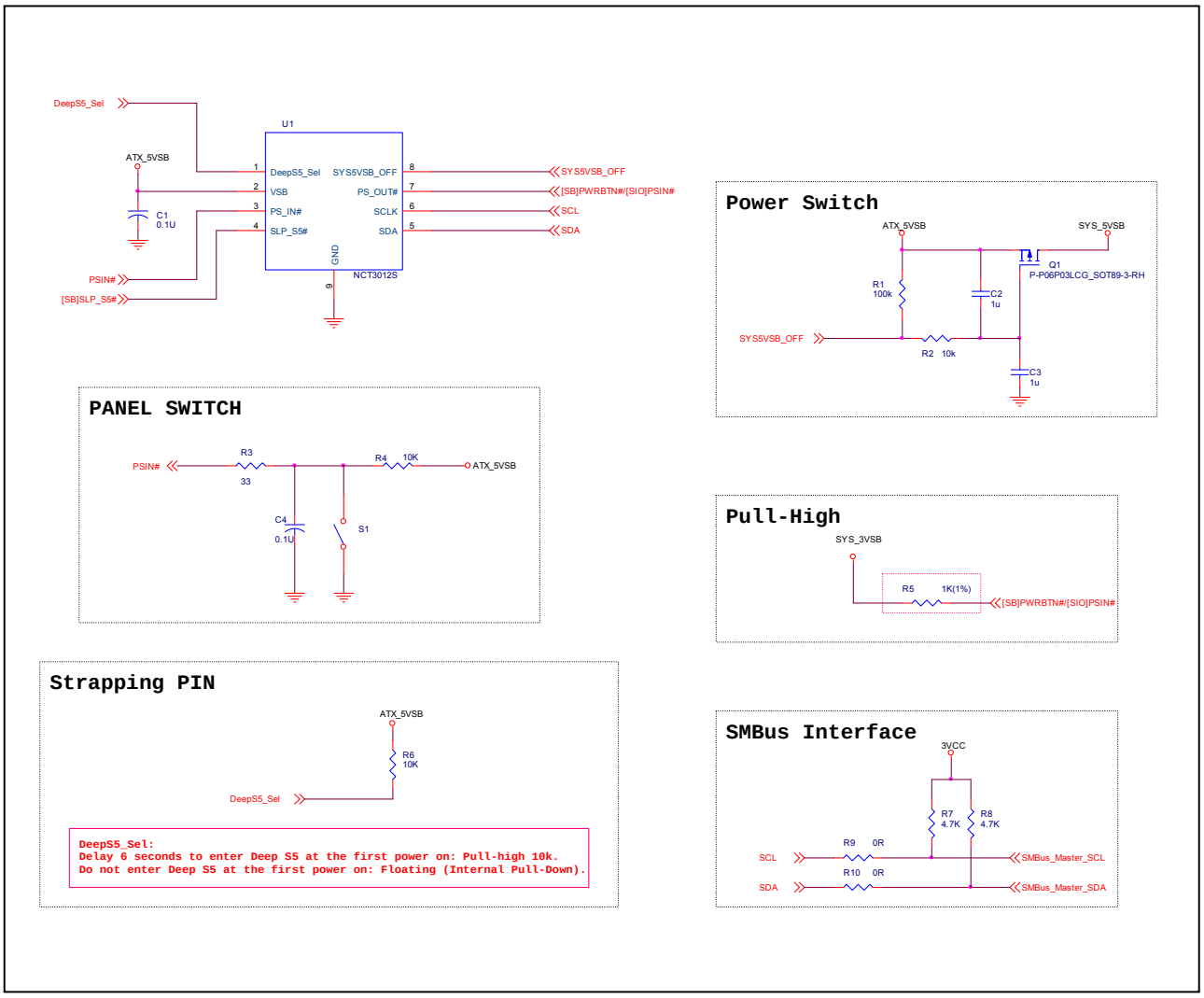
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Supply Input Voltage						
VSB Input Voltage	VSB			5.5	V	
Supply Input Current						
VSB Input Current	IVSB		2	5	mA	
I/OD$_{12TS}$ –TTL level and Schmitt trigger open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}			0.85	V	
Input High Threshold Voltage	V_{t+}	2.2			V	
Hysteresis	VTH		1.25			
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Input High Leakage	ILIH			+10	μA	
Input Low Leakage	ILIL			-10	μA	
OUT – 3.3V output pin with 12mA source and sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD12 – Open-drain output pin with 12mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
IN – TTL-level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	
Input Low Leakage	ILIL			-10	μA	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
IN_{TS} – TTL–level, Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-			0.85	V	
Input High Threshold Voltage	Vt+	2.2			V	
Hysteresis	VTH		1.25		V	
Input High Leakage	ILIH			+10	μA	
Input Low Leakage	ILIL			-10	μA	

7.3 AC CHARACTERISTICS

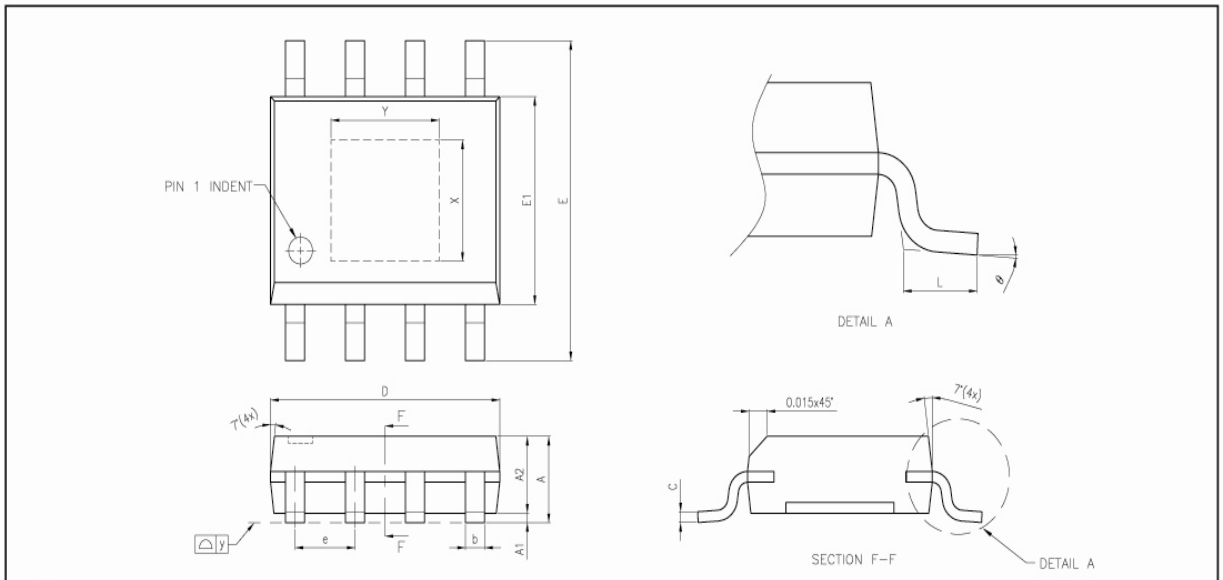


8. TYPICAL APPLICATION REFERENCE CIRCUIT



9. PACKAGE SPECIFICATIONS

ESOP-8 (150mil) PKG Outline



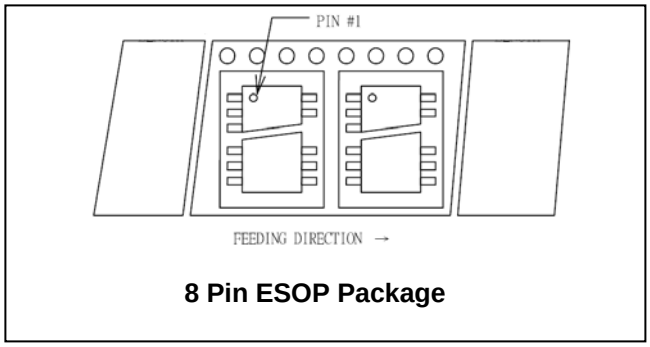
NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
⚠ A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

EXPOSED PAD DIMENSION : (MIL)
PAD SIZE: X Y
90*90

9.1 Taping Specification



8 Pin ESOP Package

10. Ordering Information

PART NUMBER	PACKAGE TYPE	SUPPLIED AS	PRODUCTION FLOW
NCT3012S	8PIN ESOP (Green package)	2,500 units/ T&R	Commercial, 0℃ to +70℃

11. TOP MARKING SPECIFICATIONS

1st line: nuvoTon – company name
2nd line: 3012S – the part number
3rd line: Tracking code 922 A X
922: Packages assembled in Year 09', week 22
A: Assembly house ID
X: The IC version (A means A; B means B…etc)

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A0	07/10/2009	ALL	Preliminary Release

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.