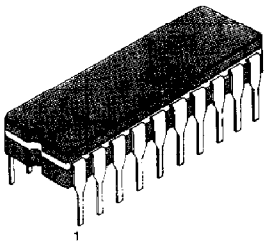
TIME SLOT ASSIGNMENT CIRCUIT (TSAC)

The KT8555 is a per channel Time Slot Assignment Circuit (TSAC) that produces 8-bit receive and transmit time slots for four 1 CHIP CODEC/Filters.
Each frame synchronization pulse may be independently assigned to a time slot in a frame of up to 64 time slots.

20 CERDIP



FEATURES

- **Single, 5V operation**
- **Low power consumption: 5mW**
- **Controls four 1 CHIP CODEC/Filters**
- **Independent transmit and receive frame syncs and enables**
- **8 channel unidirectional mode**
- **Up to 64 time slots per frame**
- **Compatible with KT8554/7 CODECs**
- **TTL and CMOS compatible**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT8555J	20 Ceramic DIP	−20~+125°C

PIN CONFIGURATION

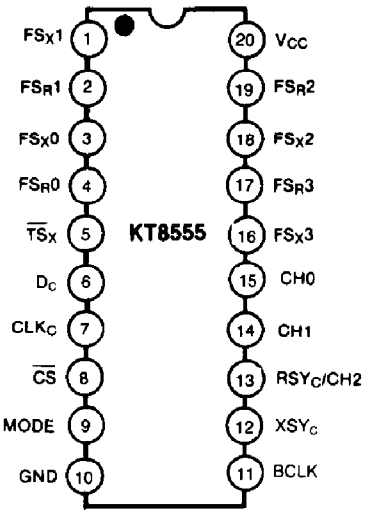


Fig. 1

PIN DESCRIPTION

Pin No	Symbol	Description
3 1 18 16	FS_X0 FS_X1 FS_X2 FS_X3	A frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
4 2 19 17	FS_R0 FS_R1 FS_R2 FS_R3	A frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
5	$\overline{TS_X}$	This pin pulls low during any active transmit time slot. (N-channel open drain)
6	D_C	The input for an 8 bit serial control word. $\overline{X}$ is the first bit clocked in.
7	CLK_C	The clock input for the control interface.
8	$\overline{CS}$	The active-low chip select for the control interface.
9	MODE	Mode 1 = Open or V_{CC} Mode 2 = Gnd
10	GND	Ground
11	BCLK	The bit clock input
12	XSY_C	The transmit TSO sync pulse input. Must be synchronous with BCLK.
13	RSY_C/CH2	The transmit time slot 0 sync pulse input. Must be synchronous with BCLK. In mode 1 this input is the receive time slot 0 sync pulse, RSY_C, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
14	CH1	The input for the NSB (next significant bit) of the channel select word.
15	CH0	The input for the LSB (last significant bit) of the channel select word, which defines the frame sync output affected by the following control word.
20	V_{CC}	Power supply pin. 5V ± 5%

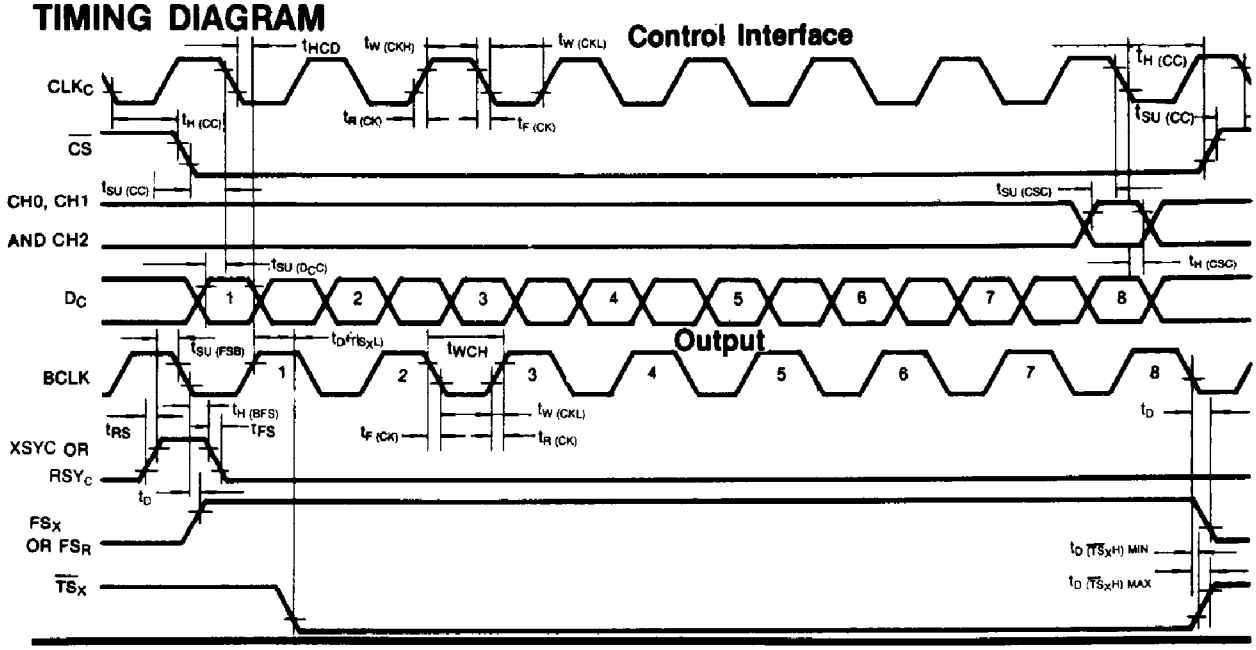
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_I	$V_{CC}+0.3 \sim -0.3$	V
Output Voltage	V_O	$V_{CC}+0.3 \sim -0.3$	V
Operating Temperature Range	T_{OPR}	$-25 \sim 125$	°C
Storage Temperature Range	T_{STG}	$-65 \sim 150$	°C
Lead Temperature (Soldering, 10 secs)	T_{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted; V_{CC} = 5.0V ± 5%, Ta = 0°C ~ 70°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	I_{CC}	BCLK = 2.048MHz, all outputs open		1	1.5	mA
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.7	V
Input Current 1	I_{I1}	All Inputs Except Mode, $V_{IL} < V_{IN} < V_{IH}$	−1		1	μA
Input Current 2	I_{I2}	Mode, V_{IN} = 0V	−100			μA
Output Voltage High	V_{OH}	FS_X and FS_R Ouputs, I_{OH} = 3mA	2.4			V
Output Voltage Low	V_{OL}	FS_X and FS_R Outputs, I_{OL} = 3mA			0.4	V
		TS_X output, I_{OL} = 3mA			0.4	V
Rise and Fall Time of Clock	$t_{R(CK)}$ $t_{F(CK)}$	BCLK, CLK_C			50	nS
Delay to $\overline{TS_X}$ Low	$t_{D(\overline{TS_X}L)}$	C_L = 50pF			140	nS
Delay to $\overline{TS_X}$ High	$t_{D(\overline{TS_X}H)}$	R_L = 1KΩ to V_{CC}	30		100	nS
Hold Time from BCLK to Frame Sync	$t_{H(BFS)}$		50			nS
Set-Up Time from Frame Sync to BLCK	$t_{SU(FSB)}$		30			nS
Delay Time from BLCK Low to $FX_{X/R}$0-3 High or Low	t_D	C_L = 50pF			50	nS
Hold Time from Channel Select to CLKC	$t_{H(CSC)}$		50			nS
Set-Up Time from Channel Select to CLKC	$t_{SU(CSC)}$		30			nS
Period of Clock	t_{CK}	BCLK, CLK_C	240			nS
Width of Clock High	$t_{W(CKH)}$	BCLK, CLK_C	50			nS
Width of Clock Low	$t_{W(CKL)}$	BCLK, CLK_C	50			nS
Set-Up Time from D_C to CLKC	$t_{SU(D_C C)}$		30			nS
Hold Time from CLKC to D_C	$t_{H(CD_C)}$		50			nS
Set-Up Time from CS to CLKC	$t_{SU(CC)}$		30			nS
Hold Time from CLKC to CS	$t_{H(CC)}$		100			nS

TIMING DIAGRAM



APPLICATION INFORMATION

OPERATING CONTROL MODE 1

The KT8555 is a control interface which requires an 8 bit serial control word. Either one of the frame sync output group, FS_X0 to FX_X3 or FS_R0 to FS_R3, affected by the control word is defined by the two bits, $\overline{X}$ and $\overline{R}$. Time slot selected from 0 to 63 is specified. A frame sync output is highly active for one time slot which is equivalent to 8 cycles of BCLK. Up to 64 time slots are allowed to form a frame. There are two operational mode. In mode 1, each channel of transmit and receive direction has different time slot assigned. This mode can be selected by either leaving pin 9 (MODE) opened or connecting it with V_{CC}. In such a case, pin 13 is RSYC input defining the start of each receive frame while four outputs, FS_R0 to FS_R3, are assigned with respect to RSYC. On the other hand, start of each transmit frame is defined by XSYC input by which output FS_X0 to FS_X3, are assigned. XSYC and RSYC can be phase related. Channels from 0-3 are selected by the input CH0 and CH1 (refer to the table 1).

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into D_C input

CONTROL DATA FORMAT

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						.
						.
						.
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	0	0	0	0	0	32
1	0	0	0	0	01	33
						.
						.
						.
1	1	1	1	1	1	63

CH1	CH0	Channel Selected
0	0	Assign to FS_X0 and/or FS_R0
0	1	Assign to FS_X1 and/or FS_R1
1	0	Assign to FS_X2 and/or FS_R2
1	1	Assign to FS_X3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE 1. OPERATING CONTROL MODE 1

OPERATING CONTROL MODE 2

In mode 2, all 8 frame sync outputs can be assigned with respect to XSYC input. The mode 2, selected by connecting pin 9 (MODE) to GND, enables the KT8555 TSAC suitable for an 8-channel undirectional controller and for a system where both transmit and receive direction of each channel have same time slot assigned. For instance, FS_X and FS_R input of 1 CHIP CODEC are hard wired together. The channel assigned has its channel selected by CH0, CH1 and CH2 (refer to table 2).

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	Assign time slot to selected output
1	0	Assign time slot to selected output
1	1	Disable both selected output

TABLE 2. OPERATING CONTROL MODE 2

APPLICATION CIRCUIT

The KT8555 TSAC combined with any kind of 1 CHIP CODEC from KT8554/7 series can obtain data timing as illustrated in Fig. 3. Even though FS_X output goes high before BCLK gets high, the D_X output of the 1 CHIP CODEC remains in the TRI-STATE mode will until both outputs are high. The eight bit period is shortened to avoid PCM data clash at PCM pre-highway.

Alternatively, full 8 bits can be obtained by inverting the BCLK to the 1 CHIP CODEC devices, thereby rising edges of BCLK and $FS_{X/R}$ are aligned.

Fig. 4 is typical timing of the control data interface.

Fig. 5 is the typical application circuit at operating control mode 2.

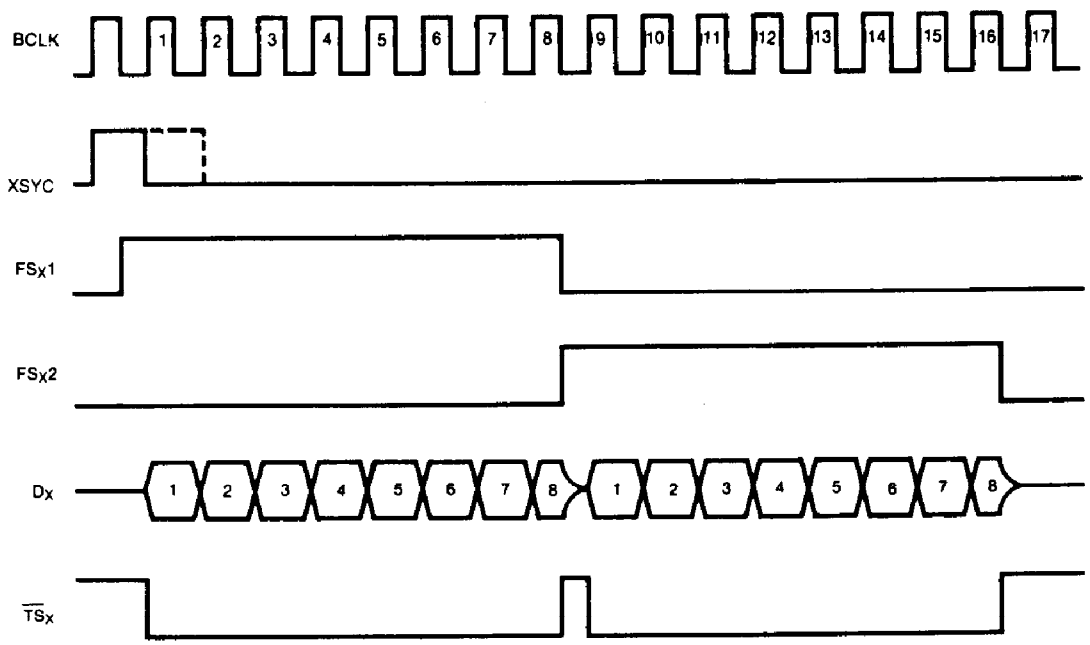


Fig. 3 **Transmit Data Timing**

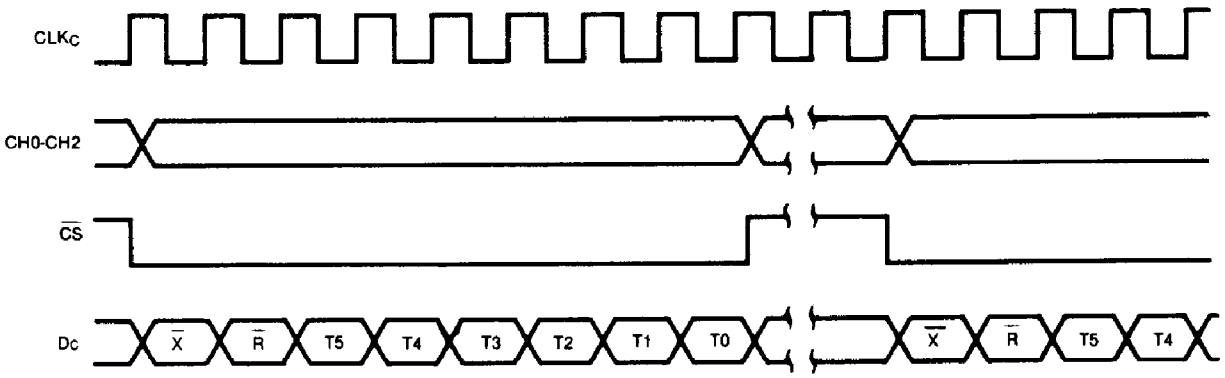
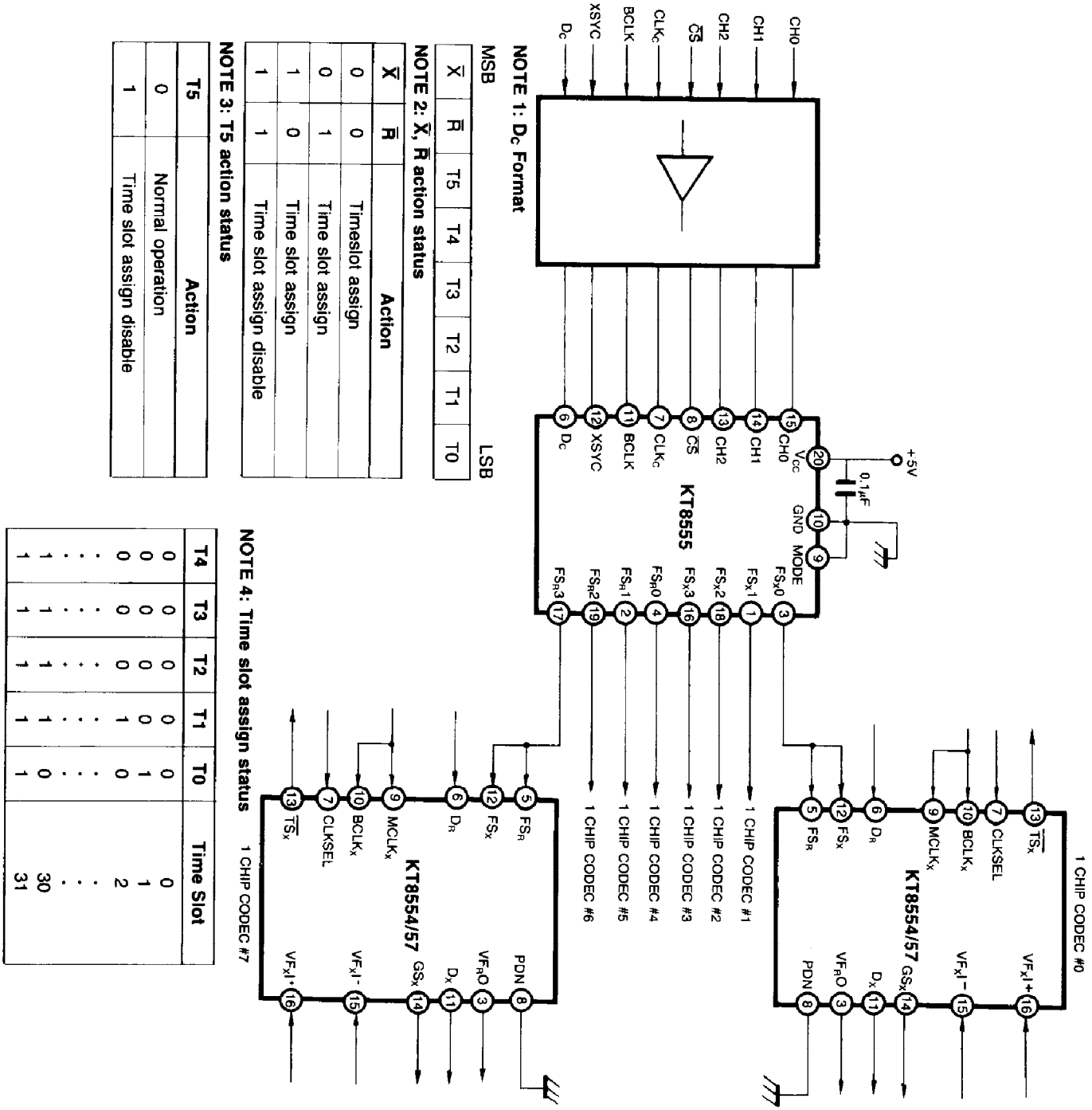


Fig. 4 **Control Data Timing**



NOTE 1: D_C Format

MSB

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

LSB

NOTE 2: $\overline{X}$, $\overline{R}$ action status

$\overline{X}$	$\overline{R}$	Action
0	0	Timeslot assign
0	1	Time slot assign
1	0	Time slot assign
1	1	Time slot assign disable

NOTE 3: T5 action status

T5	Action
0	Normal operation
1	Time slot assign disable

NOTE 4: Time slot assign status

T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	0	30
1	1	1	1	1	31

NOTE 5: Different time slot assign for RX and TX respectely also available.

Fig. 5 Digital interface on a typical subscriber linecard