Signetics

FAST 74F160A, 74F161A, 74F162A, 74F163A Counters

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter
Product Specification

FAST Products

FEATURES

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered Clock**
- **Asynchronous Reset ('F160A, 'F161A)**
- **Synchronous Reset ('F162A, 'F163A)**
- **High-speed synchronous expansion**
- **Typical count rate of 120MHz**

DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit ('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F160A	130MHz	46mA
74F161A	130MHz	46mA
74F162A	130MHz	46mA
74F163A	130MHz	46mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F160AN, N74F161AN N74F162AN, N74F163AN
16-Pin Plastic SO	N74F160AD, N74F161AD N74F162AD, N74F163AD

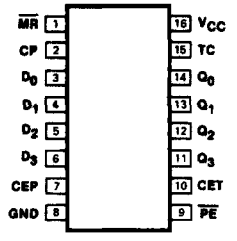
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CEP	Count Enable Parallel input	1.0/1.0	20μA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20μA/1.2mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset input (active-Low)	1.0/2.0	20μA/1.2mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input (active-Low)	1.0/2.0	20μA/1.2mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
TC	Terminal Count output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

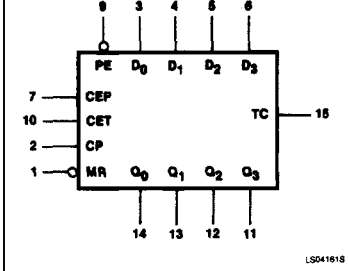
PIN CONFIGURATION

'F160A



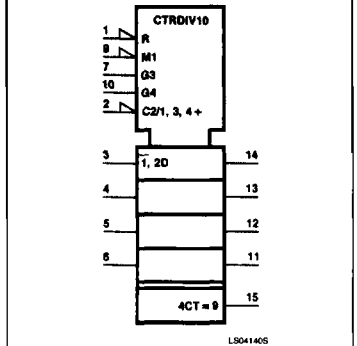
LOGIC SYMBOL

'F160A



LOGIC SYMBOL (IEEE/IEC)

'F160A



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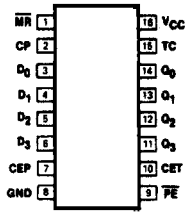
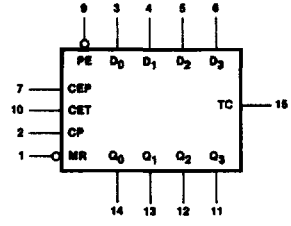
PIN CONFIGURATION

'F161A



LOGIC SYMBOL

'F161A



LOGIC SYMBOL

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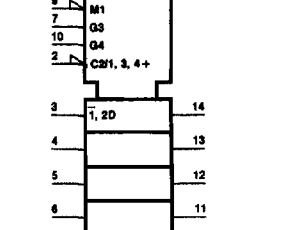
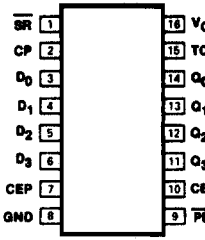


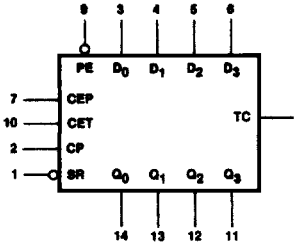
PIN CONFIGURATION

'F162A



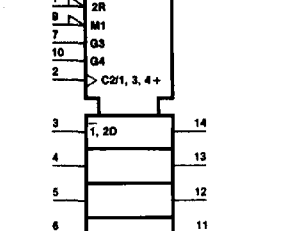
LOGIC SYMBOL

'F162A



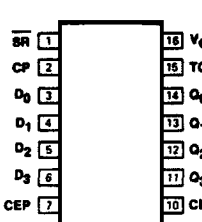
LOGIC SYMBOL

'F162A



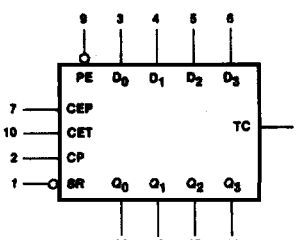
PIN CONFIGURATION

'F163A



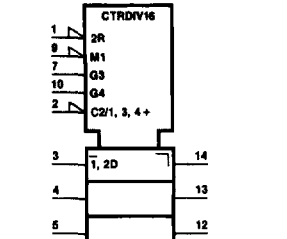
LOGIC SYMBOL

'F163A



LOGIC SYMBOL

'F163A



The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the $D_0 - D_3$ inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) in 'F160A and 'F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 'F162A and 'F163A, the clear function is synchronous. A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) to Low levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

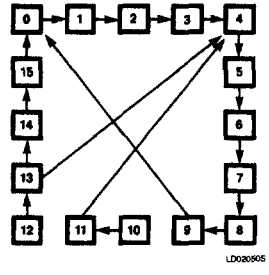
The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

The TC output is subject to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

STATE DIAGRAMS

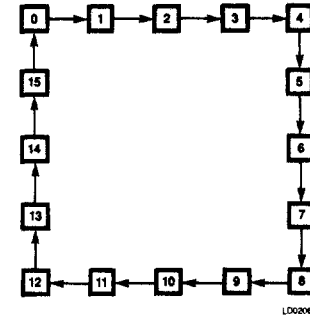
Logic Equations: Count Enable = CEP•CET•PE
$TC = Q_0 \bullet \overline{Q}_1 \bullet Q_2 \bullet Q_3 \bullet CET$

'F160A, 'F162A



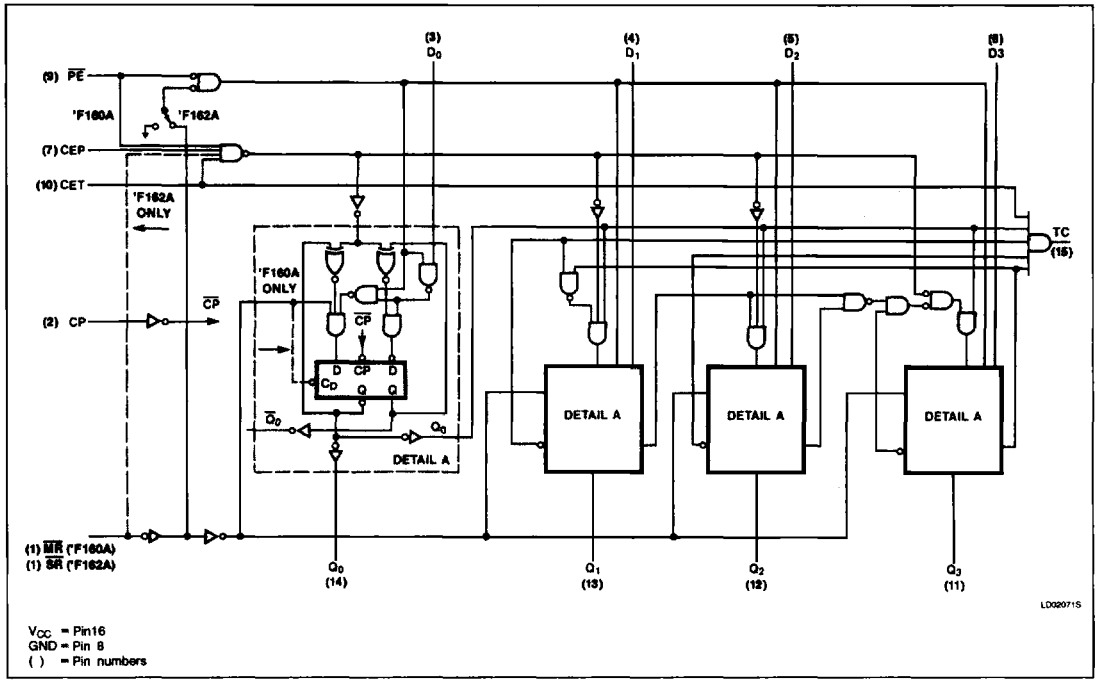
Logic Equations: Count Enable = CEP•CET•PE
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

'F161A, 'F163A



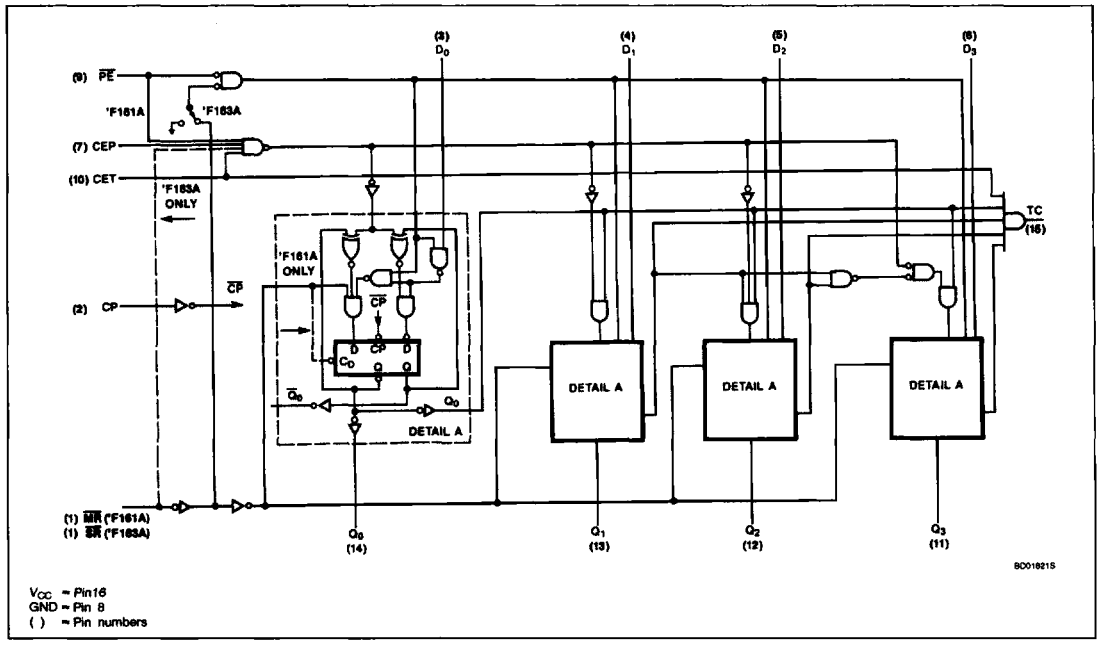
6

LOGIC DIAGRAM, 'F160A, 'F162A



V_{CC} = Pin16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM, 'F161A, 'F163A



V_{CC} = Pin16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE, 'F160A, 'F161A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H H	↑ ↑	X X	X X	l l	l h	L H	L (1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H H	X X	l X	X l(2)	h h	X X	q_n q_n	(1) L

MODE SELECT — FUNCTION TABLE, 'F162A, 'F163A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L (2)
Count	h	↑	h	h	h	X	count	(2)
Hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	(2) L

H = High voltage level steady state.
L = Low voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High clock transition.
l = Low voltage level one setup time prior to Low-to-High clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition.

NOTES:

(1) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 'F161A and HLLH for 'F160A).

(2) The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A).

6

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	*Operating free-air temperature range*	*0 to +70*	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.50	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 2.7V				40	μA
		Other inputs					20	μA
I_{IL}	Low-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Other inputs				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			42	55	mA
		I_{CCL}				49	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} is measured with $\overline{PE}$ input High, again with $\overline{PE}$ input Low, all other inputs High and outputs open. I_{CCL} is measured with Clock input High, again with Clock input Low all other inputs Low, and outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F160A, 74F162A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = High	2.0 4.0	4.5 7.0	7.0 10.0	2.0 4.0	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = Low	2.0 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	4.5 4.5	10 10	10.5 9.5	4.5 4.5	15 15	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	4.5 4.5	6.5 7.0	1.5 2.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F160A	Waveform 3	6.5	9.0	12	6.5	13	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F160A	Waveform 3	6.0	8.0	10.0	5.5	11.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F160A, 74F162A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 5	5.0 5.0			5.5 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	11 7.0			11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CEP or CET to CP		Waveform 4	11.0 6.0			11.0 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CEP or CET to CP		Waveform 4	0 0			0 0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (load), High or Low		Waveform 1	4.0 5.0			4.0 6.5		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (count), High or Low		Waveform 1	4.0 5.5			4.0 6.0		ns
$t_W(L)$	$\overline{MR}$ pulse width Low	'F160A	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	'F160A	Waveform 3	5.0			6.0		ns

6

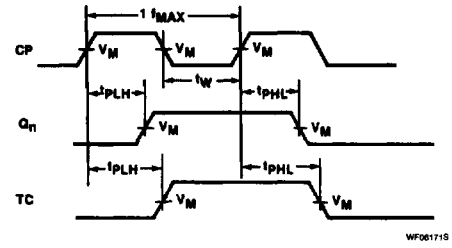
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	74F161A, 74F163A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = High	2.0 4.0	4.0 6.5	6.5 10.5	2.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1 $\overline{PE}$ = Low	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F161A	Waveform 3	6.5	8.5	12.5	5.5	13	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F161A	Waveform 3	6.0	8.5	11.0	5.0	12.0	ns

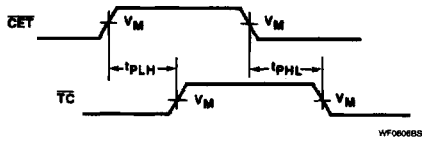
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	74F161A, 74F163A					UNIT
				$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	9.0 6.5			9.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CEP or CET to CP		Waveform 4	10.5 7.0			10.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CEP or CET to CP		Waveform 4	0 0			0 0		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (load), High or Low		Waveform 1	4.0 5.0			4.0 5.5		ns
$t_W(H)$ $t_W(L)$	Clock pulse width (count), High or Low		Waveform 1	4.0 6.0			4.0 7.0		ns
$t_W(L)$	$\overline{MR}$ pulse width Low	'F161A	Waveform 3	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	'F161A	Waveform 3	6.0			6.5		ns

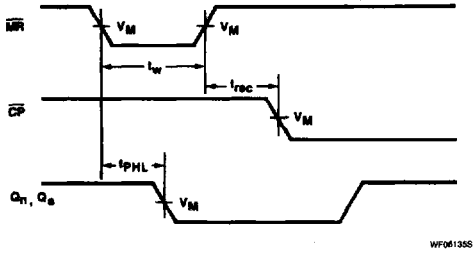
AC WAVEFORMS



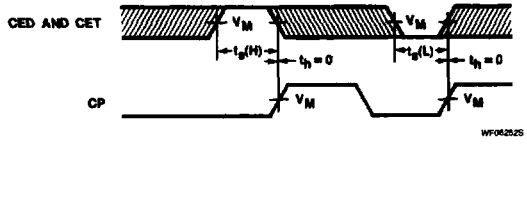
Waveform 1. Clock to Output Delays, Maximum Clock Frequency, and Clock Pulse Width



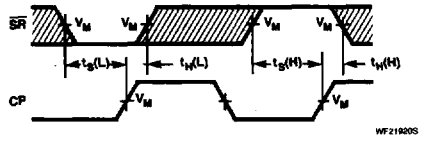
Waveform 2. Propagation Delays CET Input to TC Output



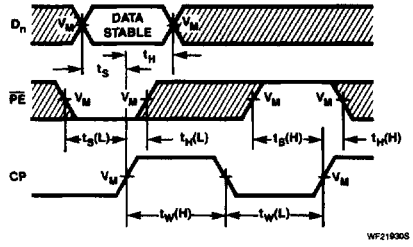
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time ('F160A, 'F161A)



Waveform 4. CEP and CET Setup and Hold Times



Waveform 5. Synchronous Reset Setup and Hold Times

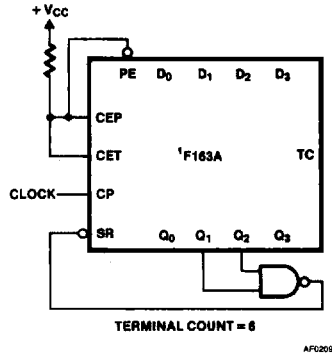


Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times

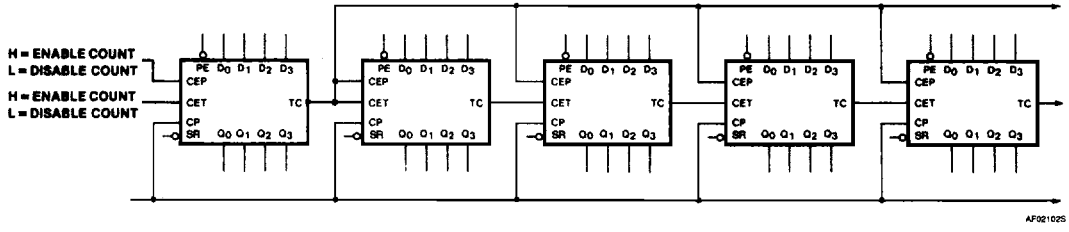
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

6

APPLICATION

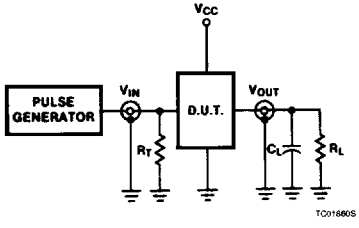


a.

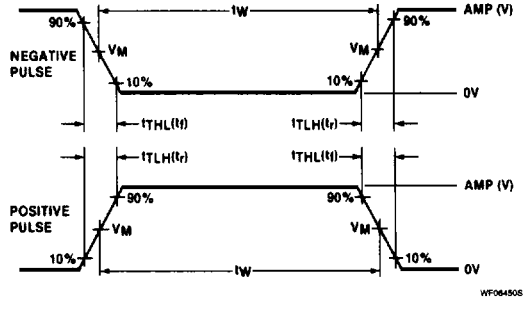


b. Synchronous Multistage Counting Scheme

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



VM = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns