Texas Instruments

TLV07 36-V Precision, Rail-to-Rail Output Operational Amplifier

1 Features

- Low Offset Voltage: 100 µV (Maximum)
- Rail-to-Rail Output
- Low Noise: 19 nV / √Hz
- Unity-Gain Stable
- RFI Filtered Inputs
- Input Range Includes Negative Supply
- Rail-to-Rail Output
- Gain Bandwidth: 1 MHz
- Low Quiescent Current: 930 µA
- Full Industrial Temperature Range: –40°C to +125°C
- Offered in the Industry-Standard 8-Pin SOIC Package

2 Applications

- Battery Testers
- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers

3 Description

The TLV07 device is a 36-V, single-supply, low-noise, precision operational amplifier (op amp) manufactured using TI's laser trim operational amplifier technology. Each amplifiers' input offset voltage is trimmed in production to obtain a low offset voltage of 100 µV (maximum).

The TLV07 offers outstanding dc precision and ac performance, including rail-to-rail output, low offset voltage (±100 µV, maximum) and 1-MHz bandwidth. The TLV07 is stable at G = 1 with capacitive loads up to 200 pF. The input can operate 100 mV below the negative rail and within 2 V of the positive rail. This wide input voltage range, combined with a high CMRR of 120 dB, make the TLV07 well-suited when operated in the non-inverting configuration.

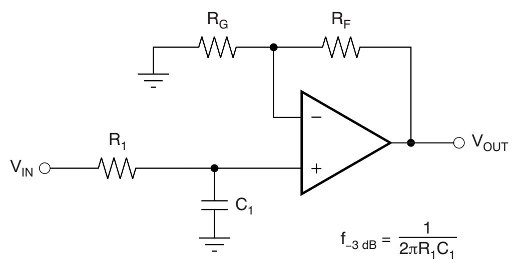
The TLV07 op amp is specified from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV07	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Single Pole Low-Pass Filter With Gain



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

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4 Revision History

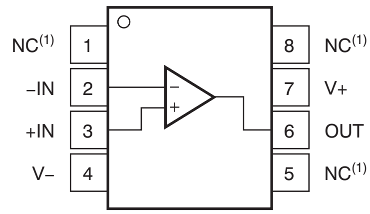
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2017) to Revision A **Page**

- First release of production-data data sheet 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



(1) NC- no internal connection

Pin Functions: TLV07

NAME	NO.	I/O	DESCRIPTION
–IN	2	I	Negative (inverting) input
+IN	3	I	Positive (non-inverting) input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.[1]

	MIN	MAX	UNIT
Supply voltage	–20	20	V
Single supply voltage		40	V
Signal input pin voltage	(V–) – 0.5	(V+) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current[2]	Continuous		
Operating ambient temperature, T_A	–40	125	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V_S = V+ – V–)	2.7	36	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information: TLV07

THERMAL METRIC		TLV07 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

6.5 Electrical Characteristics

at T_A = 25°C, V+ = +15 V, V- = -15 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			50	±100	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		±0.9		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 36 V		0.3		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±40		pA
		T_A = –40°C to 125°C		±3		nA
I_{OS}	Input offset current			±4		pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.7		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		19		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) - 0.1 V < V_{CM} < (V+) – 2 V	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1		MHz
SR	Slew rate	G = 1		0.4		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step		20		µs
		To 0.01% (12-bit), V_S = ±18 V G = 1 10-V step		28		µs
OUTPUT						
V_O	Voltage output swing from rail	R_L = 10 kΩ		120		mV
I_{SC}	Short-circuit current			17		mA
R_O	Open-loop output resistance	f = 1 MHz I_O = 0 A		900		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 A		930	1800	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–40		125	°C

6.6 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

Table 1. Characteristic Performance Measurements

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CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 9
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Large-Signal Settling Time	Figure 29
Short-Circuit Current vs Temperature	Figure 30
Maximum Output Voltage vs Frequency	Figure 31
EMIRR IN+ vs Frequency	Figure 32

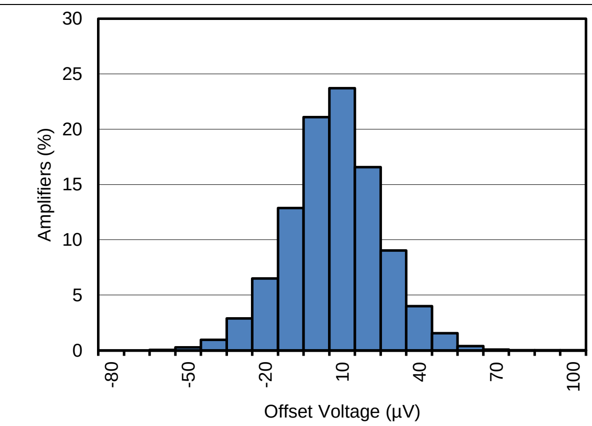


Figure 1. Input Offset Voltage Distribution

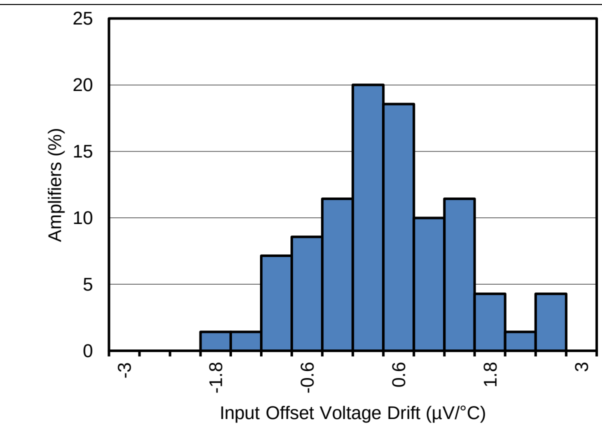


Figure 2. Input Offset Voltage Drift Distribution

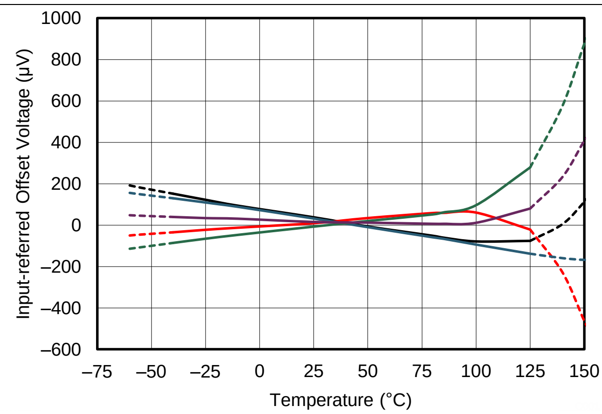


Figure 3. Input Offset Voltage vs Temperature

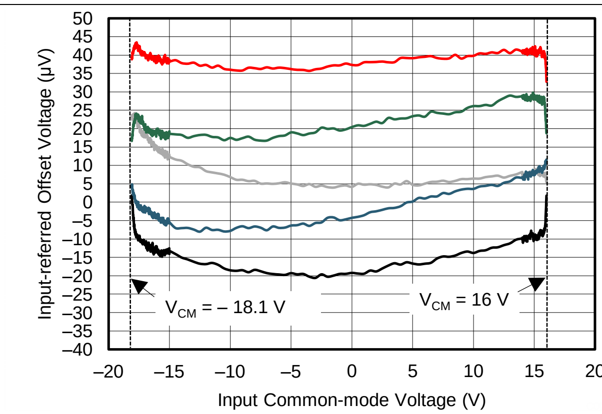


Figure 4. Input Offset Voltage vs Common-Mode Voltage

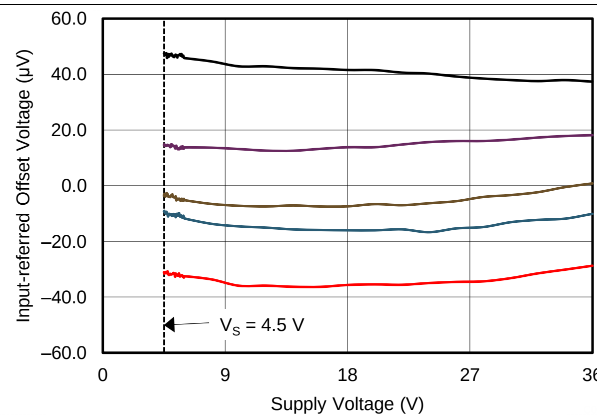


Figure 5. Offset Voltage vs Power Supply

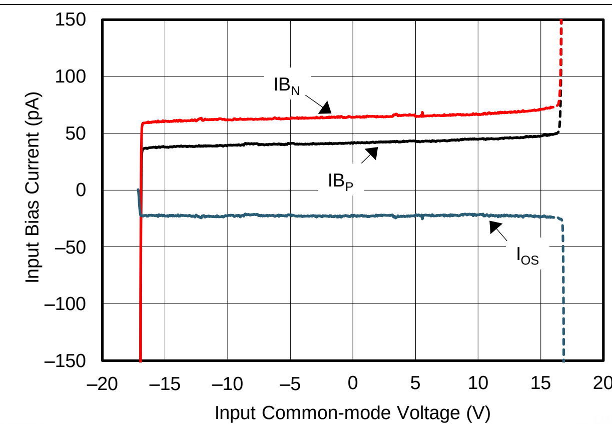


Figure 6. I_B and I_{OS} vs Common Mode Voltage

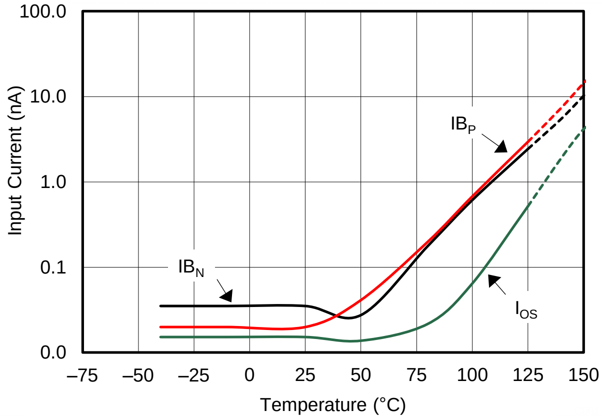


Figure 7. Input Bias Current vs Temperature

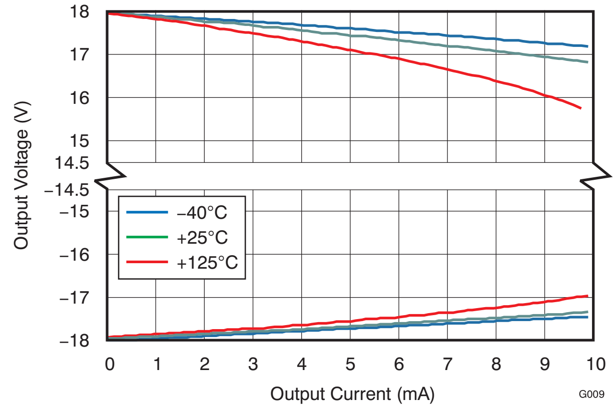


Figure 8. Output Voltage Swing vs Output Current (Maximum Supply)

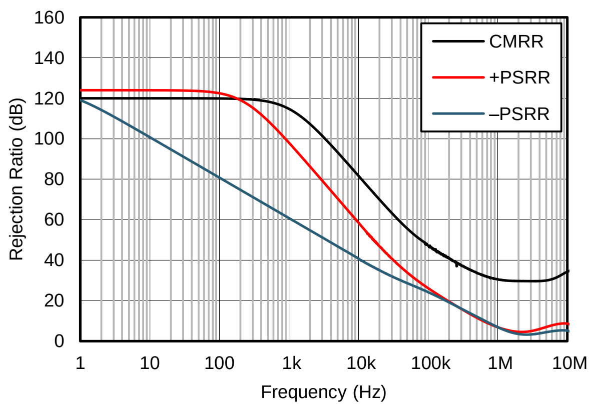


Figure 9. CMRR and PSRR vs Frequency

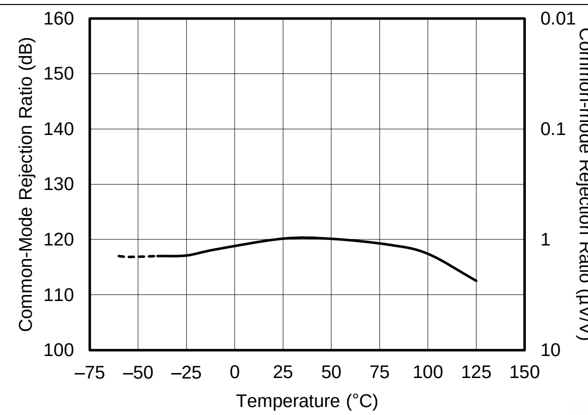


Figure 10. CMRR vs Temperature

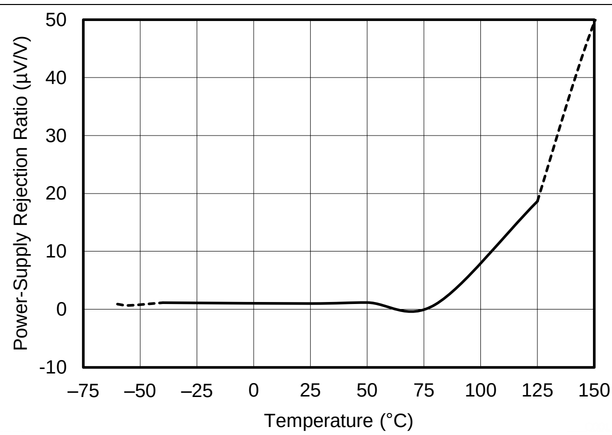


Figure 11. PSRR vs Temperature

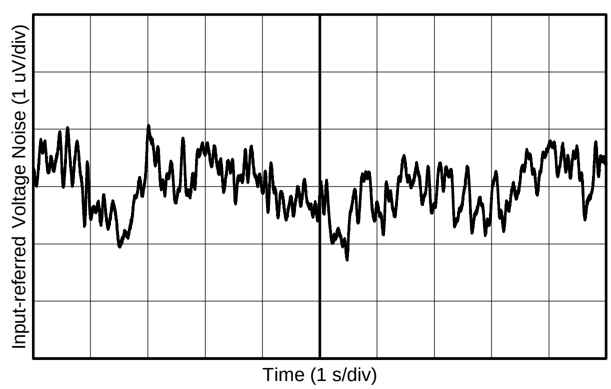


Figure 12. 0.1-Hz to 10-Hz Noise

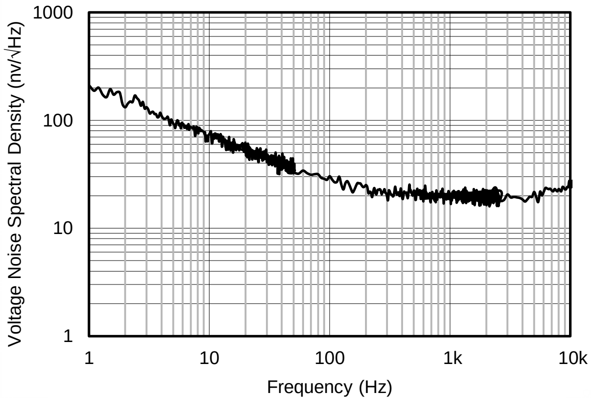


Figure 13. Input Voltage Noise Spectral Density vs Frequency

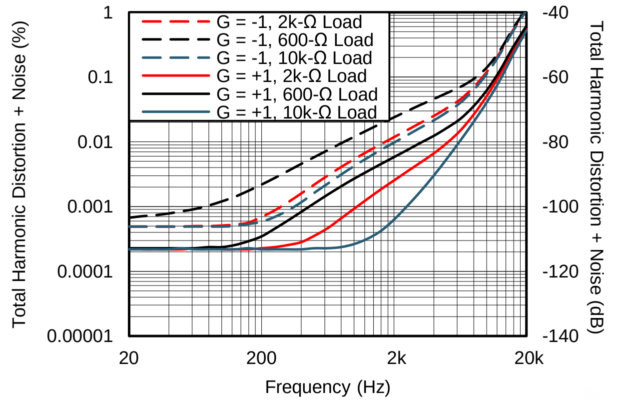


Figure 14. THD + N Ratio vs Frequency

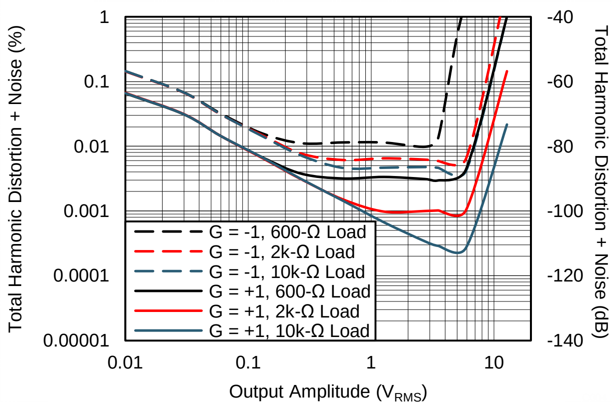


Figure 15. THD + N vs Output Amplitude

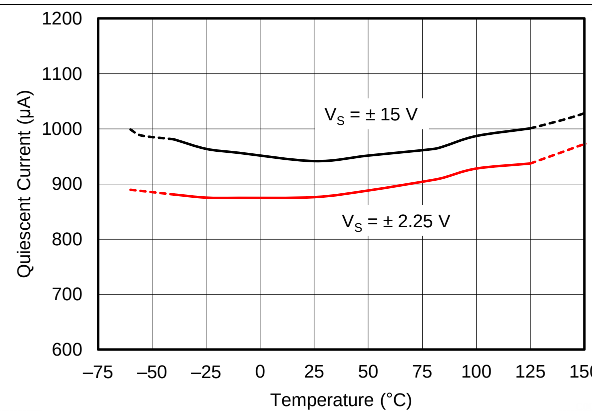


Figure 16. Quiescent Current vs Temperature

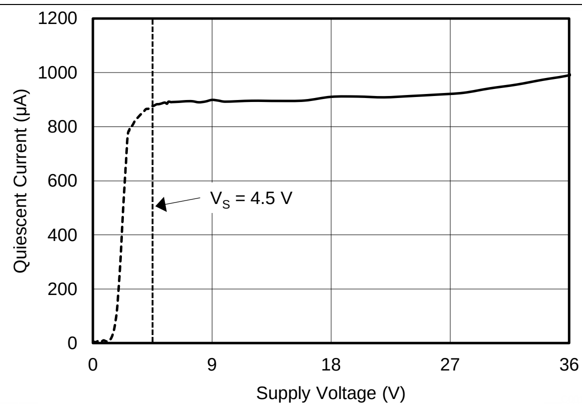


Figure 17. Quiescent Current vs Supply Voltage

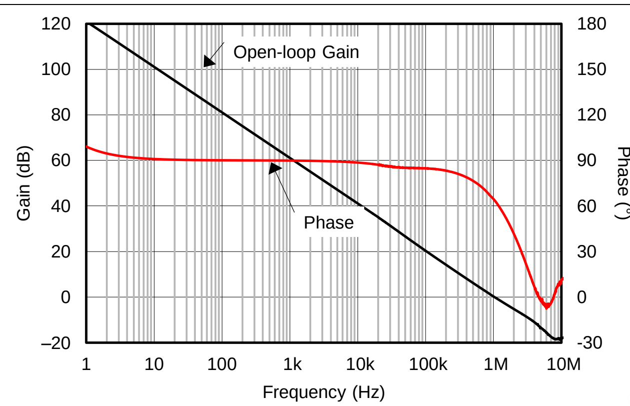


Figure 18. Open-Loop Gain and Phase vs Frequency

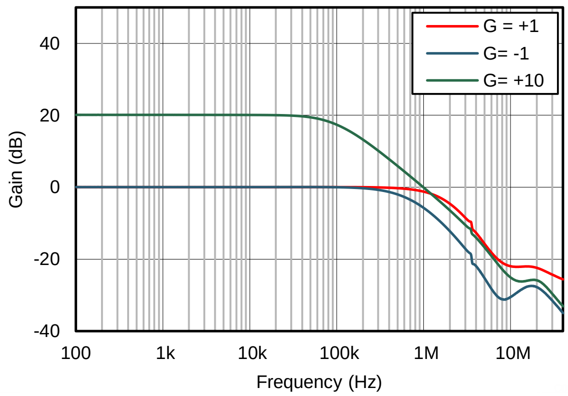


Figure 19. Closed-Loop Gain vs Frequency

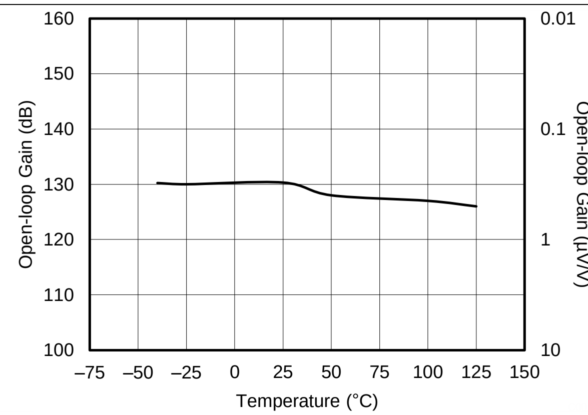


Figure 20. Open-Loop Gain vs Temperature

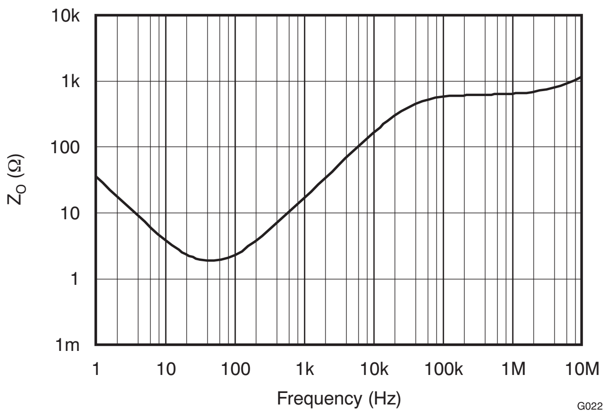


Figure 21. Open-Loop Output Impedance vs Frequency

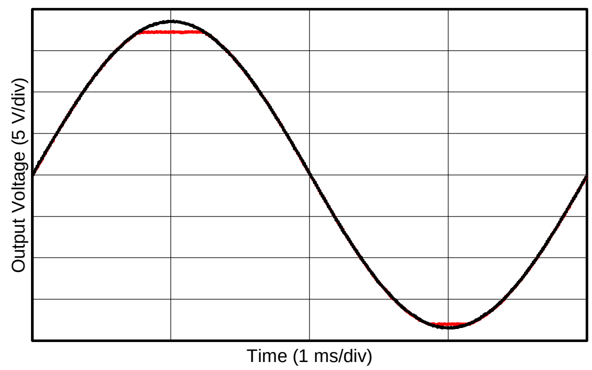


Figure 22. No Phase Reversal

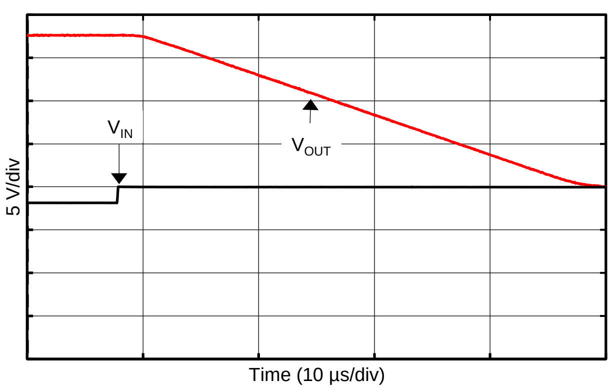


Figure 23. Positive Overload Recovery

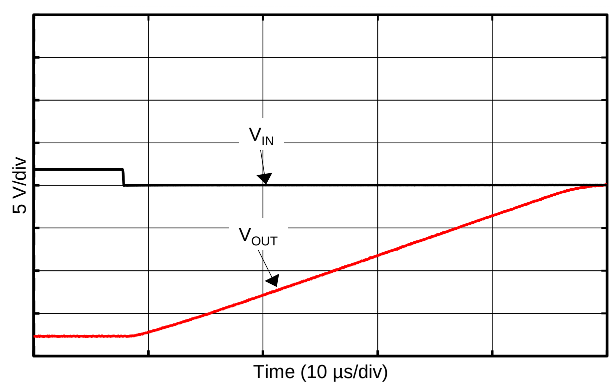
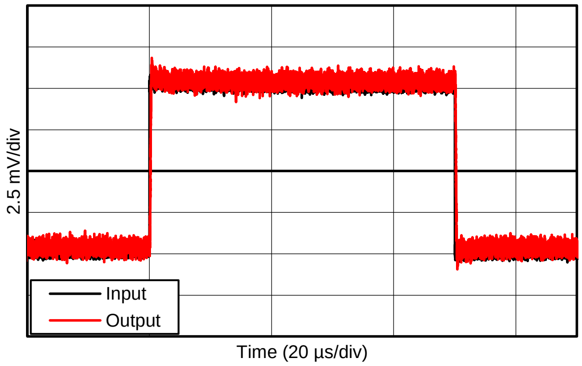
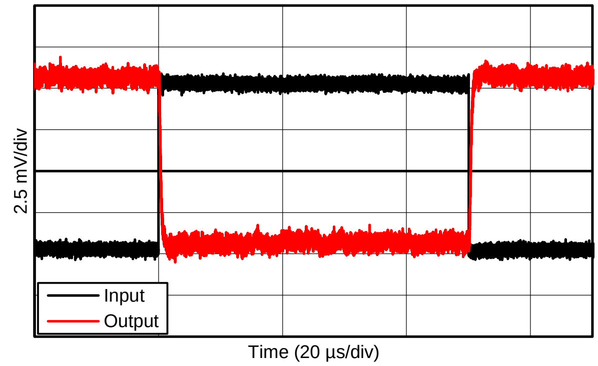


Figure 24. Negative Overload Recovery



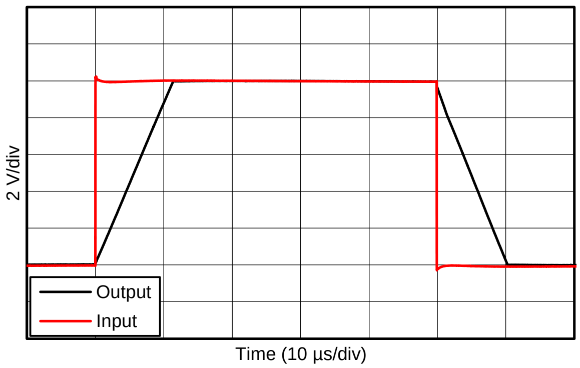
G = +1 V/V

Figure 25. Small-Signal Step Response



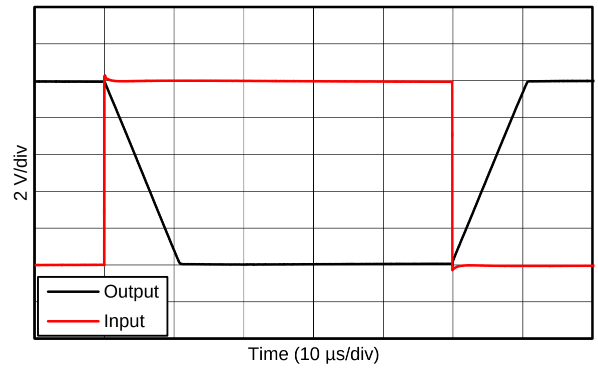
G = –1 V/V

Figure 26. Small-Signal Step Response



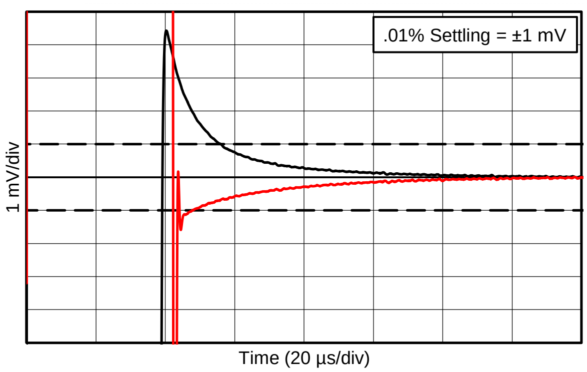
G = +1 V/V

Figure 27. Large-Signal Step Response



G = –1 V/V

Figure 28. Large-Signal Step Response



10-V positive step

Figure 29. Large-Signal Settling Time

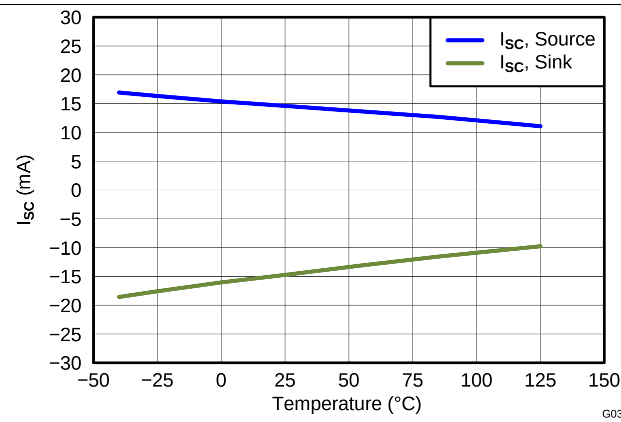


Figure 30. Short-Circuit Current vs Temperature

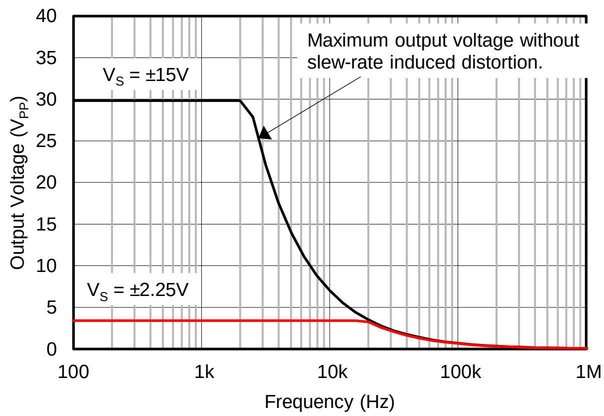


Figure 31. Maximum Output Voltage vs Frequency

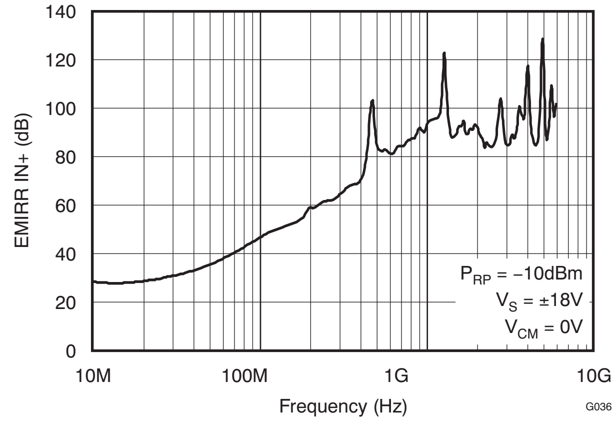


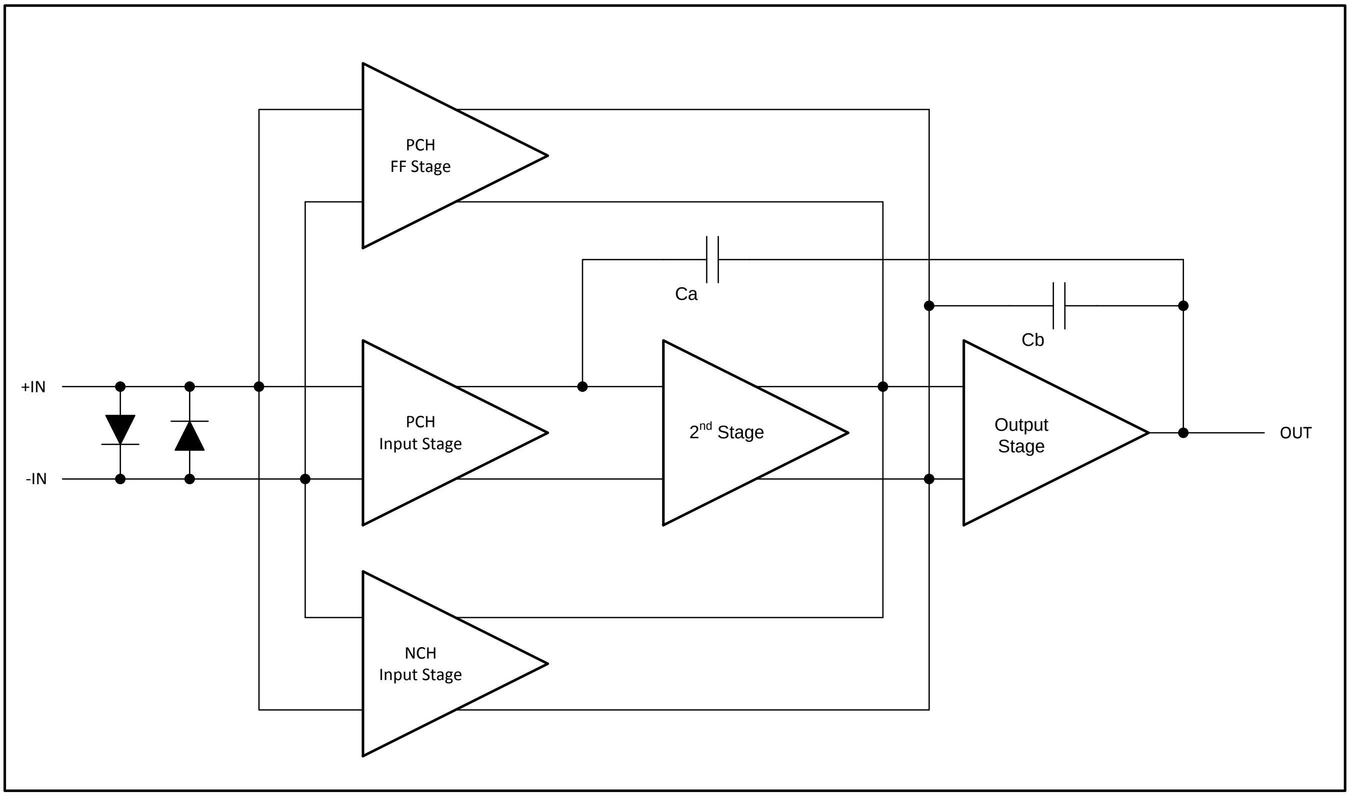
Figure 32. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The TLV07 operational amplifier provides high overall performance, making the device suitable for many general-purpose applications. The excellent offset drift of only 0.9 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The TLV07 op amp is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in *Typical Characteristics*.

7.3.2 Phase-Reversal Protection

The TLV07 has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input drives beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input drives beyond the specified common-mode voltage range, which causes the output to reverse into the opposite rail. The input of the TLV07 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 33.

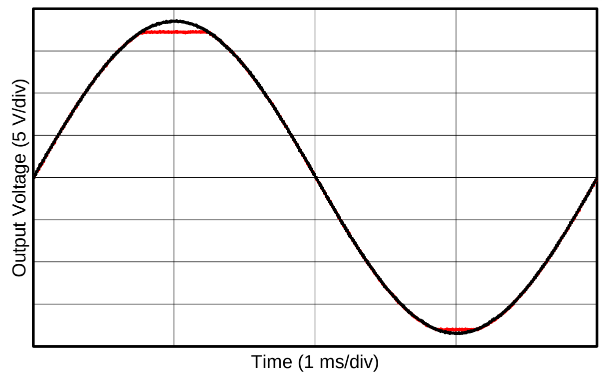


Figure 33. No Phase Reversal

7.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. The questions typically focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Internal electrostatic discharge (ESD) protection is built into the circuits to protect the circuits from accidental ESD events before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance of the circuitry to an electrical overstress event is helpful. Figure 34 shows the ESD circuits contained in the TLV07 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at the power-supply ESD cell, an absorption device, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)

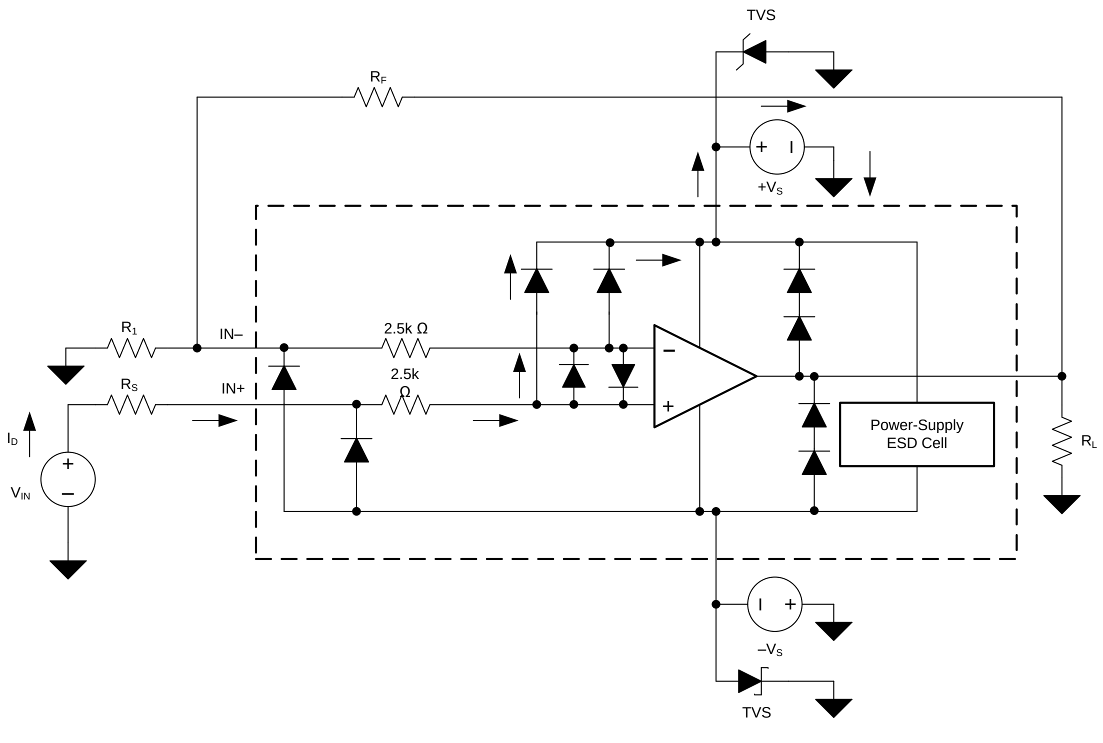


Figure 34. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLV07, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see Figure 34), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 34 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} sources current to the operational amplifier and becomes the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. This question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see Figure 34. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The TLV07 input pins are protected from excessive differential voltage with back-to-back diodes; see Figure 34. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, use an input series resistor to limit the input signal current.

7.4 Device Functional Modes

7.4.1 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices must have time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. As a result, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV07 is approximately 2 µs.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV07 op amp provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Follow the additional recommendations in *Layout Guidelines* to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier, potentially causing instability. Add an isolation resistor between the amplifier output and the capacitive load to stabilize the amplifier. *Typical Application* shows the design process for selecting this resistor.

8.2 Typical Application

This circuit can drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

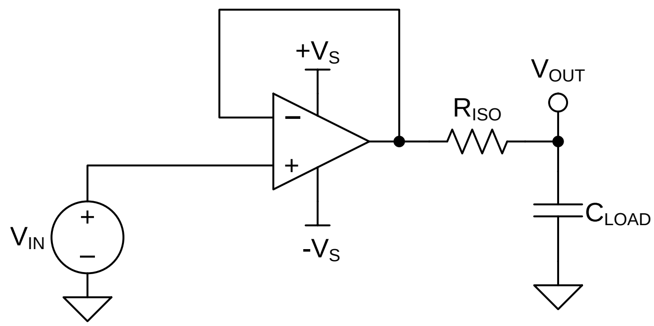


Figure 35. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

Figure 35 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 35. Figure 35 does not show the open-loop output resistance of the op amp (R_O).

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function shown in Equation 1 has a pole and a zero. ($R_O + R_{ISO}$) and C_{LOAD} determine the frequency of the pole (f_p). The R_{ISO} and C_{LOAD} components determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and $1/\beta$ is 20 dB/decade.

Typical Application (continued)

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_O. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. These measurements then calculate phase margin. Table 2 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLV07, see *Capacitive Load Drive Solution Using an Isolation Resistor*

Table 2. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

The values of R_{ISO} that yield phase margins of 45° and 60° for various capacitive loads are determined using the described methodology Figure 36 shows the results.

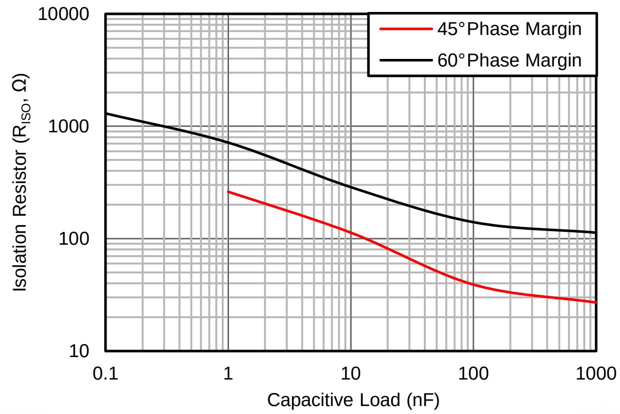


Figure 36. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

9 Power Supply Recommendations

The TLV07 is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 38, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

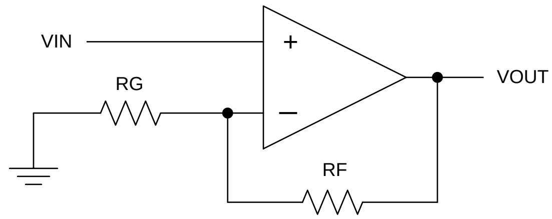


Figure 37. Schematic Representation of a Non-inverting Amplifier

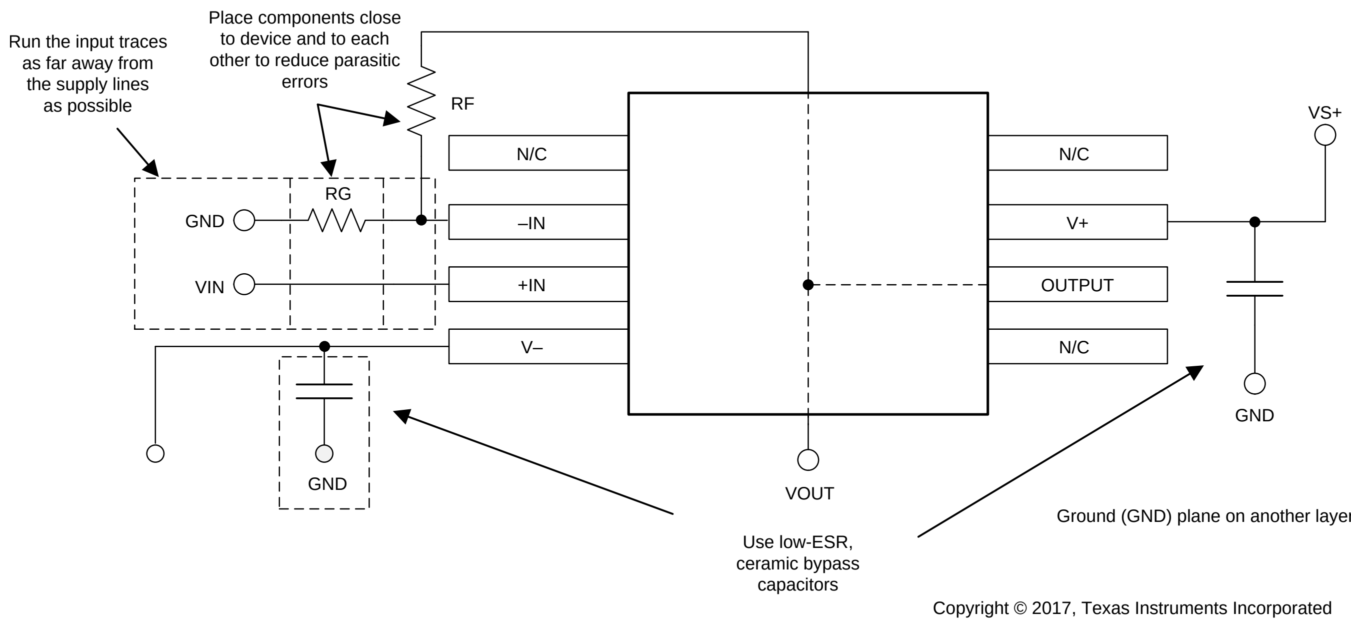


Figure 38. Operational Amplifier Board Layout for a Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.2.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount devices. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.2.3 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.2.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

Device Support (continued)

11.1.2.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following (available for download from www.ti.com) :

- *Feedback Plots Define Op Amp AC Performance*
- *Capacitive Load Drive Solution Using an Isolation Resistor*

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV07IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV07	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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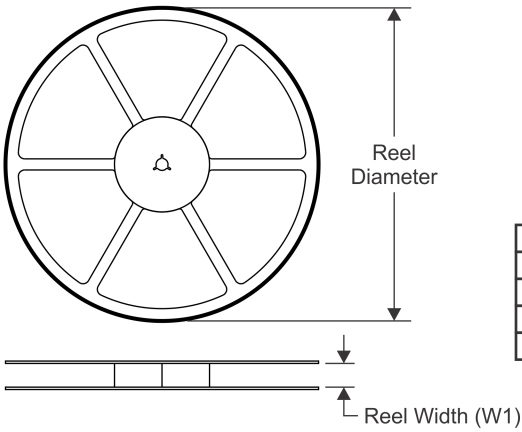
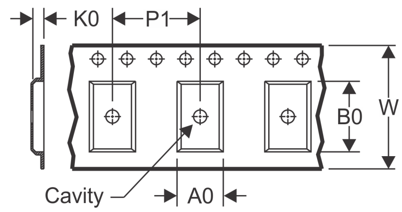
TAPE AND REEL INFORMATION

REEL DIMENSIONS

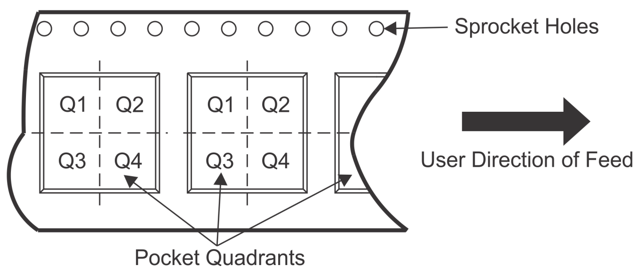


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

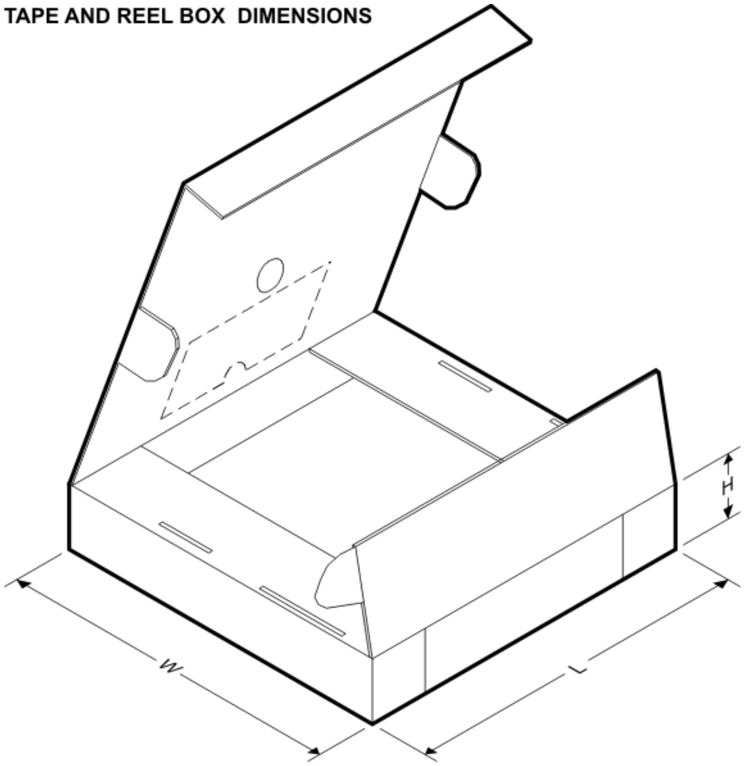
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV07IDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLV07IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

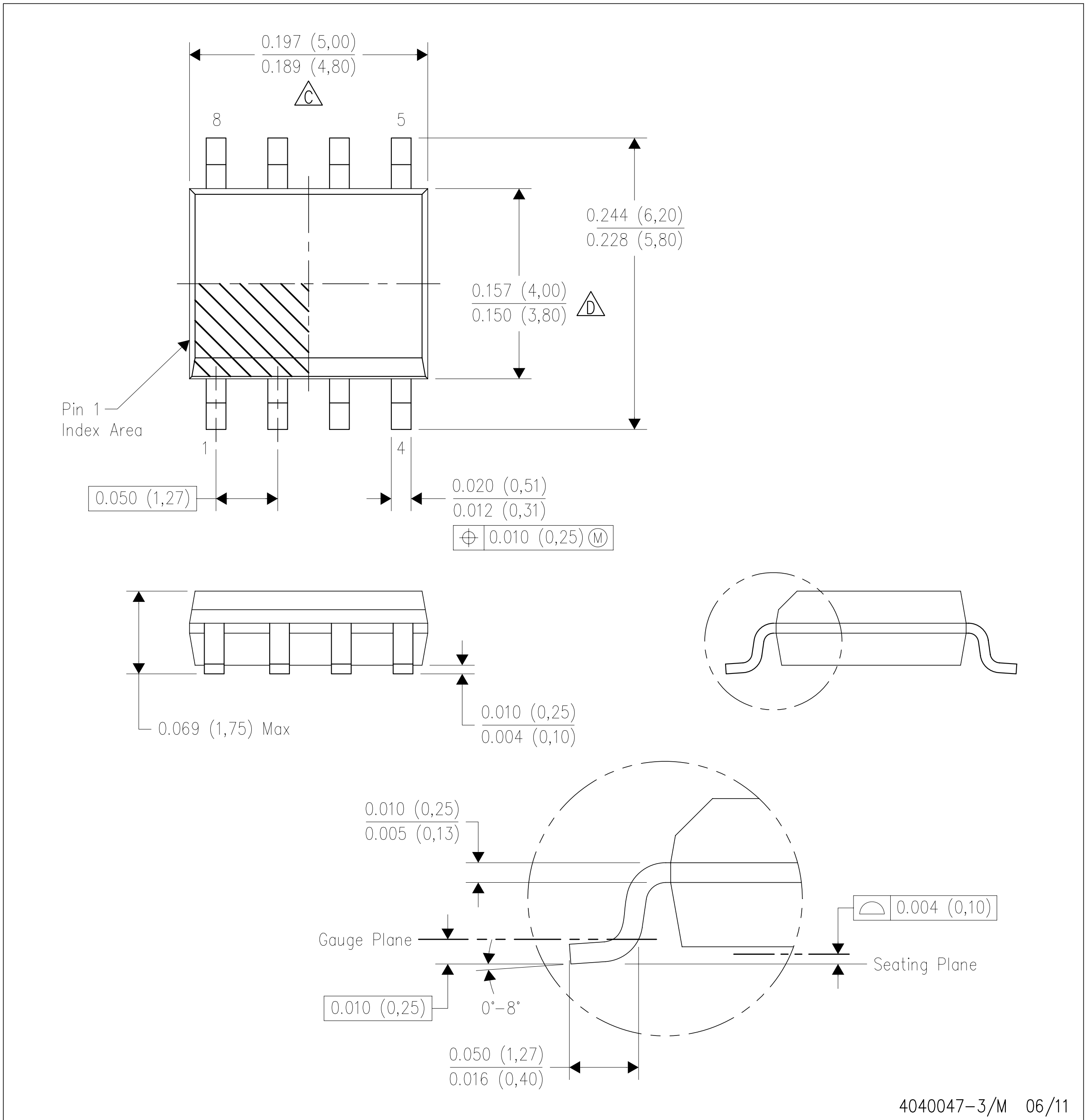
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

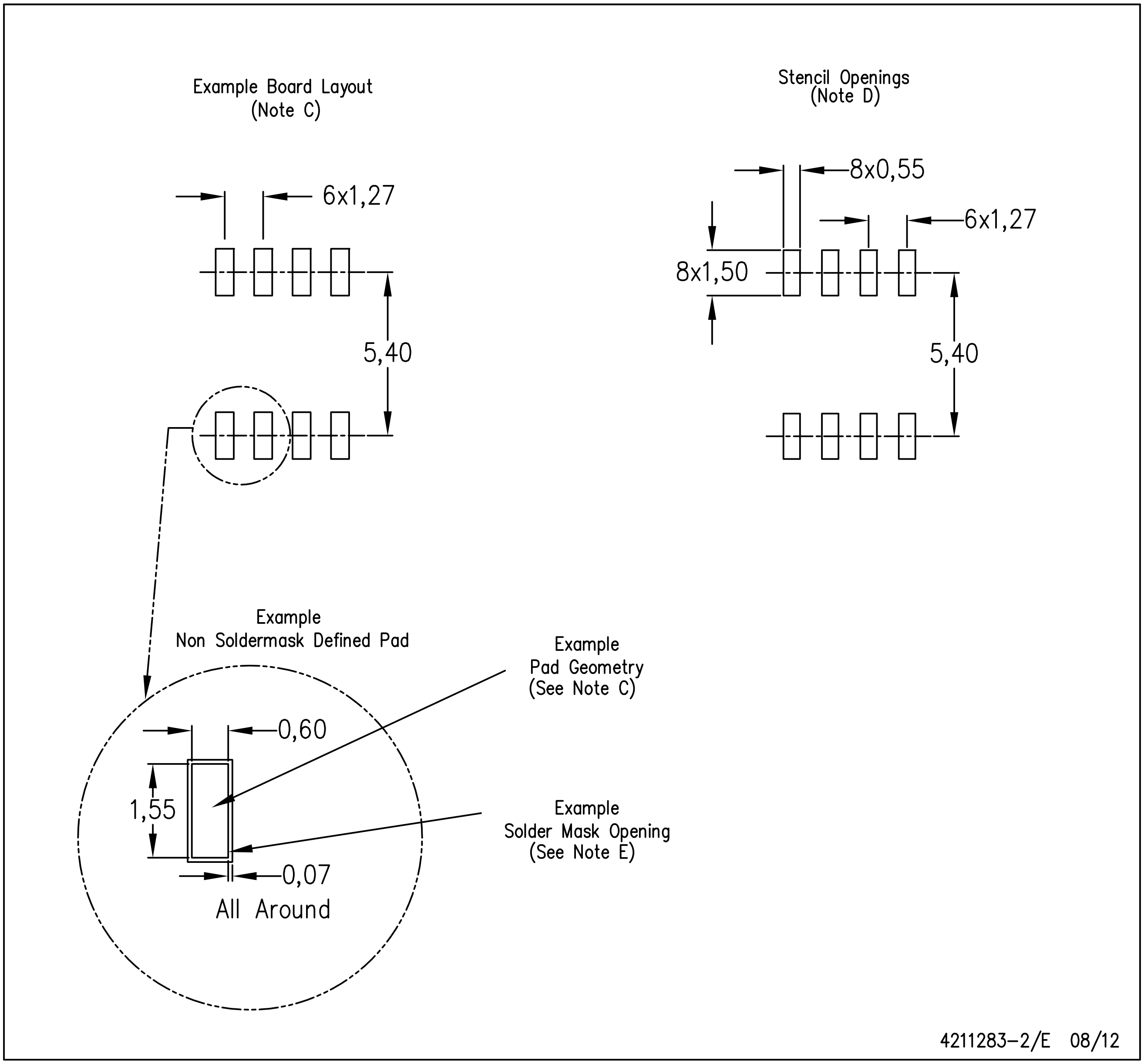
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV07IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV07IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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