AV2026

AV2026 Digital Satellite Tuner

Single Chip Tuner for DVB-S/ ABS-S Receiver

Datasheet

VERSION 0.20 18-Jul-11

Revision History

Version	Change Summary	Page	Date
0.10	Created		02-Nov-10
0.20	RFIN- Description	7,8	18-Jul-11

INDEX

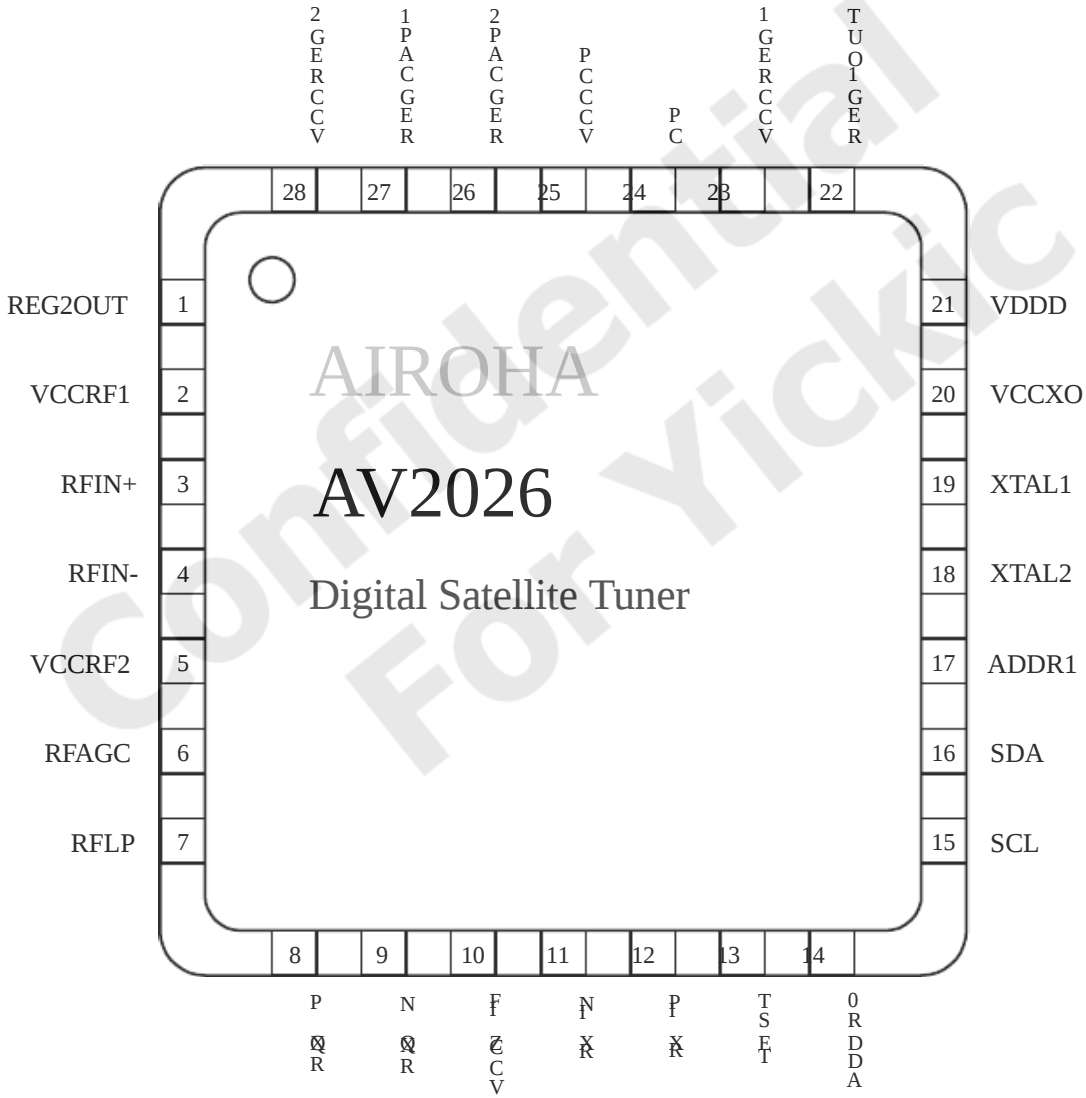
1 Features

- Input RF Frequency: 850MHz to 2300MHz
- Single +3.3V Power Supply
- Embedded LNA, Mixer, VCO, crystal oscillator and LDO regulators
- Embedded DC offset Cancel Circuit
- No Calibration Required
- Programmable channel filter with bandwidth from 4MHz to 40MHz
- Embedded RF signal loop through path
- 2-wire serial control interface
- QFN4*4mm 28pin package

2 Description

AV2026 is a highly integrated single chip for DVB-S/ABS-S Tuner receiver application. The input RF signal frequency ranges from 850MHz to 2300MHz. AV2026 implements zero-IF direct conversion architecture with embedded LNA, Mixer, VCO, crystal oscillator and LDO regulators to minimize the external BOM cost. There is no additional calibration procedure required in AV2026 during power-on procedures. A programmable baseband channel filter is also implemented to provide different channel bandwidths from 4MHz to 40MHz. A 27MHz reference clock with on-chip buffer is also provided for the baseband section clock source. A simple 2-wire interface allows easy control from the baseband controller.

3 Pin Assignment

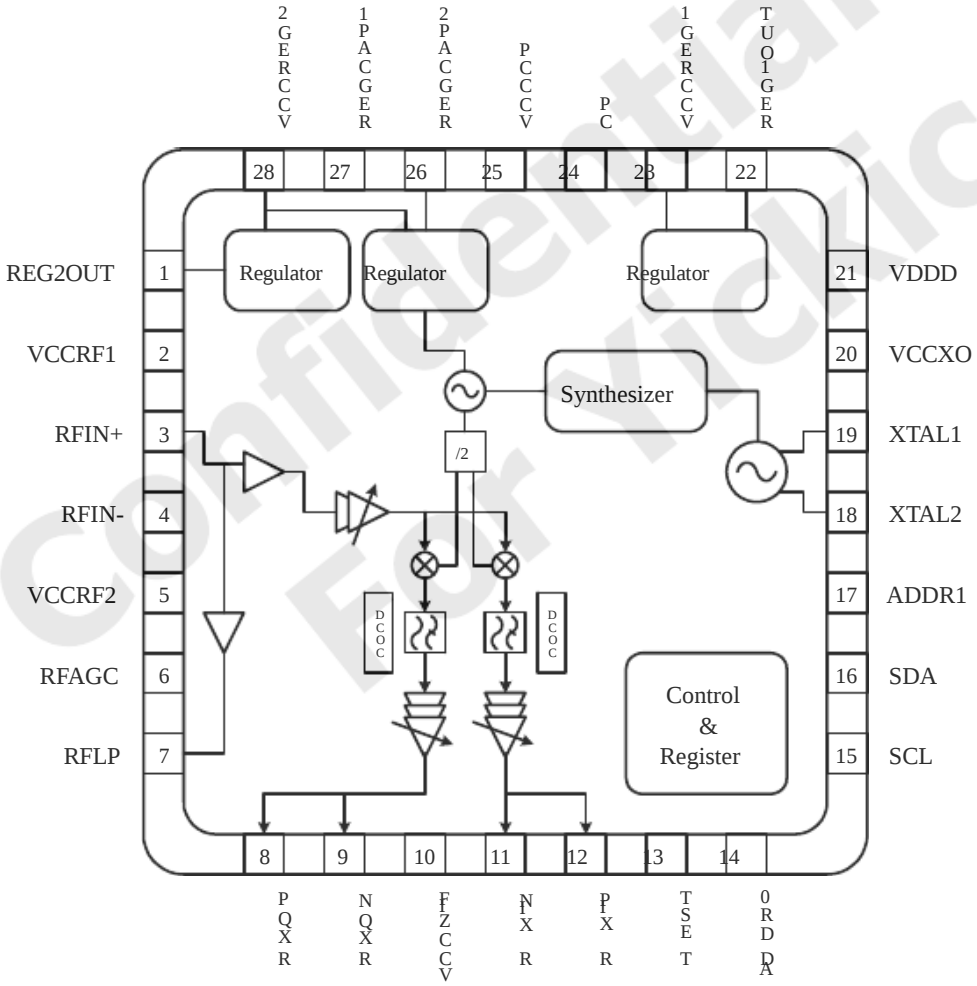


4 Pin Name Description

PIN	SIGANL	TYPE	DESCRIPTION
1	REG2OUT	Regulator Output	RFVCC Regulator Output
2	VCCRF1	VCC Supply	RFVCC Supply Voltage for RF Circuits
3	RFIN+	Input, Analog	RF Signal Input
4	RFIN-	Analog	LNA virtual ground
5	VCCRF2	VCC Supply	RFVCC Supply Voltage for RF Circuits
6	RFAGC	Input, Analog Control	RF AGC Control Voltage
7	RFLP	Output, Analog	RF Loop Through Signal Output
8	RXQP	Output, Differential Analog	BB Output
9	RXQN	Output, Differential Analog	BB Output
10	VCCZIF	VCC Supply	RFVCC Supply Voltage for ZIF Circuits
11	RXIN	Output, Differential Analog	BB Output
12	RXIP	Output, Differential Analog	BB Output
13	TEST	Input, Digital Control	Should be connected to ground
14	ADDR0	Digital	Device Address Control
15	SCL	Input, Digital	Serial Interface
16	SDA	Input/Output, Digital	Serial Interface
17	ADDR1	Digital	Device Address Control
18	XTAL2	Analog	XTAL Input
19	XTAL1	Analog	XTAL Input
20	VCCXO	VCC Supply	DIGVCC Supply Voltage for XO Circuits
21	VDDD	VCC Supply	DIGVCC Supply Voltage for Digital Circuits
22	REG1OUT	Regulator Output	DIGVCC Regulator Output
23	VCCREG1	VCC Supply	3.3V Supply Voltage for Regulator
24	CP	Analog	Charge Pump
25	VCCCP	VCC Supply	RFVCC Supply Voltage for CP Circuits
26	REGCAP2	Analog	Regulator Output for External Capacitor
27	REGCAP1	Analog	Regulator Output for External Capacitor
28	VCCREG2	VCC Supply	3.3V Supply Voltage for Regulator

5 Block Diagram and Description

5.1 General Description



AV2026 is a single chip IC for DVB-S/ABS-S Tuner receiver application. There are three main sections within AV2026, i.e. the Receiver section, the synthesizer/PLL/VCO section and the control section. Embedded LDO regulators are also integrated in AV2026 such that only a single 3.3volt VCC supply is needed.

5.2 Receiver Section

The Receiver section comprises a LNA and RF variable gain amplifiers, a Zero-IF mixer, a programmable channel filter and a VGA. The RF signal is directly down-converted to baseband signals, filtered by the channel filter and amplified by the VGA and then output to RXIQ output pins. An internal DC offset cancellation mechanism is implemented to reject DC offset at RXIQ output signals.

A loop-through path is also provided in AV2026. The input RF signal can be re-transmitted to another receiver box through this path. A buffer amplifier is used to keep the RF signal unchanged to the next receiver. This path can be enabled/disabled independently.

5.3 Synthesizer/VCO/XO Section

A fractional-N frequency synthesizer architecture is implemented in AV2026. The input RF frequency ranges from 850MHz to 2300MHz. An on-chip VCO with embedded loop filter is also included in AV2026. A crystal oscillator is provided in AV2026 and only an external crystal is needed. The generated 27MHz reference clock signal can be output to baseband processor.

5.4 Control Section

A 2-wire control interface is implemented in AV2026. Detailed timing diagram and read/write procedures of the 2-wire interface are described in chapter 6. A 7-bit device address plus read/write bit is required for this 2-wire interface. There are four device addresses available in AV2026 in each read and write mode, selected by external pins ADDR0/ADDR1, as listed in table 5.1 and table 5.2. The level of ADDR1/0 would be “High” if it kept open or NC, and would be “Low” if connected to GND directly.

ADDR1	ADDR0	7-bit Address							R/W bit	Read Address (in Hex)
		MSB						LSB		
Low	Low	1	1	0	0	0	0	0	1	0xC1
Low	High	1	1	0	0	0	0	1	1	0xC3
High	Low	1	1	0	0	0	1	0	1	0xC5
High	High	1	1	0	0	0	1	1	1	0xC7

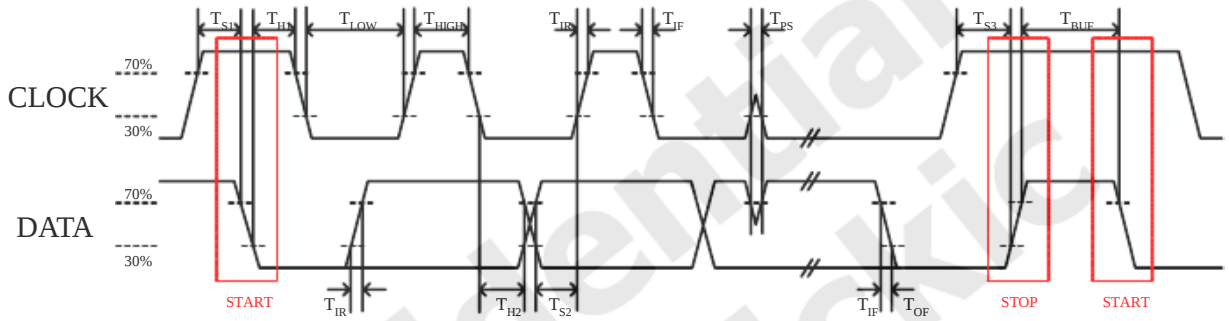
Table 5.1: Read Address

ADDR1	ADDR0	7-bit Address							R/W bit	Write Address (in Hex)
		MSB						LSB		
Low	Low	1	1	0	0	0	0	0	0	0xC0
Low	High	1	1	0	0	0	0	1	0	0xC2
High	Low	1	1	0	0	0	1	0	0	0xC4
High	High	1	1	0	0	0	1	1	0	0xC6

Table 5.2: Write Address

6 2-wire Serial Interface

6.1 Read/write Timing Parameters



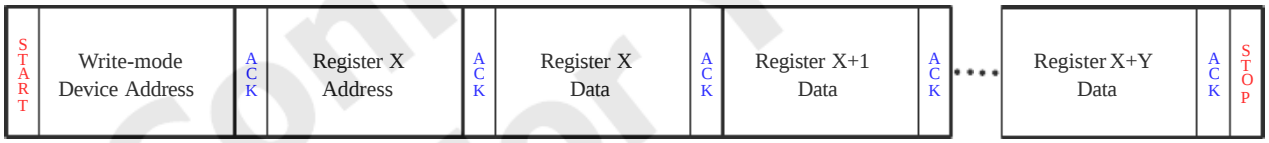
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		400	KHz
T_{S1}	CLOCK Input to DATA N-edge Setup time (START)	600			ns
T_{H1}	CLOCK Input to DATA N-edge Hold time (START)	600			ns
T_{S2}	DATA Input to CLOCK P-edge Setup time	100			ns
T_{H2}	DATA Input to CLOCK N-edge Hold time	0		900	ns
T_{S3}	CLOCK Input to DATA P-edge Setup time (STOP)	600			ns
T_{BUF}	STOP to START time	1300			ns
T_{OF}	DATA Output Fall time	20		250	ns
T_{IR}	DATA Input & CLOCK Rise time	20		300	ns
T_{IF}	DATA Input & CLOCK Fall time	20		300	ns
T_{HIGH}	CLOCK HIGH duration	600			ns
T_{LOW}	CLOCK LOW duration	1300			ns
T_{PS}	Input Filter Pulse Suppression			50	ns

6.2 Read/write Procedures

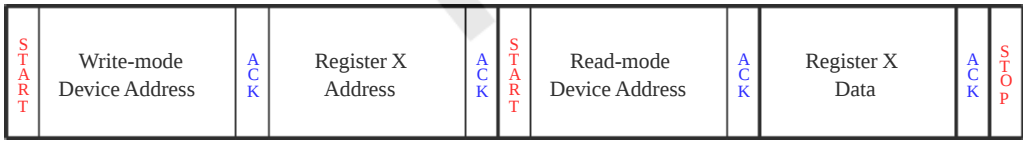
AV2026 allows single register read/write and multiple registers write sequentially through the 2-wire interface. The procedures are described as follows. In each R/W process a read or write device address is first transmitted, then followed by the register address and data content. There are four device addresses available in AV2026 for read/write mode, and is selected by external pins ADDR0/ADDR1 as described in Sec 5.4.

Single Write Procedure

Sequential Write Procedure



Single Read Procedure



7 Electrical Characteristics

7.1 Absolute Maximum Ratings

AV2026 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (VCCREG1/2)	– 0.3V	5.5V
Pin voltage	– 0.3V	HOST_IO_VCC + 0.3V
Maximum power dissipation	-	0.5W
Operating temperature	– 20 ° C	+85 ° C
Storage temperature	– 65 ° C	+150 ° C
LNA input level	-	+10 dBm
Digital pin	-	+5mA
RFAGC pin	-	+5mA

*Connect current limit resistor at Digital pin, RFAGC pin.

7.2 DC Electrical Specifications

Typical values are measured at VCCREG=3.3V, Ta=25 °C on Airoha AV2026 evaluation board unless the items specified in the notes of the table.

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VCCREG		2.97	3.3	3.63	V
Power Supply Current (RF Loop Through path disabled)				130	140	mA
Power Supply Current (RF Loop Through path enabled)				140	150	mA
Digital Input Voltage – High Level	V_{IH}		0.7*VCCREG		VCCREG+0.3	V
Digital Input Voltage – Low Level	V_{IL}		- 0.3		0.3*VCCREG	V
Interface Output Voltage – High Level	V_{OH}	I_{OUT} = 500µA	0.8*VCCREG			V
Interface Output Voltage – Low Level	V_{OL}	I_{OUT} = - 500µA			0.2*VCCREG	V

7.3 AC Electrical Specification

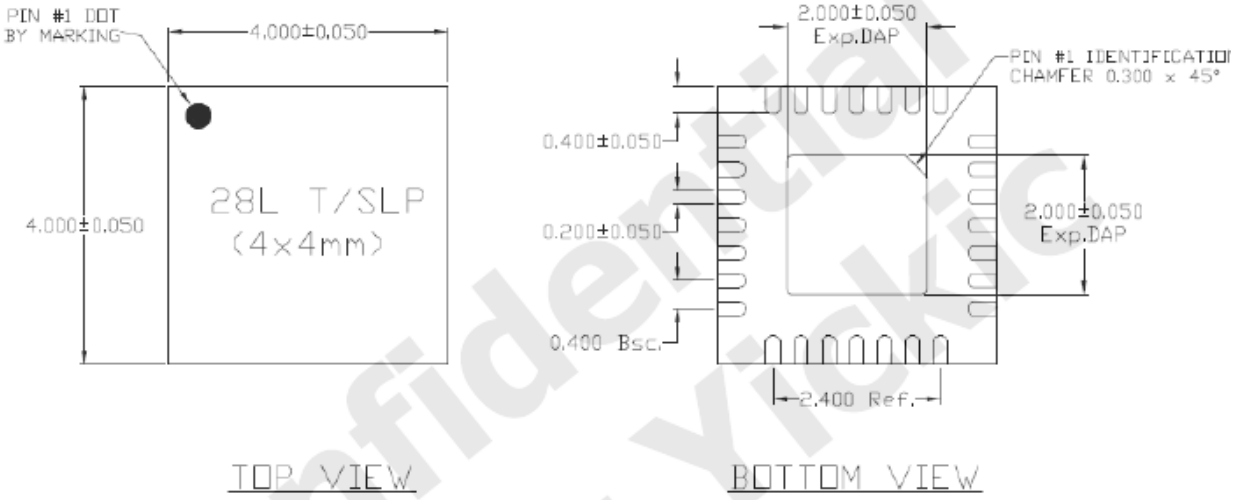
Typical values are measured at VCCREG=3.3V, Ta=25 °C on Airoha AV2026 evaluation board unless the items specified in the notes of the table.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver Section					
RF Front-End Input					
Input frequency range		850		2300	MHz
RF gain control range	Controlled by RFAGC pin	-10		+70	dB
Noise Figure	Max Gain		5		dB
RFAGC control voltage range		0.5		2.8	V
Baseband gain control range	Controlled by register		12		dB
Baseband gain control step			1.5		dB/step
IIP3	-25dBm RF input		2		dBm
IIP2	-25dBm RF input		10		dBm
Adjacent Channel Rejection			23		dB
LO product leakage at RFIN			-80		dBm
2LO-RF rejection	-45dBm RF Input	35	50		dBc
2RF-LO rejection	-45dBm RF Input		50		dBc
Baseband Output					
Normal output swing			0.5		Vpp
I/Q Amplitude imbalance			1		dB
I/Q Quadrature phase imbalance	@ 1.5MHz		3		deg
I/Q output impedance				50	Ohm
High pass –3dB frequency			500	1200	Hz
Channel filter -3dB Bandwidth		4		40	MHz
Channel filter Rejection Ratio	> 2x F_{-3dB}		40		dB
Channel filter BW accuracy	> 8MHz		+/- 5		%
	< 8MHz		+/- 0.5		MHz
RF Loop Through Path					
Output return loss	850-2300 MHz		10		dB
Gain		0	1.5	4.5	dB
Noise Figure			10		dB
OIP3			5		dBm
OIP2			10		dBm
Reverse Isolation			30		dBc

Synthesizer/VCO/XO Section					
Ref divider frequency range			27		MHz
LO integrated phase jitter	10kHz to 20MHz		2	3	Degree
Locking time			1	4	ms
Xtal buffer output swing			600		mVpp
Xtal buffer output duty cycle		40	50	60	%

8 Package Dimension

Package: Punch type QFN 4x4x0.9mm, 0.4mm pitch, 28 pins



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800