

HD74LS283 • 4-bit Binary Full Adders

The HD74LS283 adder is electrically and functionally identical to the HD74LS83A, respectively; only the arrangement of the terminals has been changed.

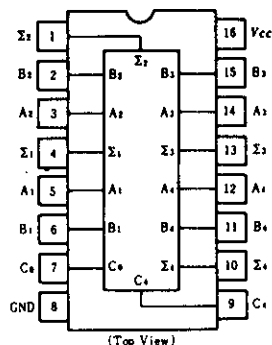
This improved full adder performs the addition of two 4-bit binary words.

The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. This adder features full internal look-ahead across all four bits generating the carry term in then nanoseconds.

The adder logic, including the carry, is implemented in its true form.

End around carry can be accomplished without the need for logic or level inversion.

PIN ARRANGEMENT



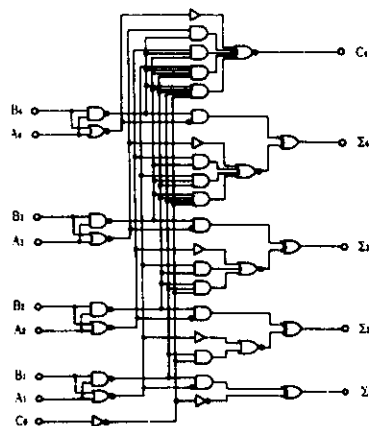
FUNCTION TABLE

Inputs				Outputs						
				When $C_0=L$		When $C_1=L$		When $C_2=H$		When $C_3=H$
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_1	C_2	
A_3	B_3	A_4	B_4	Σ_3	Σ_4	C_4	Σ_2	Σ_4	C_4	
L	L	L	L	L	L	L	H	L	L	
H	L	L	L	H	L	L	L	H	L	
L	H	L	L	H	L	L	L	H	L	
H	H	L	L	L	H	L	H	H	L	
L	L	H	L	L	H	L	H	H	L	
H	L	H	L	H	H	L	L	L	H	
L	H	H	L	H	H	L	L	L	H	
H	H	H	L	L	L	H	H	L	H	
L	L	L	H	L	H	L	H	H	L	
H	L	L	H	H	H	L	L	L	H	
L	H	L	H	H	H	L	L	L	H	
H	H	L	H	L	L	H	H	L	H	
L	L	H	H	L	L	H	H	L	H	
H	L	H	H	H	L	H	L	H	H	
L	H	H	H	H	L	H	L	H	H	
H	H	H	H	L	H	H	H	H	H	

H; high level, L; low level

Notes) Input conditions at A_1 , B_1 , A_2 , B_2 , and C_0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2 . The values at C_2 , A_3 , B_3 , A_4 , and B_4 are then used to determine outputs Σ_3 , Σ_4 , and C_4 .

BLOCK DIAGRAM



HD74LS283

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output voltage	V_{OH}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	—	—	V	
	V_{OL}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$	$I_{OL} = 4\text{mA}$	—	—	0.4	V
			$I_{OL} = 8\text{mA}$	—	—	0.5	V
Input current	except C_0	I_{IH}	$V_{CC} = 5.25\text{V}$, $V_i = 2.7\text{V}$	—	—	40	μA
				C_0	—	—	
	except C_0	I_{IL}	$V_{CC} = 5.25\text{V}$, $V_i = 0.4\text{V}$	—	—	-0.8	mA
				C_0	—	—	
	except C_0	I_i	$V_{CC} = 5.25\text{V}$, $V_i = 7\text{V}$	—	—	0.2	mA
C_0				—	—	0.1	
Short-circuit output current	I_{OS}	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA	
Supply current	I_{CC}	$V_{CC} = 5.25\text{V}$	All inputs grounded	—	22	39	mA
			All B low, other inputs at 4.5V	—	19	34	
			All inputs at 4.5V	—	19	34	
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}$, $I_{IK} = -18\text{mA}$	—	—	-1.5	V	

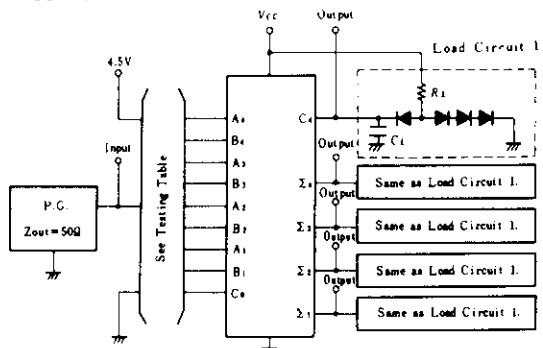
* $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

■ SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	C_0	Σi	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	—	16	24	ns
	t_{PHL}				—	15	24	ns
	t_{PLH}	A_i, B_i	Σi		—	15	24	ns
	t_{PHL}				—	15	24	ns
	t_{PLH}	C_0	C_i		—	11	17	ns
	t_{PHL}				—	11	22	ns
	t_{PLH}	A_i, B_i	C_i		—	11	17	ns
	t_{PHL}				—	12	17	ns

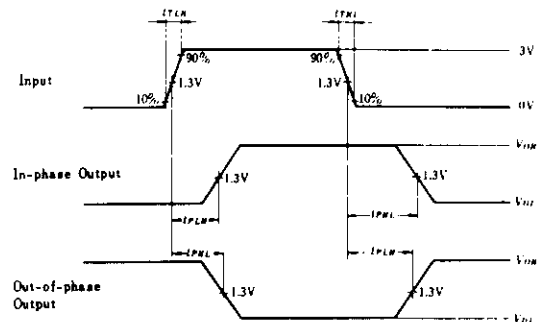
■ TESTING METHOD

1) Test Circuit



- Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

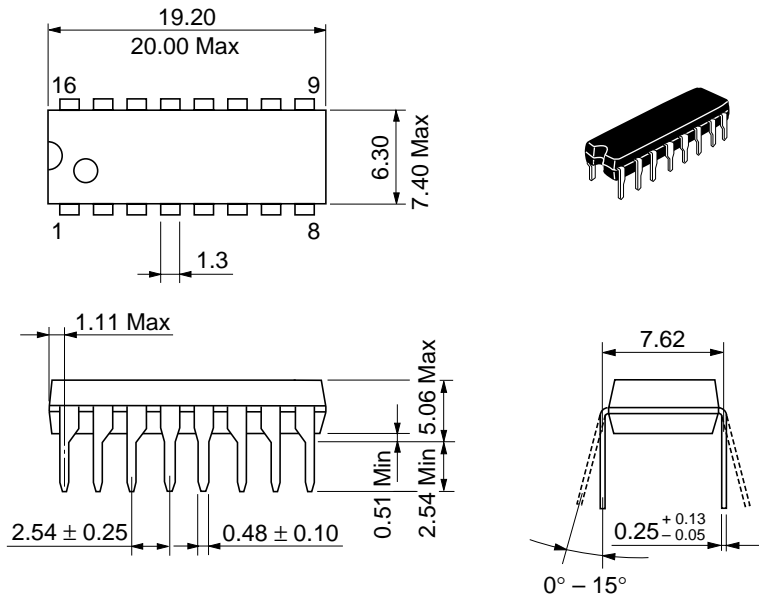
Waveform



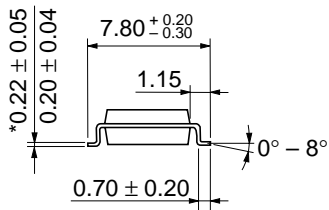
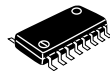
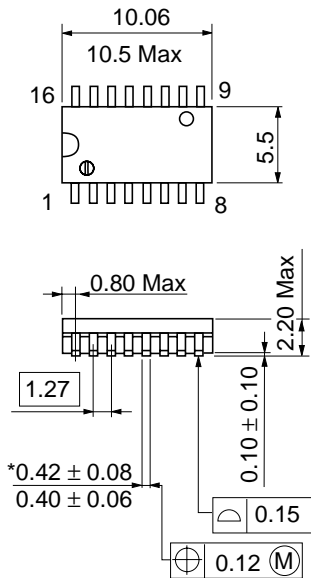
Input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$,
 $PRR = 1\text{MHz}$, duty cycle 50%.

2) Testing Table

Item	From input to output	Inputs									Outputs					
		B ₄	A ₄	B ₃	A ₃	B ₂	A ₂	B ₁	A ₁	C ₀	C ₄	Σ ₄	Σ ₃	Σ ₂	Σ ₁	
	C ₀ → Σ _i or C ₄	GND	GND	GND	GND	GND	GND	GND	GND	IN	—	—	—	—	OUT	
		GND	4.5V	GND	4.5V	GND	4.5V	GND	4.5V	IN	OUT	OUT	OUT	OUT	OUT	
<i>t_{PLH}</i>	Ai or Bi → Σ _i or C ₄	GND	GND	GND	GND	GND	GND	GND	IN	IN	GND	—	—	—	OUT	
		GND	GND	GND	GND	GND	IN	IN	GND	GND	GND	—	—	—	OUT	—
<i>t_{PHL}</i>	Ai or Bi → Σ _i or C ₄	GND	GND	GND	IN	GND	GND	GND	GND	GND	—	—	OUT	—	—	
		GND	IN	GND	GND	GND	GND	GND	GND	GND	—	OUT	—	—	—	
	Ai or Bi → Σ _i or C ₄	GND	GND	GND	GND	GND	GND	4.5V	IN	IN	GND	—	—	—	OUT	OUT
		GND	GND	GND	GND	4.5V	IN	IN	GND	GND	GND	—	—	OUT	OUT	—
	Ai or Bi → Σ _i or C ₄	GND	GND	4.5V	IN	GND	GND	GND	GND	GND	—	OUT	OUT	—	—	
		4.5V	IN	GND	GND	GND	GND	GND	GND	GND	OUT	OUT	—	—	—	

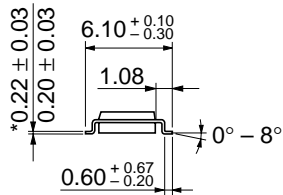
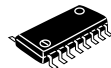
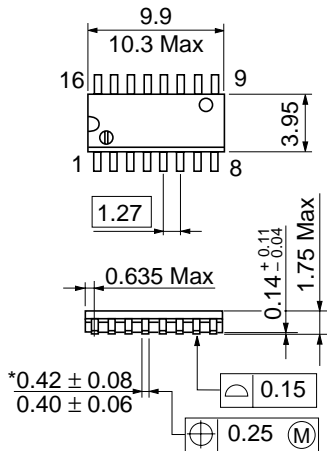


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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