TELEDYNE DALSA
A Teledyne Technologies Company

L I N E S C A N S E N S O R S

Teledyne DALSA IL-P3-B Image Sensors

Fast and sensitive, the IL-P3-B has been designed and fabricated using the industry's most sophisticated technology. The IL-P3-B delivers consistently high image quality, and its single output design reduces the cost and complexity of support electronics.

Features

- Single output, 40 MHz data rate
- Surface gated photodiodes for low lag
- Line rate to 73 kHz (512 model)
- Low voltage clocks (<5V)
- 14 μm (H) x 14 μm (V) pixels, 100% fill factor
- 512, 1024, or 2048 pixels
- Antiblooming and exposure control
- Highly sensitive, with responsivity reaching 43 V/(μJ/cm^2)
- RoHS compliant

Description

Physical Characteristics	IL-P3-B
Pixel dimensions	14 μm x 14 μm
Active area 14μm x	7.2 / 14.4 / 28.7 mm
Active pixels per line	512 / 1024 / 2048
Isolation pixels per line	20
Shielded pixels per line	6

Table 1. IL-P3-B Pin Functional Description

Pin	Symbol	Name
1	VSS	Amplifier Return
2	OS	Output Signal
3	VDD	Amplifier Supply
4, 11	TCK	Transfer Gate
5	PR	Pixel Reset Gate
6, 20	VLS	Light Shield
7, 10, 14	NC	No Connection
8	VPR	Pixel Reset Drain, Guard Ring
9	VSTOR	Pixel Storage Gate
12	VLOW	Low Bias Voltage
13	VHIGH	High Bias Voltage
15, 16	CR2	Readout Register, Phase 2
17, 18	CR1	Readout Register, Phase 1
19	VBB	Substrate
21	CRLAST	Last Register
22	VSET	Output Node Set Gate
23	RST	Output Reset Gate
24	VOD	Output Reset Drain

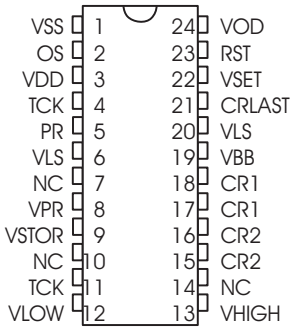


Figure 1. IL-P3-B Block Diagram

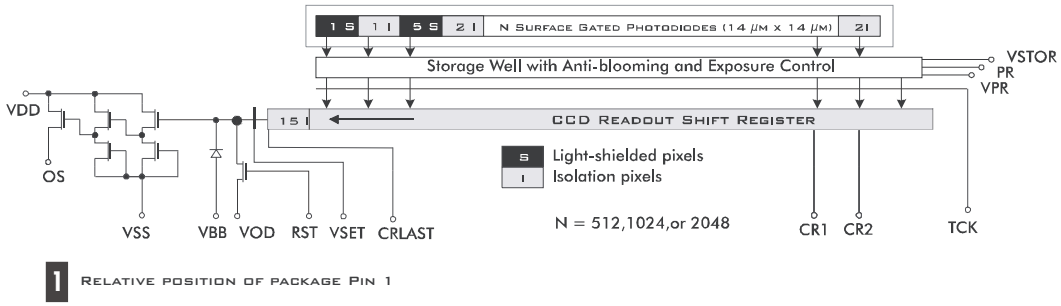


Table 2. # of Clock Drivers Required

Clock Drivers		Min. # Required [1]	
Type	Speed	PR [2] off	PR on
Low Voltage	High	2	2
Low Voltage	Low	1	2
Glitch	High	1	1

1. Redundant clock drivers may be required to drive the CCD input capacitance. Refer to Figure 7 for details.
2. PR = Pixel Reset (exposure control).

Table 3. # of DC Biases Required

DC Biases	# Required [1]	
Regulated?	PR [2] off	PR on
Yes	7	7
No	1	1

1. Refer to Figure 7 for details.
2. PR = Pixel Reset (exposure control).

The IL-P3-B series of linear CCD image sensors use proprietary technology to provide a single output at 40 MHz. The series employs buried channel CCD shift registers to maximize output speed and reduce noise. The sensor has a dynamic range of >1800:1 and provides output which is linear for the operating range of light input. The IL-P3-B's exposure control allows integration times shorter than the readout time. Proprietary image sensor architecture provides low image lag pixels and high blue response.

The IL-P3-B sensor's superior performance makes it ideally suited for applications requiring maximum speed and high resolution, such as:

- High performance document scanning
- Inspection
- Optical character recognition

Functional Description

The IL-P3-B sensor is composed of three main functional groups: surface gated photodiodes in which the signal charge packets are generated, a single CCD readout shift registers, and an output amplifier where the charge packets are converted to voltage pulses.

Detection

The IL-P3-B series includes sensors with 512, 1024, or 2048 pixels with active imaging area lengths of 7, 14, and 28 mm, respectively. Photoelements are 14 μm square for a photosensitive area of 196 μm^2 and a 1:1 aspect ratio. Light incident on these photoelements is converted into charge packets whose size (i.e., number of electrons) is linearly dependent on the light intensity and the integration time. The charge is collected into a separate storage well (VSTOR) adjacent to each photoelement. This helps to minimize image lag, nonuniformities associated with the use of pixel reset, and crosstalk between the photodiode and the CCD shift register.

With exposure control disabled, the integration time is the period between successive pulses of the transfer (TCK) clock. The integration time can be further reduced with electronic exposure control using the pixel reset (PR) clock. The pixel reset clock resets not the photoelements themselves but the storage well adjacent to each photoelement. When PR is clocked, the integration time becomes the duration between the falling edge of the PR clock and the rising edge of the TCK clock.

When PR is clocked, the PR pulse must be damped to produce a smooth PR pulse. If PR switches too rapidly, the uniformity of

the OS signal will be affected by the PR clock feedthrough. A current-drive PR clock circuit generally introduces less feedthrough than a voltage-drive circuit.

Antiblooming is always present when biases fall within the specified operating conditions. By adjusting VSTOR however, the user has the added flexibility of selecting the antiblooming level (the signal level beyond which the additional signal charge is drained away). A higher VSTOR bias results in a higher antiblooming level.

Transfer

The TCK clock controls the transfer of electrons from the storage well into the 2-phase buried-channel CCD readout register. Transfer is from the storage wells into the CR1 phases of the readout register. The readout register is then used to serially shift the charge packets to the high-speed low-noise output amplifier.

The final phase of the readout register is connected separately to CRLAST. This provides the flexibility of timing the transfer of signal charges to the output node. CRLAST is normally clocked in phase with CR1, but may be delayed (see Figure 4) to shift the sampled portion of the output video away from clock feedthroughs.

All CR clocks operate with 50% duty cycle.

Additional details on driving the sensor are provided on Figure 7.

Output

The signal charge packets from the readout shift register are transferred serially from the last readout gate (CRLAST), over the set gate (VSET), to a floating sense node diffusion. The set gate isolates the sense node diffusion from the last readout gate and the rest of the readout shift register. As signal charges accumulate on the floating node diffusion, the potential of this diffusion decreases. The floating node diffusion is connected to the input of a 2.5-stage low-noise amplifier, producing an output signal voltage on the amplifier output (OS). The floating diffusion is cleared of signal charge by the reset gate (RST) in preparation for the next signal charge packet. The voltage level of the floating diffusion after each reset is determined by the output reset drain voltage (VOD). AC coupling the output is recommended to eliminate the DC offset.

The output signal (OS) requires an off-chip load drawing approximately 10mA of load current. If the load capacitance (C_{LOAD}) is greater than 10pF, larger load current (up to the 18mA operating limit) may be required. As the load current increases, the amplifier bandwidth increases. The amplifier can also drive larger capacitive loads when the load current is larger. We recommend however that just enough bandwidth be used since larger bandwidth also results in increased noise.

If an off-chip current load is not available, the amplifier output (OS) can be connected to a 1kΩ load resistor. The use of a passive (resistive) load reduces the amplifier gain, resulting in lower responsivity and saturation output signal. We do not recommend passive loads at data rates greater than 25 MHz because variations in DC offset will result in variations in bandwidth.

The isolation pixels should not be used for calibration or detection.

Table 4. IL-P3-B Absolute Maximum Ratings

Parameter	Unit	Min.	Max.
Storage Temp	°C	-20	80
Operating Temp	°C	-20	60
Voltage on CR1, CR2, VSTOR, TCK, PR, VLS[1] with respect to VBB	V	-10	18
Voltage on OS, VDD, VOD, VSS, VPR, VHIGH, CRLAST, RST, VSET, VLOW with respect to VBB	V	0	18
Voltage on OSn with respect to VSS	V	VDD-8	VDD+1
Amplifier Load Current (I_{LOAD})	mA per output		20

WARNING: Exceeding these values will void product warranty and may damage the device.

Note:

1. When VOD or VDD is biased, ensure that VLS never deviates from VBB.

CAUTION! These devices are sensitive to damage from electrostatic discharge (ESD). The leads should be shorted together during storage or handling to prevent damage to the device.

WARNING: To prevent damage to the sensor, a Schottky diode must connect VBB and VSS. See Figure 7.

Table 5. IL-P3-B Input/Output Characteristics

Input Characteristics: Capacitance to VBB [1]	Unit	Typical		
		512	1024	2048
from CR1, CR2[2]	pF	70	125	250
from CRLAST	pF	9	9	9
from RST	pF	7	7	7
from PR	pF	31	53	99
from TCK	pF	20	36	70
Output Characteristics:				
Output Impedance (R_{OUT})[3]	Ω	130Ω with I_{LOAD} = 10 mA		
Amplifier Supply Current (I_{DD}) [4]	mA	14mA with I_{LOAD} = 10 mA		
DC Output Offset (VOS) [5]	V	8.3V with I_{LOAD} = 10 mA		

Notes:

1. Using 1V pk-pk 1MHz signal with +5V DC offset.
2. The two CR1 pins (pins 17 and 18) are internally connected, as are the two CR2 pins (pins 15 and 16).
3. In general, $R_{OUT}(\Omega) \simeq 324 * (I_{LOAD})^{-0.389}$, I_{LOAD} in mA.
4. In general, I_{DD} (mA) = 4 + I_{LOAD}, I_{LOAD} in mA.
5. In general, V_{OFFSET} (V) = 0.0018 * $(I_{LOAD})^2$ - 0.17 * (I_{LOAD}) + 9.8, I_{LOAD} in mA.

Table 6. IL-P3-B DC Operating Conditions

Symbol	Description	Unit	Min.	Rec. [1]	Max.
I_{LOAD}	Load current to the output (OS)	mA	7.5	10.0	18.0
VDD	Amplifier supply	V	13.5	14.0	15.0
VOD	Output reset drain	V	12.0	12.5	13.0
VSET	Output node set gate	V	0.7	1.2	1.4
VSTOR [2, 4]	Pixel storage gate	V	1.6	2.0	2.2
VPR	Pixel reset drain, guard ring	V	13	14	15
VHIGH	High bias voltage	V	13	14	15
VLOW	Low bias voltage	V	-0.5	0	15
VBB[3]	Substrate	V	-2.5	-2	-1.5
VLS	Light shield	V		VBB	
VSS[3]	Amplifier return	V		0	

Notes:

1. When deviating from the recommended biases, ensure that the new biases still meet the essential conditions on Table 8.
2. VSTOR may be adjusted to affect the antiblooming level. V_{SAT} decreases by ~ 870mV for every 1.0V reduction in VSTOR.
3. VBB should never be forward biased with respect to VSS. To protect against damage, a Schottky diode between VBB and VSS is recommended (see Figure 7).
4. The VSTOR operating limits are only valid for PR Low = 0V. When negative PR Low is applied, the VSTOR operating limits should be read as the difference, (VSTOR - PR Low). The antiblooming is determined by this difference.

Table 7. IL-P3-B AC Operating Conditions

Symbol	Description		Unit	Min.	Rec.[1]	Max.
CRx	All CR Clocks	low*	V		0	
		swing*	V	4.8	5.0	6.5
RST	Reset Clock	low	V		0	
		swing	V	7.0	7.0	9.0
TCK	Transfer Clock	low	V	-5.0	-3.5	-3.5
		high	V	4.5	5.0	6.0
PR[4]	Pixel Reset Clock	low	V	-6.0	0	
		swing	V	3.5	4.0	6.0
f_{DATA}[2]	Data rate		MHz	5		45
f_{LINE}[3]	Line rate	0512	kHz			82.3
		1024				42.5
		2048				21.6

Notes:

1. When deviating from the recommended biases, ensure that the new biases still meet the essential conditions on Table 8.
2. The minimum data rate can be lower than 5MHz if 100x antiblooming is not required.
3. Unless the pixel is reset using the PR clock, the integration time increases as line rate decreases. Dark signal is proportional to the integration time. The minimum line rate is determined by the maximum dark signal or the maximum dark signal shot noise that the application can tolerate.
4. The VSTOR operating limits are only valid for PR Low = 0V. When negative PR Low is applied, the VSTOR operating limits should be read as the difference, (VSTOR - PR Low). The antiblooming is determined by this difference.

Table 8. IL-P3-B Essential Bias Conditions

Conditions	If condition not satisfied, the sensor will exhibit…
CR1 high + 1 > TCK > VSTOR + 3	Larger lag
PR high > VSTOR + 1.5	High PRNU when exposure control is enabled
RST high + 5.5 > VOD	Poor MTF
VOD $\leq$ VDD - 1.5	Higher non-linearity
VLOW $\geq$ VBB + 2	Spurious charge injection under certain power-up conditions

Table 9. IL-P3-B Performance Specifications

Specification	Unit	Min.	Typ.	Max.
Saturation Output Voltage (VSAT)[1]	mV	680	800	930
rms Noise	mV		0.44	0.48
Wavelength of Peak Responsivity	nm		700	
Peak Responsivity	V/(μJ/cm^2)	41.3	43.7	46.5
Dynamic Range		1420:1	1820:1	2110:1
Charge Conversion Efficiency (CCE)	μV/e$^-$	8.8	9.3	9.9
Noise Equivalent Exposure (NEE)	pJ/cm^2	9	10	12
Saturation Equivalent Exposure (SEE)	nJ/cm^2	15	18	
Full Well Capacity[1]	ke$^-$	73	86	
Fixed Pattern Noise (FPN) [2,3]	mV		< 0.5	1.0
Photoresponse Non-Uniformity (PRNU) [4]	% OS			
8 pixel local neighborhood			3.0	6.5
Global			5.0	8.5
Charge Transfer Efficiency (CTE) (readout register)		0.99997	0.999999	
First Field Lag [5]	mV	3.1	4.3	5.4
Dark Signal, Integration time = 52μs	mV		0.19	0.22

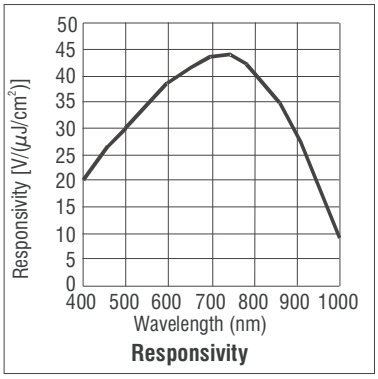
Notes:

1. VSTOR can be adjusted to increase VSAT and full well. As these quantities increase, the antiblooming capability is compromised.
2. Maximum peak-to-peak variation of all outputs.
3. Due to its general purpose design, the camera and sensor evaluation hardware provides an output that cannot be used to directly measure low FPN.
4. The peak-to-peak variation is measured at ~50% SEE.
5. Lag is measured at 500 mV. Lag is lower if signal is lower.

Test Conditions:

- Operating temperature = 35°C.
- f_{RST} = data rate per output = 40MHz.
- I_{LOAD} = 10mA.
- C_{LOAD} = 10pF.
- Tungsten halogen light source, black body color temperature 3200K, filtered with 750nm IR cutoff filter.
- See Sensor Measurement Definitions (doc# 03-36-00149) for specification definitions.

Figure 2. Performance Measurements



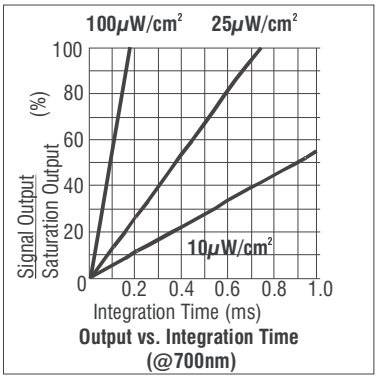


Table 10. IL-P3-B Timing Parameters

Symbol	Description	Unit	Min.	Rec.	Max.
t_{CR}	Period of CRx clocks				
t_1	Integration time (PR disabled)				
t_2	Integration time (PR enabled)				
t_3	TCK to first valid pixel	pixels	24		24
t_4	Overclock pixels	pixels	0	2	
t_5	CRLAST rising edge to CR2 falling edge	ns	$-0.25t_{CR}$	0	$0.25t_{CR}$
t_6	TCK high overlap with CR1 high	ns	200	200	
t_7	TCK falling edge to CR1 falling edge	ns	2		
t_8	CRLAST rising to RST rising edge	ns	$-0.25t_{CR}$	$0.5t_{CR} - t_{11}$	$0.5t_{CR} - t_{11}$
t_9	RST falling edge to CRLAST falling edge	ns	0	0	$0.5t_{CR}-t_{11}$
t_{10}	RST pulse width (FWHM)[1]	ns	3.5	5	$0.25t_{CR}$
t_{11}	CR rise and fall time	ns	1	2	$0.25t_{CR}$

Notes:

1. Full Width Half Maximum

Figure 3. IL-P3-B Overall Timing

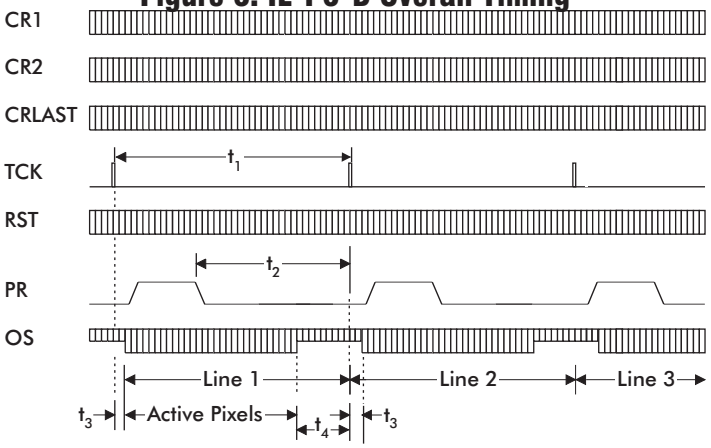


Figure 4. IL-P3-B Detailed Readout Register Timing

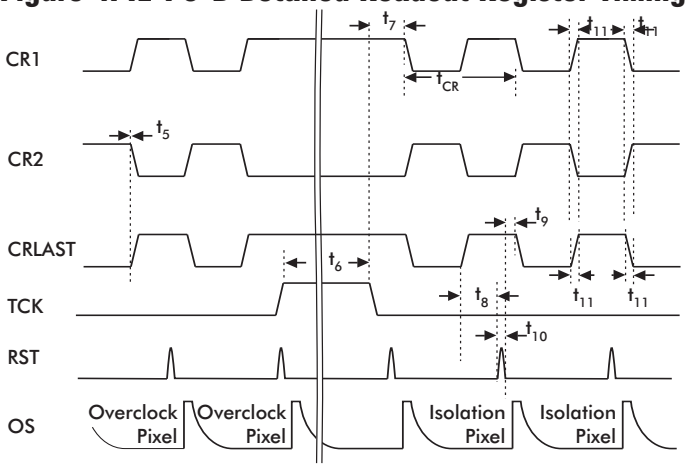


Figure 5. IL-P3-B Gate Structure Diagram

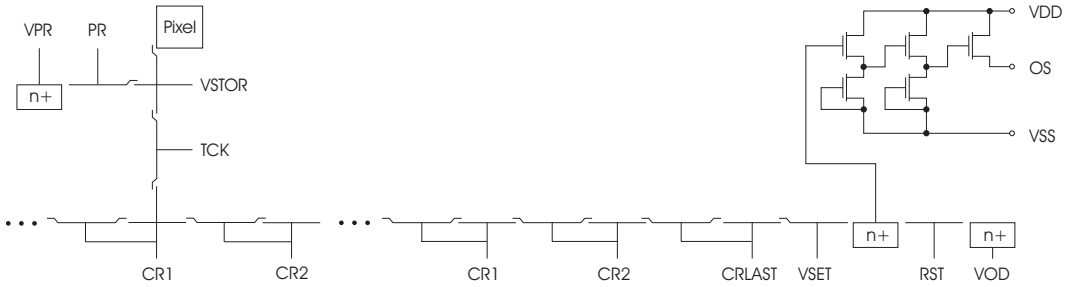


Figure 6. IL-P3-B Readout Register Timing

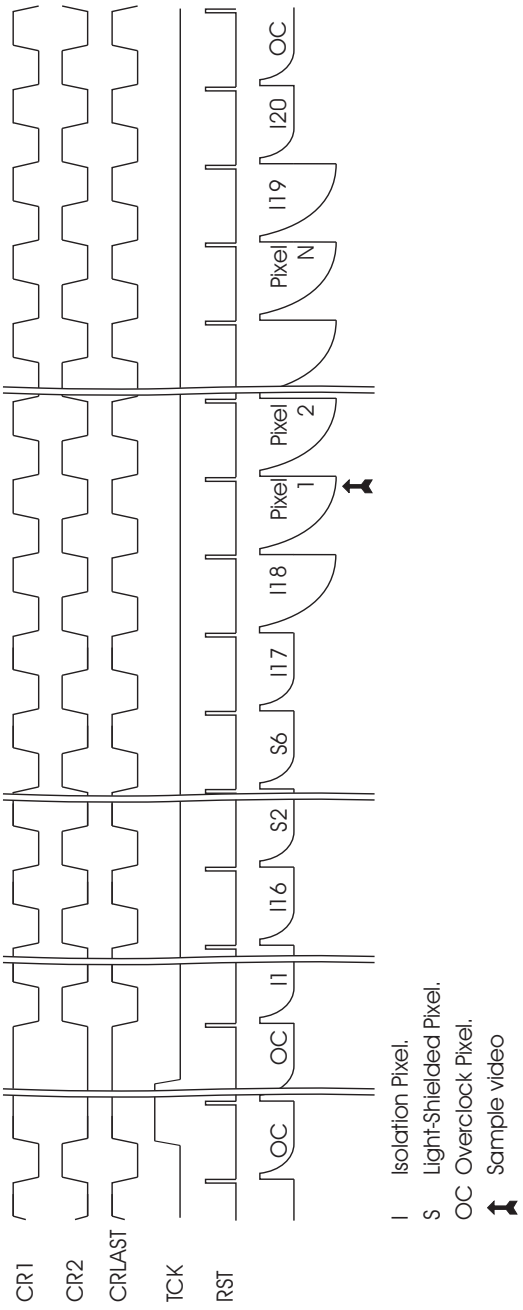
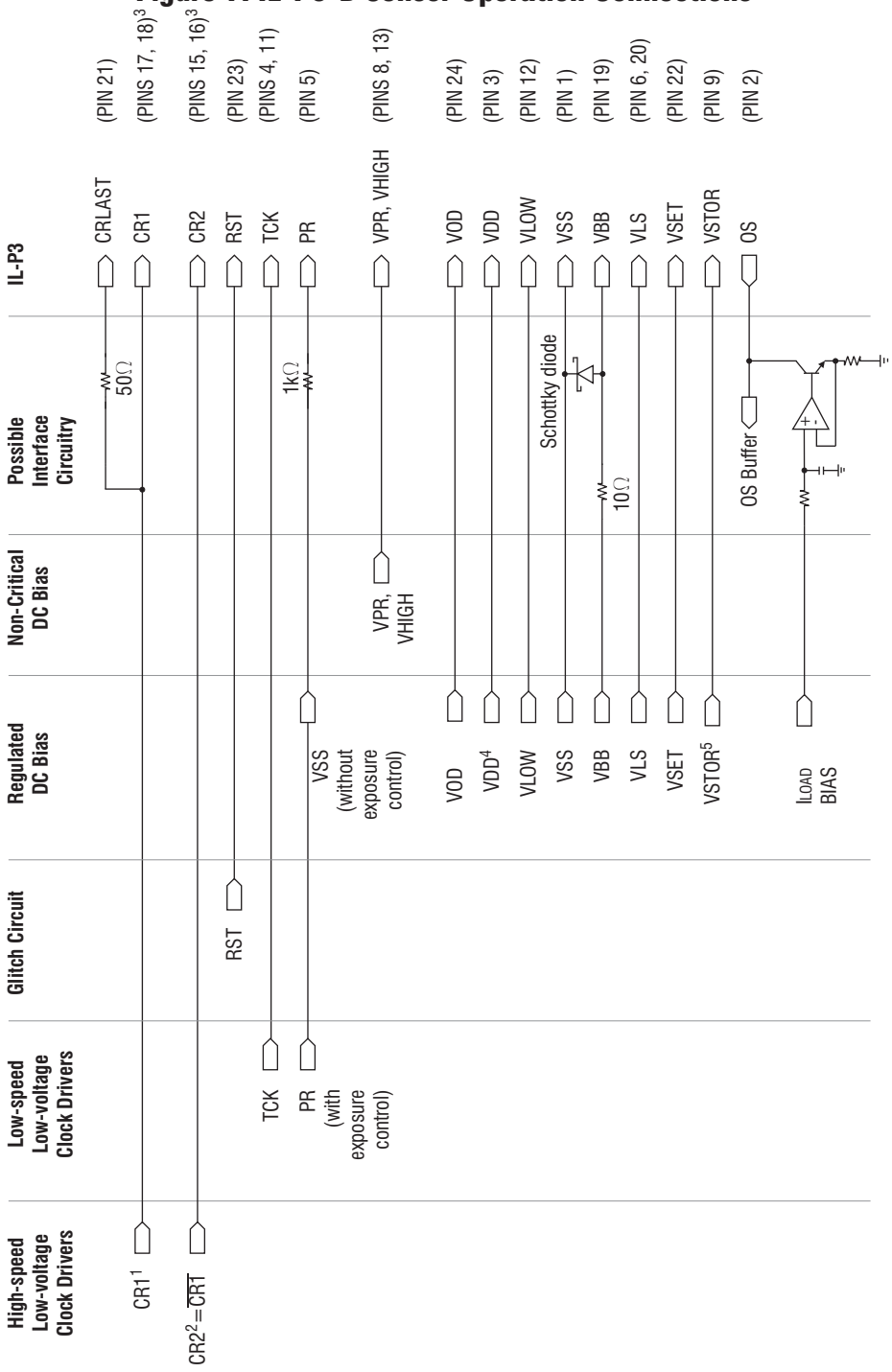


Figure 7. IL-P3-B Sensor Operation Connections

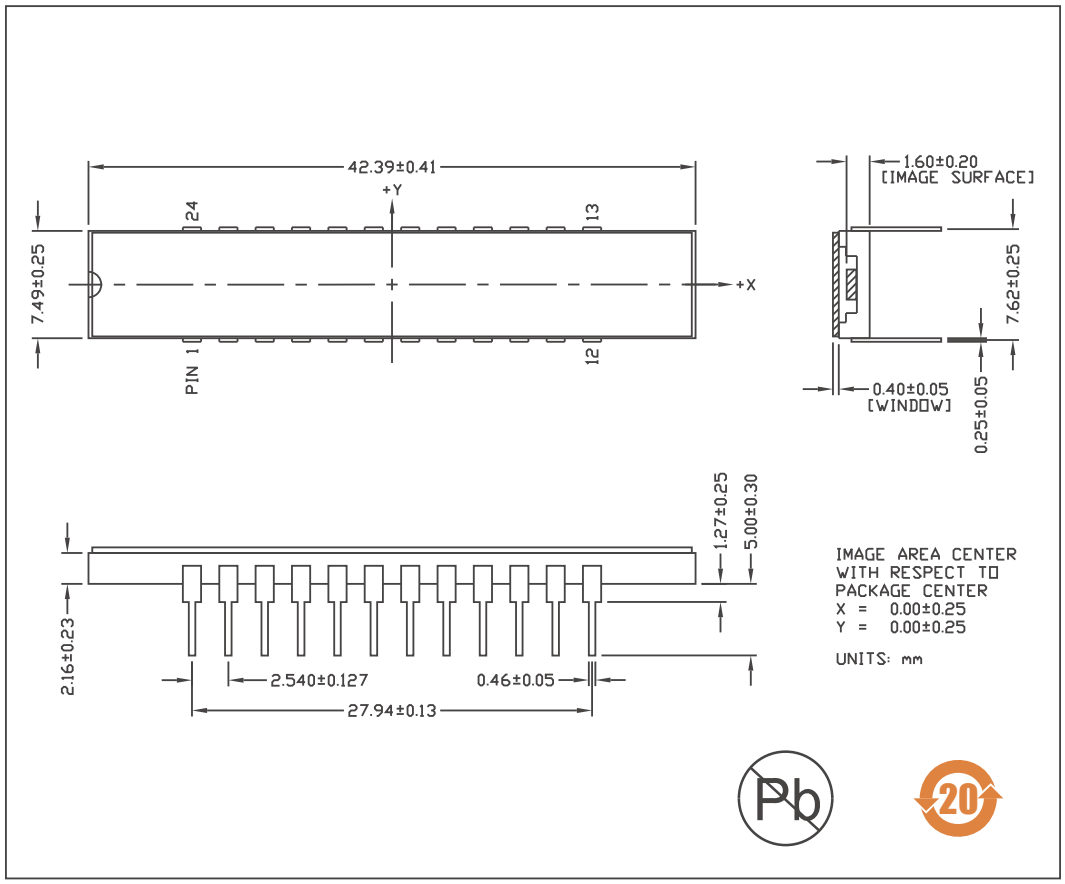


Notes to Figure 7.

1. Clock drivers are designed to drive only up to a maximum capacitance (C_{MAX}) at a given clock frequency. If the total capacitances of CRLAST and CR1 (see Table 5) exceed C_{MAX}, more than one CR1 driver is required.
2. Clock drivers are designed to drive only up to a maximum capacitance (C_{MAX}) at a given clock frequency. If the total capacitances of CR2 (see Table 5) exceed C_{MAX}, more than one CR2 driver is required.
3. Each pin should be connected to a clock driver, though not necessarily to the same clock driver. If more than one clock driver is used, it is acceptable to drive each pin from separate drivers.
4. Need to source $I_{DD} = 4 + I_{LOAD}$ mA.
5. May have an optional antiblooming level adjustment.

ISO 9001 Teledyne DALSA maintains a registered quality system meeting the ISO 9001 standard.

Figure 8. IL-P3-B Package Dimensions*



***Note:** 2048 mechanical shown. Sensor mechanicals for the 1k and 512 resolutions available on request.

Table 11: Revision History

Revision	Description
00	Document release
01	Depiction of "center array to edge" measurement for the 512 and 2048 sensor mechanical drawings referenced incorrectly. Correct reference restored. References to "offset/swing" changed to "low/swing". VLOW value changed to -0.5V. VBB value changed to -2.5V. CRLAST rising to RST rising edge timing parameter changed to -0.25tcr.
02	VBB operating conditions now listed as Min. -2.5V, Rec. -2V, Max. -1.5V. VLS operating conditions listed as Rec. VBB.
03	Added "The isolation pixels should not be used for calibration or detection" to the Functional Description→Output section
04	Added Figure 1. IL-P3-B Block Diagram. Diagram was missing.
05	Added PR Low (min) spec of -6V to table 7. Added a note 4 to VSTOR in table 6 and note 5 to PR in table 7.
06	Added “RoHs compliant” to Features section on page 1. Added lead-free logo to Figure 8.
07	Added revised 2048 package dimensions. Sensor length and height tolerance updated. Note 1 removed.
08	Added RoHS logo to Figure 8.
09	Note added to Table 4.”When VOD or VDD is biased, ensure that VLS never deviates from VBB.” Table 7. AC Operating Conditions, note removed stating that it is important that RST have a 5-V swing, an alternate set of biases is available...The alternative biases result in a reduction of either the antiblooming performance or VSAT. Revised mechanical drawing added.