

Fine Tune Sensitivity 2-wired Monaural Microphone Amplifier

■ FEATURES

- Supply Voltage $V_s = 8V$ to $16V$
- Operating Voltage $V_{DD} = 1.8V$ to $16V$
- 2-wired connections
- Built-in Pre-Amplifier (FET Input for Impedance Converter) & Bias Circuit
- Voltage Gain Range
24dB to 40dB (Set by external resistors.)
- Adjust and memorize the gain by 2-wire serial interface
- Gain Adjustment 9dB \pm 3dB / 0.2dB step
- Maximum Output Voltage 2.1Vrms typ.
- Equivalent Input Noise Voltage -111dBV typ.
- CMOS Technology
- Package MSOP10 (TVSP10)

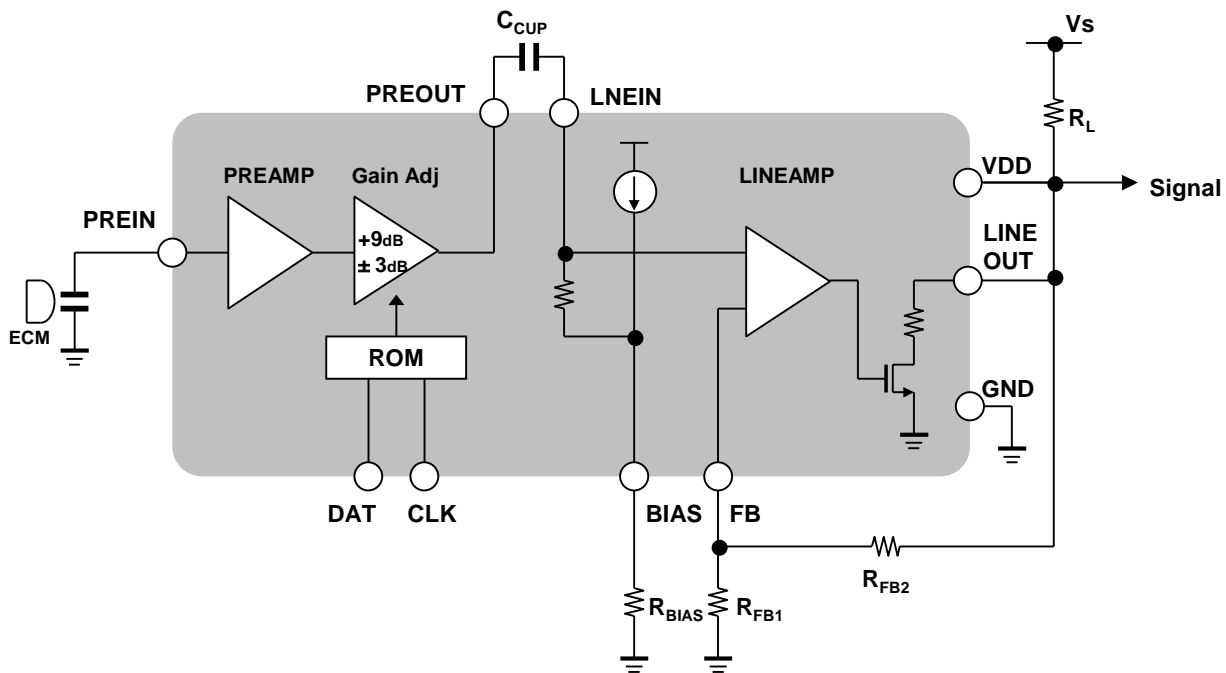
■ DESCRIPTION

The NJU72090 is a monaural microphone amplifier IC including pre-amplifier (impedance converter) for ECM microphone, gain adjuster and line amplifier. It is able to set the output gain by external resistors. And it is able to adjust and memorize the gain after parts assembling. The NJU72090 is the most suitable for the ECM especially which needs sensitivity accuracy.

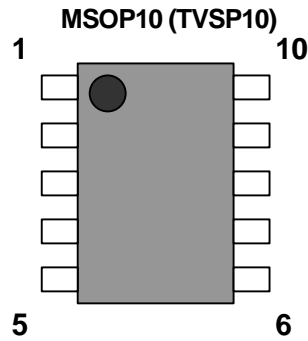
■ APPLICATIONS

- Microphone module
- Hands-free microphones
- ECM module

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	SYMBOL	FUNCTION
1	PREOUT	Pre-amplifier output terminal
2	LINEIN	Line amplifier input terminal
3	BIAS	Reference current setting terminal
4	FB	Line amplifier feedback terminal
5	LINEOUT	Line amplifier output terminal
6	VDD	Power supply terminal
7	GND	Ground terminal
8	DAT	Serial data input terminal
9	CLK	Serial clock input terminal
10	PREIN	Pre-amplifier input terminal

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU72090RB2 (TE1)	MSOP10 (TVSP10)	Yes	Yes	Sn2Bi	72090	19	2000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage	V_{DD}	18 ⁽¹⁾	V
Maximum Input Voltage	V_{imax}	0.3	V _{rms}
Power Dissipation ($T_a = 25^\circ\text{C}$) MSOP10 (TVSP10)	P_D	2-Layer 470 ⁽²⁾	mW
Storage Temperature	T_{stg}	-40 to 150	°C
Junction Temperature	T_j	150	°C

(1) VDD terminal

(2) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage	V_{DD}	1.8 to 16 ⁽¹⁾	V
Operating Temperature	T_{opr}	-40 to 105	°C

(1) VDD terminal

■ ELECTRICAL CHARACTERISTICS

 (V_S = 8V, R_L = 680Ω, R_{BIAS} = 18kΩ, R_{FB1} = 1kΩ, R_{FB2} = 27kΩ, f = 1kHz, T_a = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS (R_G = 0Ω, No Signal, unless otherwise noted.)						
Supply Current1	I _{DD1}		-	4.85	6.00	mA
Supply Current2	I _{DD2}	R _{FB1} = 0Ω, R _{FB2} = ∞, VDD terminal	-	220	320	μA
Supply Current3	I _{DD3}	R _L = 0Ω	-	24	35	mA
Reference Current	I _{REF}		-	9.3	-	μA
Output DC Voltage	V _O	LINEOUT terminal	4.6	4.7	4.8	V
AC CHARACTERISTICS (C_{IN} = 1nF, unless otherwise noted.)						
PREIN Input Capacitance	C _{IPRE}		-	1	-	pF
PREIN Input Resistance	R _{iPRE}		-	500	-	GΩ
LINEIN Input Resistance	R _{iLINE}		210	300	390	kΩ
PREOUT Typical Voltage Gain	G _{vtyp}	V _{IN} = 10mVrms, GAIN setting = 0 × 00	-	9	-	dB
PREOUT Maximum Voltage Gain	G _{vmax}	V _{IN} = 10mVrms, GAIN setting = 0 × 0F	-	12	-	dB
PREOUT Minimum Voltage Gain	G _{vmin}	V _{IN} = 10mVrms, GAIN setting = 0 × 10	-	5.8	-	dB
Voltage Gain	G _v	V _{IN} = 10mVrms,	36.9	37.9	38.4	dB
Frequency Response	ΔG _f	f = 1kHz to 10kHz, C _{CUP} = 15nF	-0.5	0.0	0.5	dB
Equivalent Input Noise Voltage	V _{NI}	Weighted-A	-	-111	-107	dBV
Total Harmonic Distortion	THD	V _{IN} = 10mVrms, BW = 400Hz to 30kHz	-	0.1	0.5	%
Maximum Output Voltage	V _{OM}	THD = 3%	1.8	2.1	-	Vrms
Ripple Rejection Ratio	RR	V _{Ripple} = 0.5Vrms	-	30	-	dB

■ THERMAL CHARACTERISTICS

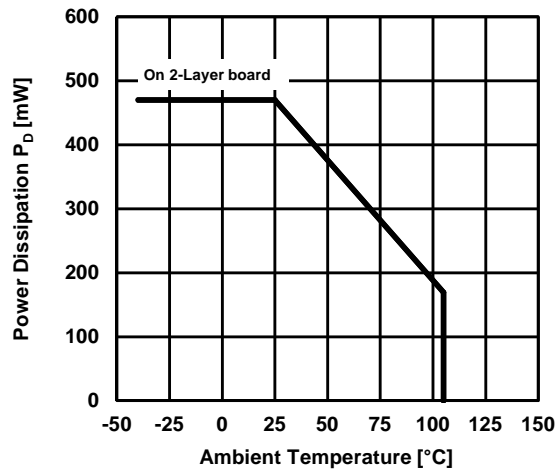
PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance MSOP10 (TVSP10)	θ_{ja}	2-Layer 266 ⁽²⁾	°C/W

(2) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

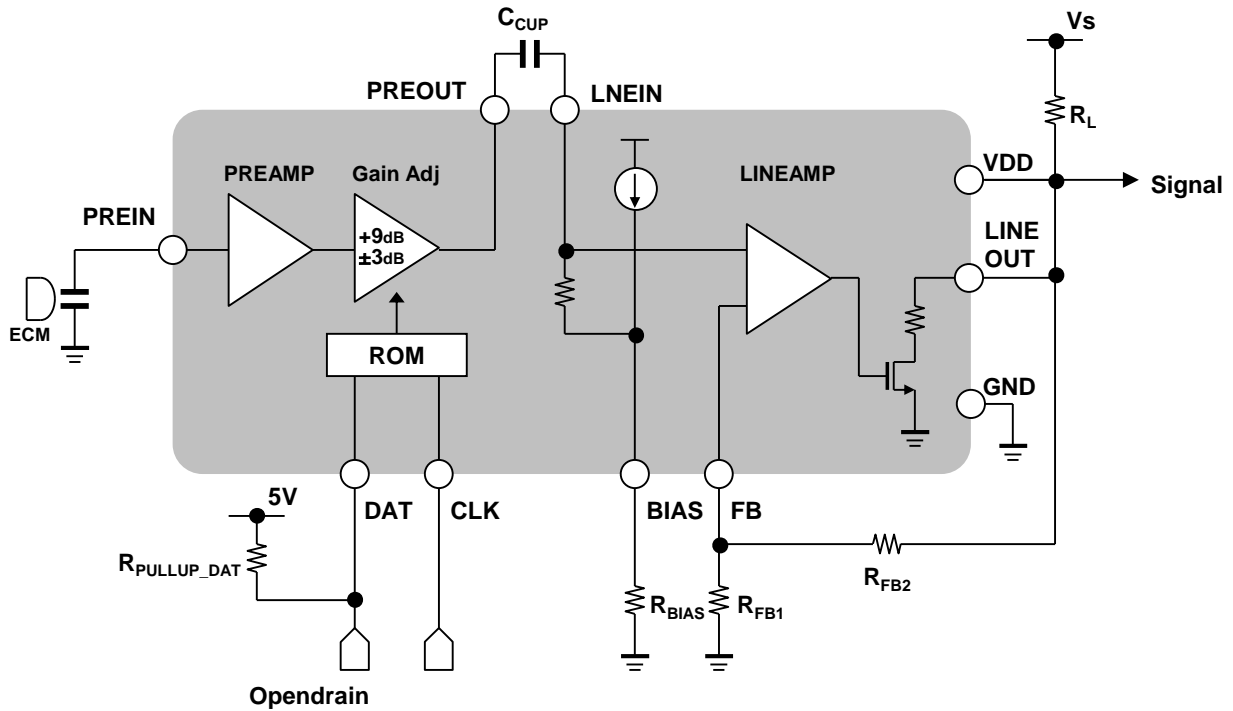
■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

MSOP10 (TVSP10) Power Dissipation vs. Temperature

$T_{opr} = -40^{\circ}\text{C}$ to 105°C , $T_j = 150^{\circ}\text{C}$



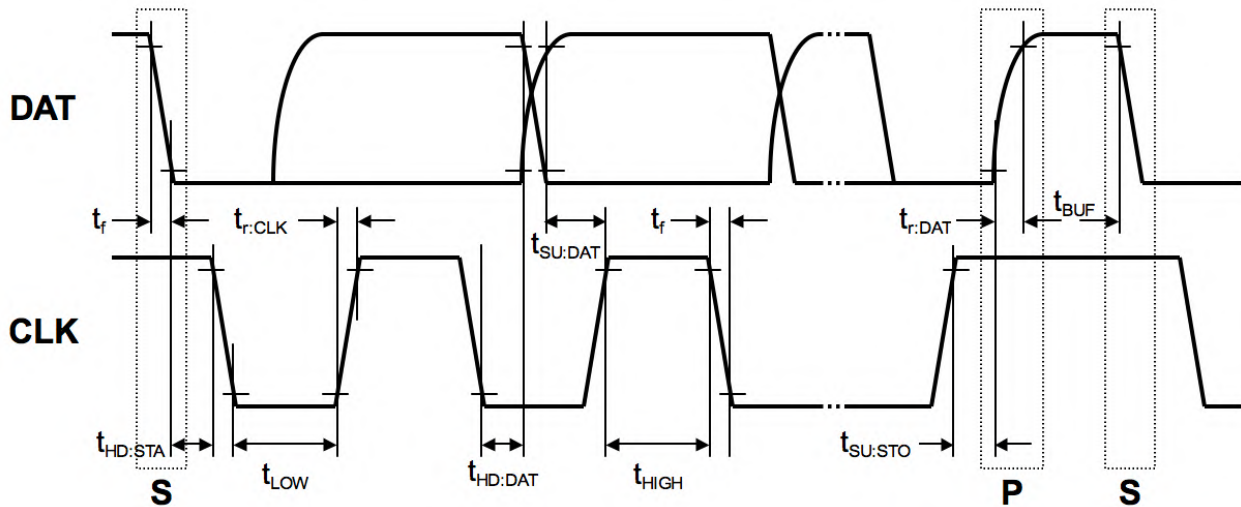
■ APPLICATION CIRCUIT



■ 2-wire BUS (DAT, CLK)

The NJU72090 has a 2-wire serial interface with a DAT terminal and a CLK terminal. The DAT terminal is open drain, and the CLK terminal is controlled by push-pull drive.

The CLK terminal requires a source current capacity of up to 100mA (CLK OTP write current (I_{WRITE})) when writing OTP.

■ TIMING ON 2-wire BUS (DAT, CLK)

■ CHARACTERISTICS OF I/O STAGES FOR 2-wire BUS (DAT, CLK)

 (T_a = 25°C, V_S = 8V, R_L = 680Ω, R_{BIAS} = 18kΩ, R_{FB1} = 1kΩ, R_{FB2} = 27kΩ, R_{PULLUP_DAT} = 3.9kΩ unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLK High Level Input Voltage	V _{IH_CLK}	4.95	5.00	5.30	V
CLK Low Level Input Voltage	V _{IL_CLK}	0.0	-	0.3	V
DAT High Level Input Voltage	V _{IH_DAT}	2.0	5.0	5.5	V
DAT Low Level Input Voltage	V _{IL_DAT}	0.0	-	0.3	V
DAT Low Level Output Voltage	V _{OL_DAT}	0.0	-	0.3	V
CLK High Level Input Current	I _{IH_CLK}	-	-	40	μA
CLK Low Level Input Current	I _{IL_CLK}	-	0	-	μA
DAT High Level Input Current	I _{IH_DAT}	-	-	40	μA
DAT Low Level Input Current	I _{IL_DAT}	-	0	-	μA
CLK Supply Current for OTP Writing	I _{WRITE}	-	-	100	mA

■ CHARACTERISTICS OF BUS LINES (DAT,CLK) FOR 2-wire BUS DEVICES

 (T_a = 25°C, V_S = 8V, R_L = 680Ω, R_{BIAS} = 18kΩ, R_{FB1} = 1kΩ, R_{FB2} = 27kΩ, R_{PULLUP_DAT} = 3.9kΩ unless otherwise noted.)

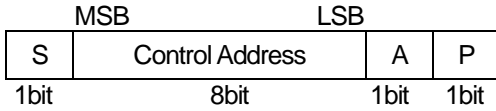
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLK clock frequency	f _{CLK}	10	50	68	kHz
Rise time of CLK signals	t _{r:CLK}	-	-	50	ns
Rise time of DAT signals	t _{r:DAT}	-	-	1	μs
Fall time of both CLK and DAT signals	t _f	-	-	300	ns
Hold time (repeated) START condition.	t _{HD:STA}	4	-	-	μs
Low period of clock	t _{LOW}	4.7	-	-	μs
High period of clock	t _{HIGH}	9.5	10.0	10.5	μs
Data set-up time	t _{SU:DAT}	250	-	-	ns
Set-up time for STOP condition	t _{SU:STO}	160	-	-	ns
Data hold time	t _{HD:DAT}	5	-	-	ns
Bus free time between a STOP and START condition	t _{BUF}	4.7	-	-	μs

■ DEFINITION OF 2-wire REGISTER

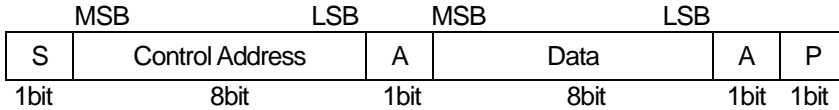
Note) Please don't send except specified data for avoiding an incorrect operation.

2-wire BUS FORMAT

<1byte command (RESET)>



<2byte command>



S: Starting Term
A: Acknowledge Bit
P: Ending Term

Control Address

Mode	Mode Select								Hex	Contents
	MSB				LSB					
RESET *	1	0	0	0	0	0	0	0	80(h)	Reload the setting from ROM.
READ	1	0	0	0	0	0	0	1	81(h)	Output the setting to DAT terminal.
CONTROL	1	0	0	0	0	0	1	0	82(h)	Write the setting on RAM and read it.
WRITE	1	0	0	0	0	1	0	0	84(h)	Write the setting on ROM.

*Please use the "1byte command" in case of RESET mode.

CONTROL REGISTER DATA TABLE

<CONTROL and WRITE Mode>

	MSB		LSB					
BIT								
D7	D6	D5	D4	D3	D2	D1	D0	
Don't Care	Don't Care	Don't Care	GAIN					

CONTROL REGISTER DEFAULT VALUE OF INTERNAL ROM

The NJU72090 read setting from internal ROM when power is turn on.
Control register default value of internal ROM is all "0" before you write setting on ROM.

	MSB		LSB				
BIT							
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

■ DEFINITION OF RESISTOR

GAIN: 5.8dB to 12.0dB in 0.2dB/step. 5-bit signed binary.

MSB					LSB		
BIT							
D7	D6	D5	D4	D3	D2	D1	D0
Don't Care	Don't Care	Don't Care	GAIN				

<GAIN Data>

Data					Setting
D4	D3	D2	D1	D0	
1	0	0	0	0	+5.8dB
1	0	0	0	1	+6.0dB
1	0	0	1	0	+6.2dB
1	0	0	1	1	+6.4dB
1	0	1	0	0	+6.6dB
1	0	1	0	1	+6.8dB
1	0	1	1	0	+7.0dB
1	0	1	1	1	+7.2dB
1	1	0	0	0	+7.4dB
1	1	0	0	1	+7.6dB
1	1	0	1	0	+7.8dB
1	1	0	1	1	+8.0dB
1	1	1	0	0	+8.2dB
1	1	1	0	1	+8.4dB
1	1	1	1	0	+8.6dB
1	1	1	1	1	+8.8dB
0	0	0	0	0	+9.0dB ⁽¹⁾
0	0	0	0	1	+9.2dB
0	0	0	1	0	+9.4dB
0	0	0	1	1	+9.6dB
0	0	1	0	0	+9.8dB
0	0	1	0	1	+10.0dB
0	0	1	1	0	+10.2dB
0	0	1	1	1	+10.4dB
0	1	0	0	0	+10.6dB
0	1	0	0	1	+10.8dB
0	1	0	1	0	+11.0dB
0	1	0	1	1	+11.2dB
0	1	1	0	0	+11.4dB
0	1	1	0	1	+11.6dB
0	1	1	1	0	+11.8dB
0	1	1	1	1	+12.0dB

⁽¹⁾Initial Setting

APPLICATION NOTES

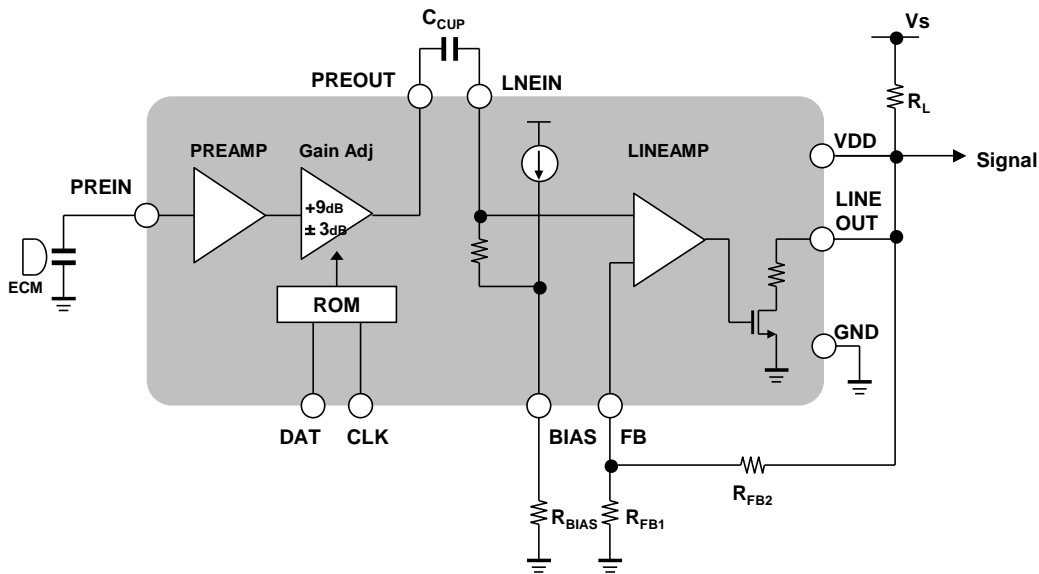


Fig. 1 Application circuit example

1. Supply Voltage of Vs

The recommended supply voltage range of Vs is as follows:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	Vs		-	8	16	V

2. Voltage Gain

2.1 Pre-Amplifier + Gain adjustment

$$G_{VP} = 9 \text{ [dB]} \quad (\text{With Gain adjustment typical gain})$$

2.2 Line Amplifier

$$G_{VL} = 20 \cdot \text{Log} \left(1 + \frac{R_{FB2}}{R_{FB1}} \right) \text{ [dB]}$$

$$\text{Ex. } G_{VL} = 20 \cdot \text{Log} \left(\frac{27\text{k}}{1\text{k}} \right) \approx 28.9 \text{ [dB]}$$

$$V_{OUT} = V_{BIAS} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}} \right) \text{ [V]}, \quad V_{BIAS} = I_{REF} \cdot R_{BIAS}$$

$$\text{Ex. } V_{OUT} = 9.3\mu\text{A} \cdot 18\text{k} \cdot \left(1 + \frac{27\text{k}}{1\text{k}} \right) \approx 4.7 \text{ [V]}$$

2.4 NJU72090 TOTAL

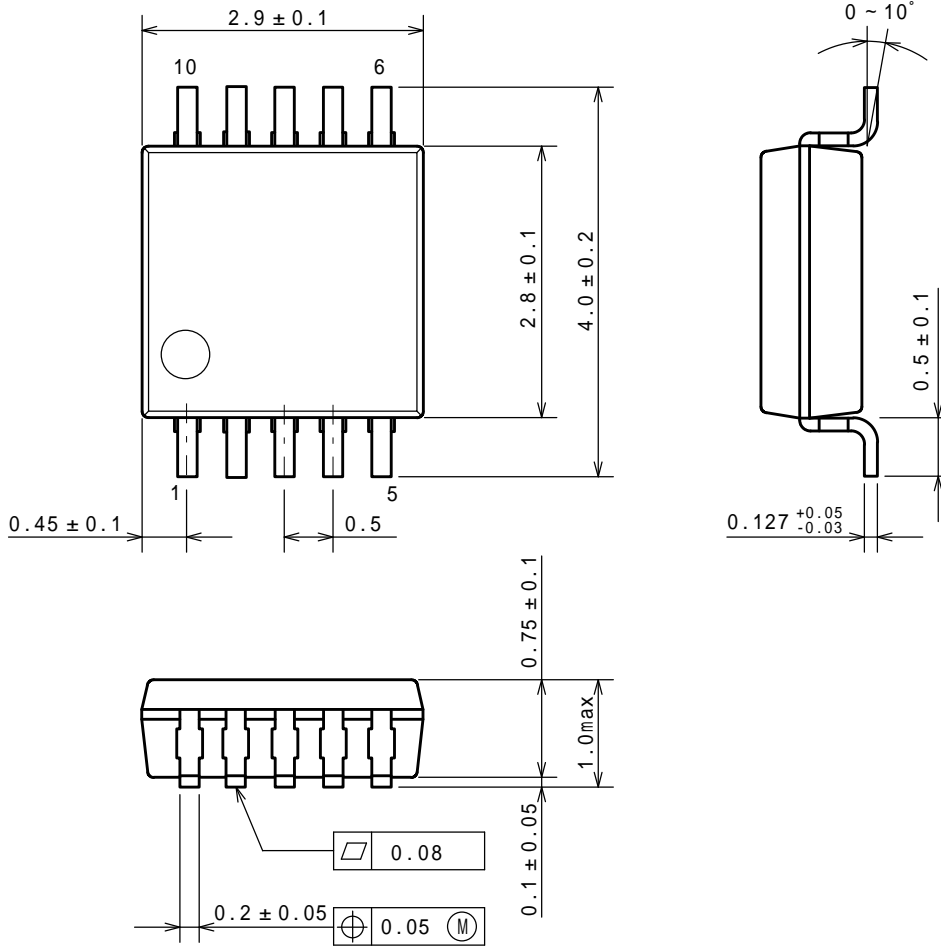
$$G_V = G_{VP} + G_{VL} = G_{VP} + 20 \cdot \text{Log} \left(1 + \frac{R_{FB2}}{R_{FB1}} \right) \text{ [dB]}$$

$$\text{Ex. } G_V = 9 + 20 \cdot \text{Log} \left(1 + \frac{27\text{k}}{1\text{k}} \right) \approx 37.9 \text{ [dB]}$$

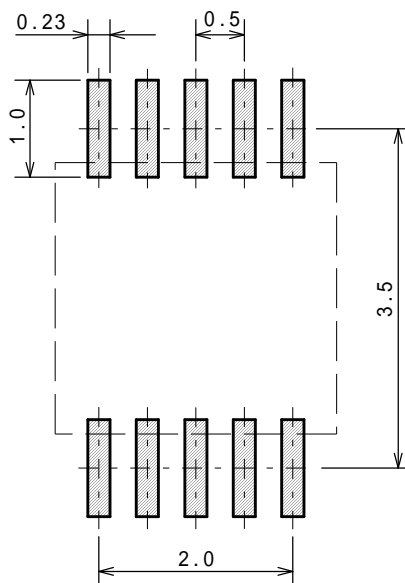
MSOP10 (TVSP10) MEET JEDEC MO-187-DA/THIN TYPE

■ PACKAGE DIMENSIONS

Unit: mm



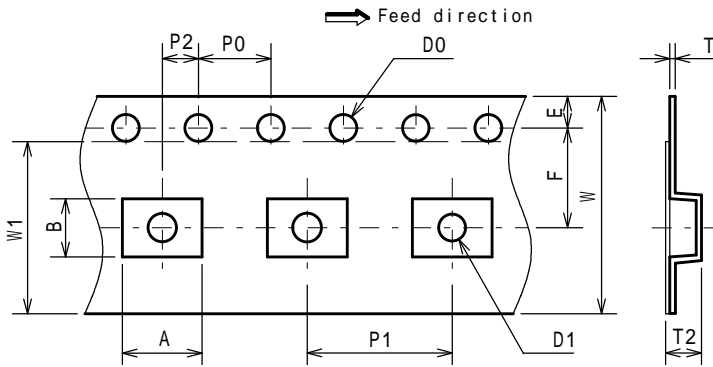
■ EXAMPLE OF SOLDER PADS DIMENSIONS



MSOP10 (TVSP10) MEET JEDEC MO-187-DA/THIN TYPE

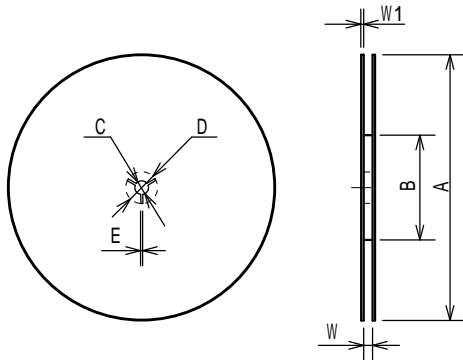
PACKING SPEC TAPING DIMENSIONS

Unit: mm



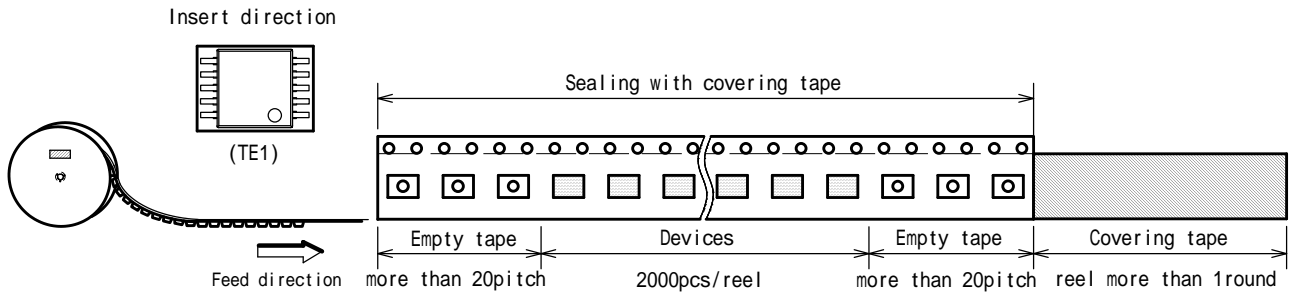
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	1.5 ^{+0.1} ₀	
D1	1.5 ^{+0.1} ₀	
E	1.75 ± 0.1	
F	5.5 ± 0.05	
P0	4.0 ± 0.1	
P1	8.0 ± 0.1	
P2	2.0 ± 0.05	
T	0.3 ± 0.05	
T2	1.75 (MAX.)	
W	12.0 ± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

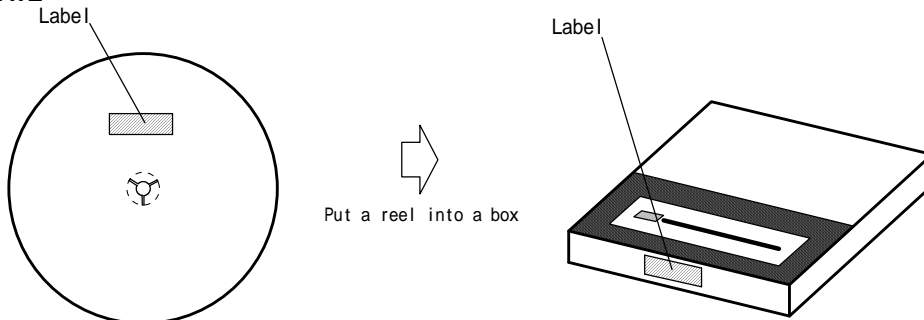


SYMBOL	DIMENSION
A	254 ± 2
B	100 ± 1
C	13 ± 0.2
D	21 ± 0.8
E	2 ± 0.5
W	13.5 ± 0.5
W1	2.0 ± 0.2

TAPING STATE

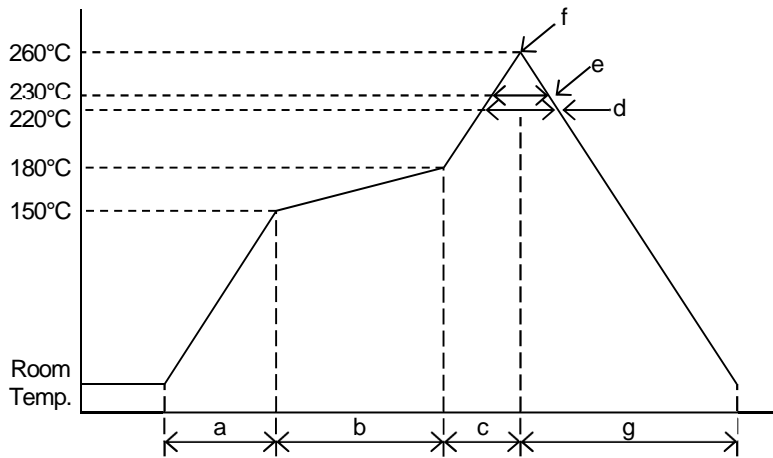


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature	150 to 180°C
	Pre-heating time	60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISION	CHANGES
November 17, 2020	Ver.1.0	Initial release

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