

# M74ALS38AP

91D 12367 D

6249827 MITSUBISHI (DGTL LOGIC)

## QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

T-43-15

### DESCRIPTION

The M74ALS38AP is a semiconductor integrated circuit consisting of four 2-input positive-logic NAND buffer gates with open collector outputs, usable as negative-logic NOR buffer gates.

### FEATURES

- Wired-AND connectability
- High fan-out ( $I_{OL} = 24\text{mA}$ )
- High-breakdown output voltage ( $V_O \geq 7\text{V}$ )
- High speed ( $t_{pd} = 11.5\text{ns}$  typical;  $C_L = 50\text{pF}$ )
- Low power dissipation ( $P_d = 14.2\text{mW}$  typical)
- Wide operating temperature range ( $T_a = -20 \sim +75^\circ\text{C}$ )

### APPLICATION

General purpose, for use in Industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

This device employs PNP transistor inputs and open collector outputs. The open collector output enables selection of high-level output impedance with an external resistor. It also permits wired-AND connection which is impossible with ordinary gates. Having a large low-level output current ( $I_{OL}$ ) of 24mA, it is suitable for a buffer gate. Utilization of a clamp diode in the inputs and outputs reduces ringing and undershooting.

When both A and B inputs are high-level, output Y is low-level, and when at least one of the inputs is low, the output is high.

The M74ALS1003AP, which, except for its name, is identical in all respects to the M74ALS38AP, is also available.

### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

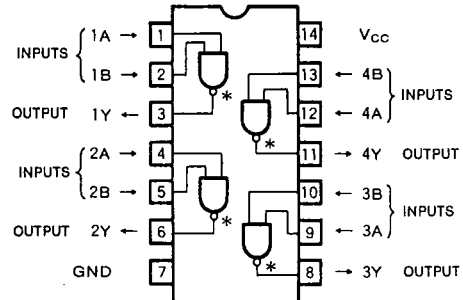
### ABSOLUTE MAXIMUM RATINGS ( $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		-0.5 ~ +7	V
$V_i$	Input voltage		-0.5 ~ +7	V
$V_o$	Output voltage	High-level state	-0.5 ~ +7	V
$T_{opr}$	Operating free-air ambient temperature range		-20 ~ +75	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		-65 ~ +150	$^\circ\text{C}$

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage			5.5	V
$I_{OL}$	Low-level output current	0		24	mA
$T_{opr}$	Operating free-air ambient temperature range	-20		+75	$^\circ\text{C}$

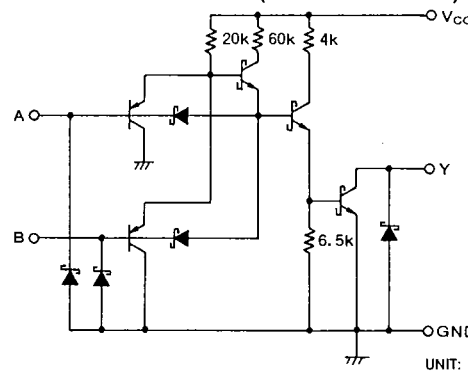
### PIN CONFIGURATION (TOP VIEW)



\*: OPEN COLLECTOR OUTPUT

Outline 14P4

### CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT:  $\Omega$

**QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT**

**ELECTRICAL CHARACTERISTICS** ( $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{IC}$	Input clamp voltage	$V_{CC}=4.5\text{V}, I_{IC}=-18\text{mA}$			-1.2	V
$I_{OH}$	High-level output current	$V_{CC}=4.5\text{V}, V_O=5.5\text{V}$			0.1	mA
$V_{OL}$	Low-level output voltage	$V_{CC}=4.5\text{V}$			0.25	0.4
			$I_{OL}=12\text{mA}$		0.35	0.5
$I_I$	Input current at maximum voltage	$V_{CC}=5.5\text{V}, V_I=7\text{V}$			0.1	mA
$I_{IH}$	High-level input current	$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$			-0.1	mA
$I_{CCH}$	Supply current, all outputs high	$V_{CC}=5.5\text{V}, V_I=0\text{V}$		0.86	1.6	mA
$I_{CCL}$	Supply current, all outputs low	$V_{CC}=5.5\text{V}, V_I=4.5\text{V}$		4.8	7.8	mA

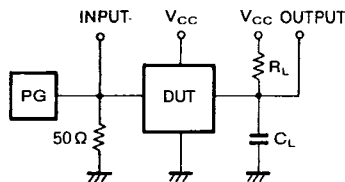
\* : All typical values are at  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ .

**SWITCHING CHARACTERISTICS**

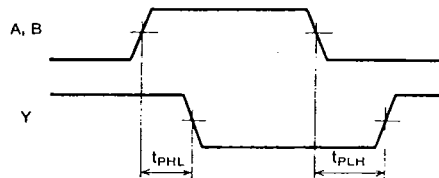
Symbol	Parameter	Test conditions/Limits (Note 1)									Unit		
				$V_{CC}=5\text{V}$			$V_{CC}=4.5\sim 5.5\text{V}$						
				$C_L=15\text{pF}$			$C_L=50\text{pF}$						
				$R_L=680\Omega$			$R_L=680\Omega$						
				$T_a=25^\circ\text{C}$			$T_a=0\sim 70^\circ\text{C}$			$T_a=-20\sim +75^\circ\text{C}$			
		Inputs	Output	Typ	Min	Typ*	Max	Min	Typ*	Max			
$t_{PLH}$	Propagation time	A, B	Y	9	10	14	33	10	14	34	ns		
$t_{PHL}$				4	2	9	12	2	9	13			

\* : All typical values are at  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ .

Note 1: Measurement circuit



**TIMING DIAGRAM (Reference level = 1.3V)**



(1) The pulse generator (PG) has the following characteristics:

PRR  $\leq 1\text{MHz}$

$t_r=2\text{ns}, t_f=2\text{ns}$

$V_{IH}=3.5\text{V}, V_{IL}=0.3\text{V}$

duty cycle=50%

$Z_o=50\Omega$

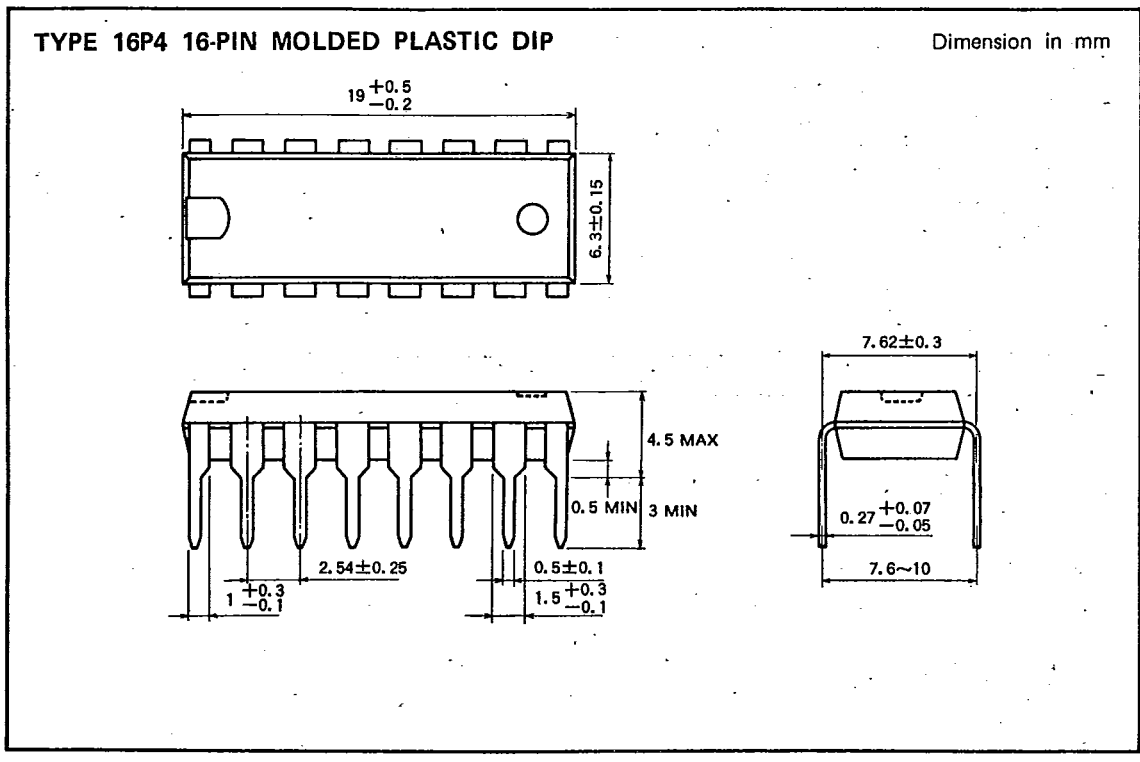
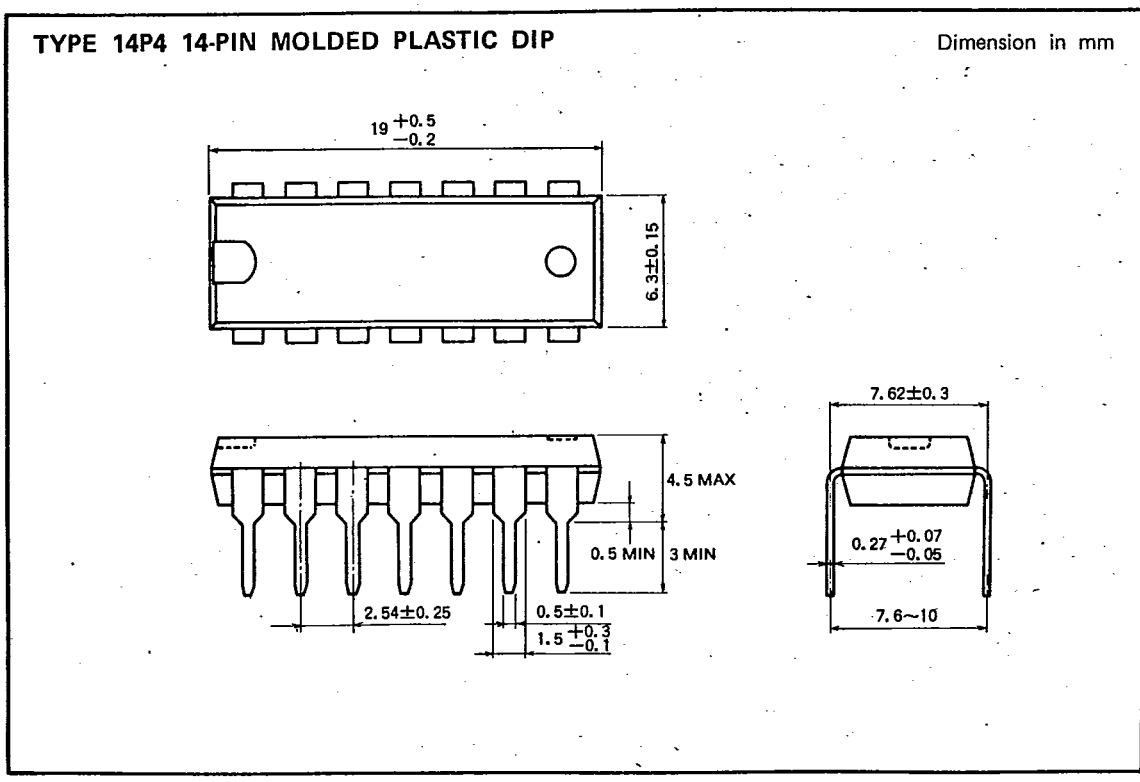
(2)  $C_L$  includes probe and jig capacitance.

PACKAGE OUTLINES

MITSUBISHI {DGTL LOGIC}

91D 12323

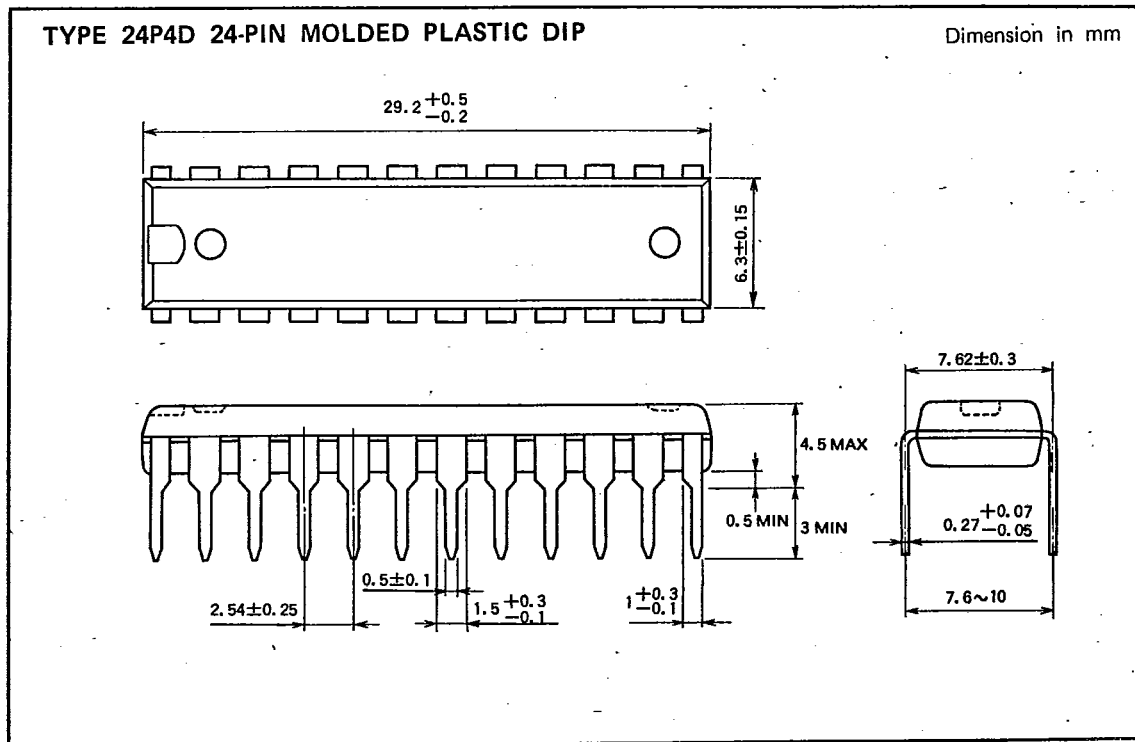
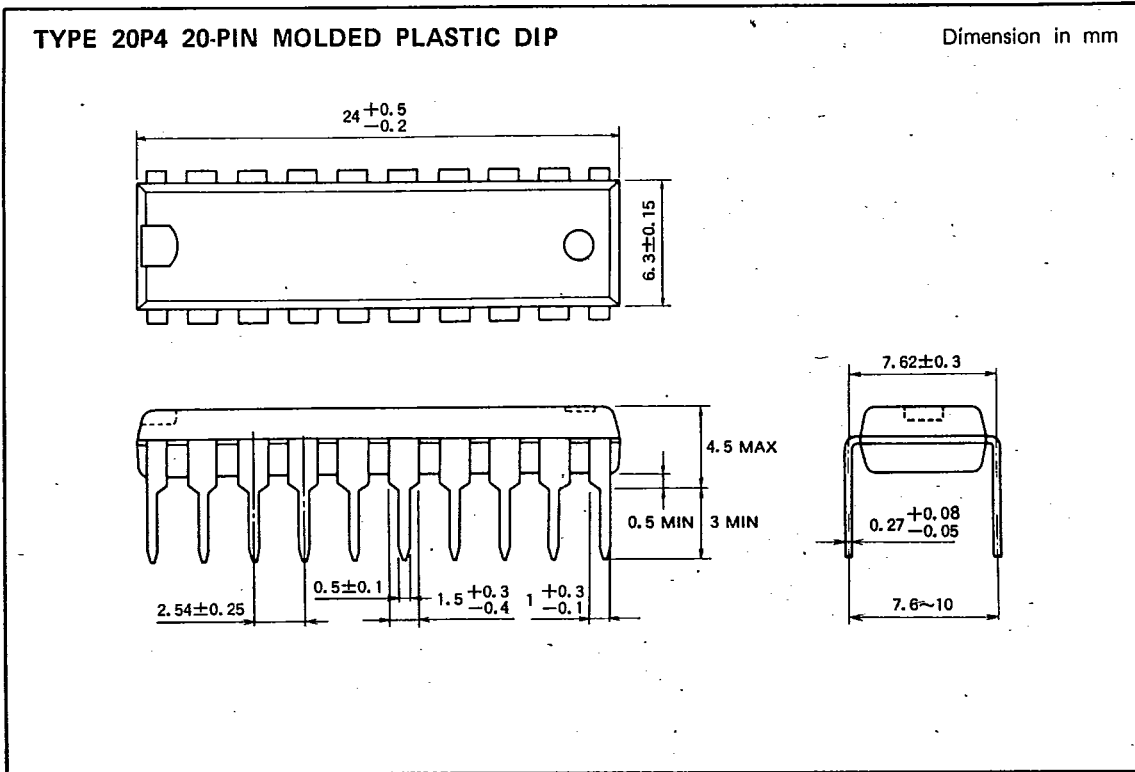
D T-9020



PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12324 D T-90-20



**TYPE DESIGNATION TABLE**

MITSUBISHI (DGLT LOGIC)

91D D ■ 6249827 0012784 7 ■ MIT3

T-90-20

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	*	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	*	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	*	Hex Inverter	14P2P
M74ALS05ADP	**	Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	*	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	**	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	*	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	*	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	**	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	**	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	**	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	*	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	**	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	**	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	*	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	**	Dual J-K Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	*	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	**	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	*	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	**	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	**	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	**	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	**	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	*	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	**	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	**	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	*	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	*	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	**	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	**	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	**	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	**	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	**	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	**	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	**	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	**	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	**	Hex Noninverting Buffer	14P2P

\*: New product    \*\*: Under development

6249827 MITSUBISHI (DGTL LOGIC)

91D 12785 D

MITSUBISHI ALSTTLs

**DESCRIPTION**

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012785 9 ■ MIT3

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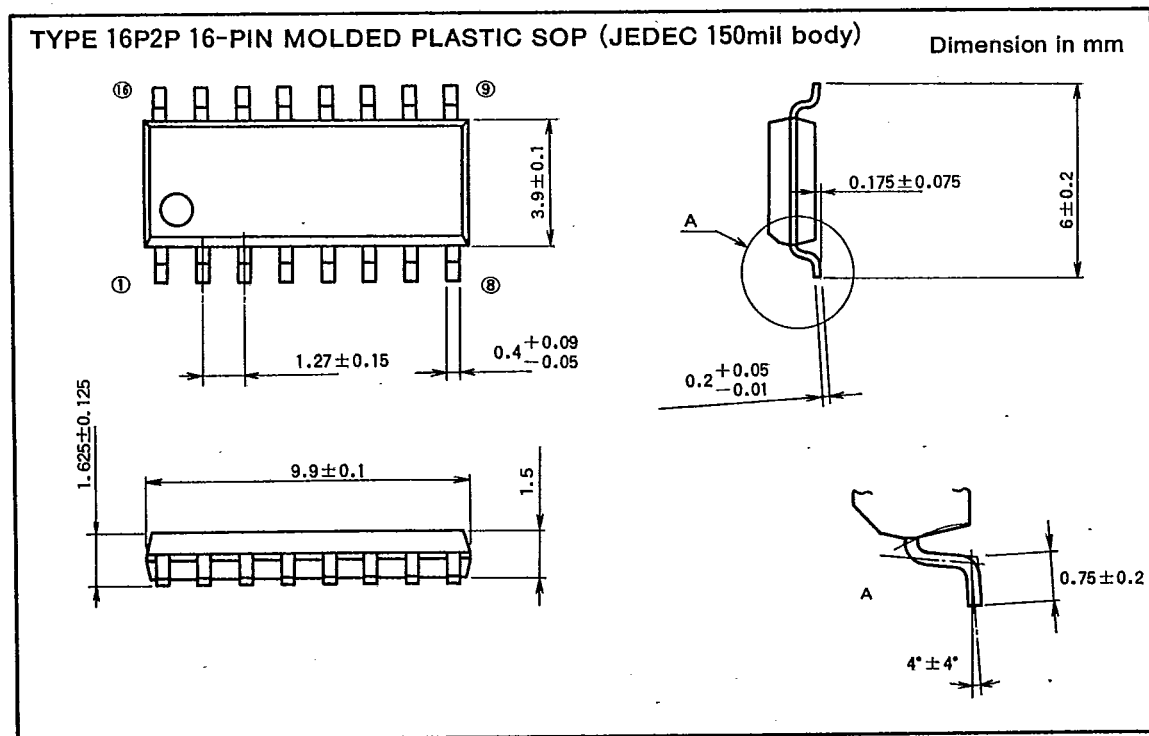
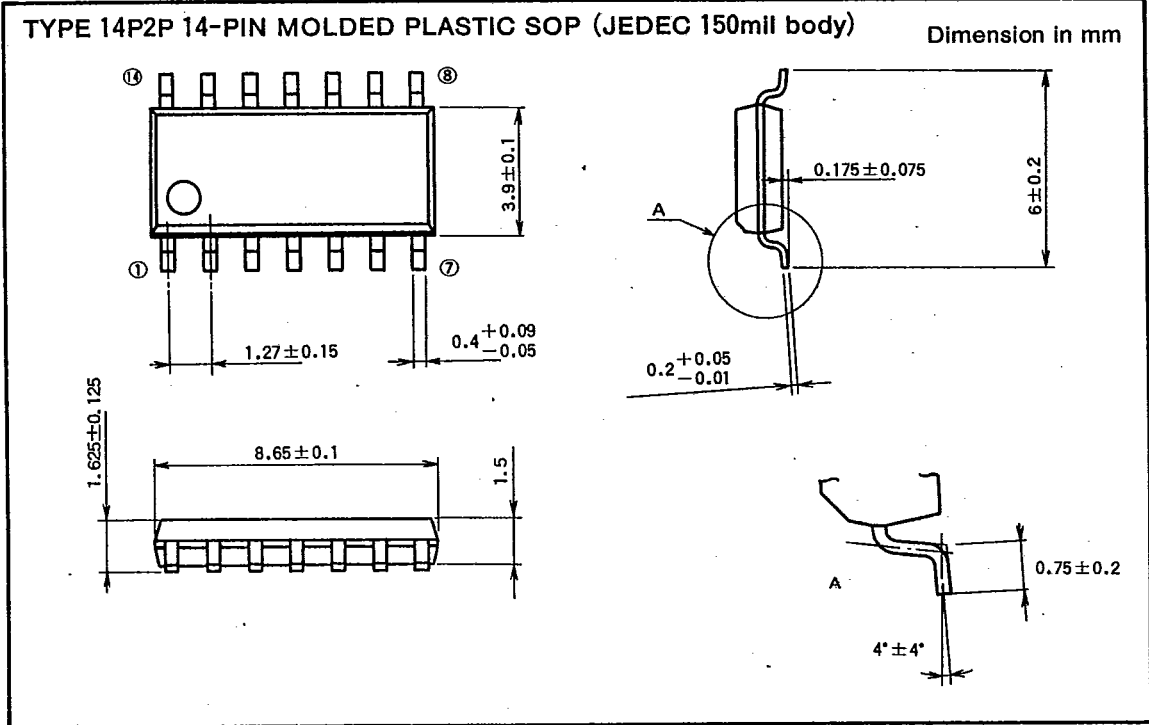
**DESCRIPTION**

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

MITSUBISHI ALSTTLs  
**PACKAGE OUTLINES**

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012786 0 ■ MIT3

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MITSUBISHI ALSTTLs  
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC) 9LD D ■ 6249827 0012787 2 ■ MIT3

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