

IT8266R

Jumper Free Over Clock Controller

Preliminary Specification V0.1.2

(For C Version)

ITE TECH. INC.



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Additional copies of this manual or other ITE literature may be obtained from:

ITE Tech. Inc. Tel: 886-2-29126889

Marketing Department Fax: 886-2-2910-2551, 886-2-2910-2552

7F, No.233-1, Baociao Rd., Sindian City, Taipei County 23145, Taiwan, ROC

If you have any marketing or sales questions, please contact:

P.Y. Chang, at ITE Taiwan:

E-mail: p.y.chang@ite.com.tw, Tel: 886-2-29126889 X6052, Fax: 886-2-29102551

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1. Features

- Six VID input (VIDIN0~5) and Six VID output (VIDOUT0~VIDOUT5) pins
 8 GPIO pins
- Supports Auto-Recovery; build-in watch-dog timer and reset output signal pin
- Provides CPU changing detect pin (SLOTOCC#)
- SM Bus interface
- 28 Pin SSOP





General Description

2. General Description

For acquiring better performance with lower cost, "Over-Clocking" gradually become a popular feature in the DIY market of PC motherboard. To do so, many interfaces such as PWM, CPU, chipset, clock generator, AGP, DIMM...etc on motherboard should be well handled.

Moreover, there is a trend to do "Jumperless" Over-Clocking in the motherboard design. For matching the trend, ITE develops a series of Jumper Free Over Clock Controllers targeted on different environments.

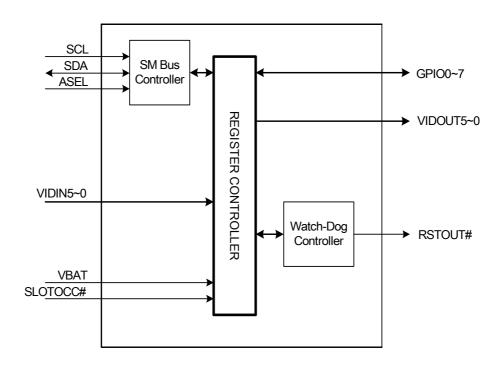
Generally, these controllers cover the following features:

- VID Interface and/or FID Interface handling
- GPIO
- Watch Dog Timers with Reset Signals for system auto-recovery from different situations
- CPU changing detection





3. Block Diagram



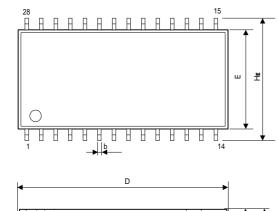


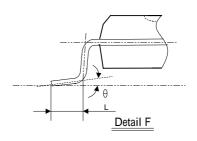


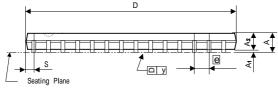
4. Package Information

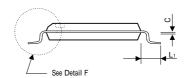
SSOP 28L Outline Dimensions

unit: inches/mm









Symbol	Dimension in inches			Dimension in mm		
Syllibol	Min	Nom	Max	Min	Nom	Max
Α	0.053	0.064	0.069	1.35	1.63	1.75
A1	0.004	0.006	0.010	0.10	0.152	0.25
A2	_	_	0.059	_	_	1.50
b	0.008	0.010	0.012	0.203	0.254	0.305
С	0.007	_	0.010	0.178	_	0.250
D	0.386	0.390	0.394	9.80	9.91	10.00
Е	0.150	0.154	0.157	3.80	3.91	4.00
е	0.025BSC			0.635BSC		
HE	0.228	0.236	0.244	5.80	5.99	6.20
L	0.016	0.025	0.050	0.40	0.635	1.27
L1	0.041REF.			1	.04REF	
S	0.033REF.			0	.838REI	F.
У	_	_	0.004	_	_	0.10
θ	O°	_	8°	O°	_	8°





Ordering Information

5. Ordering Information

Part No.	Package		
IT8266R	28 SSOP		

ITE also provides lead-free component. Please mark " -L " at the end of the Part No. when the parts ordered are lead-free.

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 (f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS
- PARAGRAPH 5 AND TO THEIR REASONABLENESS.

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