LSI/CSI

LS7083/7084

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# QUADRATURE CLOCK CONVERTER

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**FEATURES:**
- X1 and X4 mode selection
- Up to 16 MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +4.75V to +10.5V operation ($V_{DD}$-$V_{SS}$)
- 8-Pin DIP (SOIC available)

**DESCRIPTION:**
The LS7083 and LS7084 are monolithic CMOS silicon gate quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the LS7083/LS7084, are converted to strings of Up Clocks and Down Clocks (LS7083) or to a Clock and an Up/Down direction control (LS7084). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

**INPUT/OUTPUT DESCRIPTION:**

**RBIAS (Pin 1)**
Input for external component connection. A resistor connected between this input and $V_{SS}$ adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A,B pulse separation ($T_{OW} \leq T_{PS}$).

**$V_{DD}$ (Pin 2)**
Supply Voltage positive terminal.

**$V_{SS}$ (Pin 3)**
Supply Voltage negative terminal.

**A (Pin 4)**
Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

**B (Pin 5)**
Quadrature Clock Input B. This input has a filter circuit identical to input A.

**X4/$\overline{X1}$ (Pin 6)**
This input selects between X1 and X4 modes of operation. A high-level selects X4 mode and a low-level selects the X1 mode. In X4 mode, an output pulse is generated for every transition at either A or B input. In X1 mode, an output pulse is generated in one combined A/B input cycle. (See Figure 2.)

**PIN ASSIGNMENT - TOP VIEW**
**STANDARD 8 PIN PLASTIC DIP**

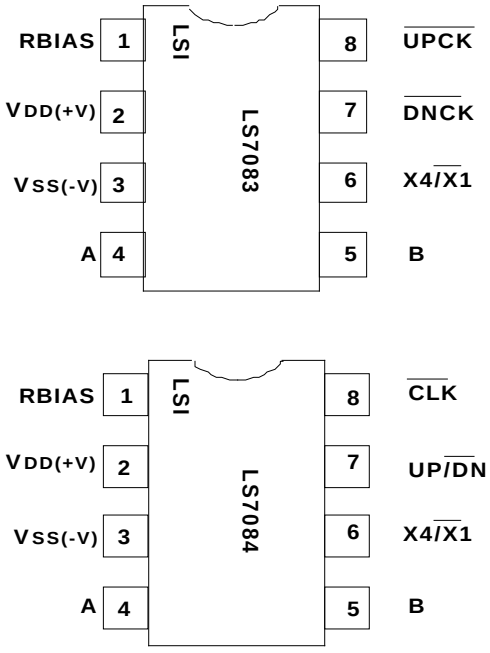


**FIGURE 1**

**LS7083 - $\overline{DNCK}$ (Pin 7)**
In LS7083, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

**LS7084 - UP/$\overline{DN}$ (Pin 7)**
In LS7084, this is the count direction indication output. When A input leads the B input, the UP/$\overline{DN}$ output goes high indicating that the count direction is UP. When A input lags the B input, UP/$\overline{DN}$ output goes low, indicating that the count direction is DOWN.

**LS7083 - $\overline{UPCK}$ (Pin 8)**
In LS7083, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

**LS7084 - $\overline{CLK}$ (Pin 8)**
In LS7084, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the UP/$\overline{DN}$ output (Pin7).

**NOTE**: For the LS7084, the timing of $\overline{CLK}$ and UP/$\overline{DN}$ requires that the counter interfacing with LS7084 counts on the rising edge of the $\overline{CLK}$ pulses.

**ABSOLUTE MAXIMUM RATINGS:**

| PARAMETER | SYMBOL | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ - $V_{SS}$ | 12 | V |
| Voltage at any input | $V_{IN}$ | $V_{SS}$ -.3 to $V_{DD}$ +.3 | V |
| Operating temperature | $T_A$ | 0 to +70 | °C |
| Storage temperature | $T_{STG}$ | -55 to +150 | °C |

**DC ELECTRICAL CHARACTERISTICS:**

(All voltages referenced to $V_{SS}$, $T_A$ = 0°C to 70°C.)

| PARAMETER | SYMBOL | MIN | MAX | UNITS | CONDITION |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 4.75 | 10.5 | V | - |
| Supply current | $I_{DD}$ | - | 6.0 | µA | $V_{DD}$ = 10.5V, All input frequencies = 0 Hz RBIAS = 2MΩ |
| **X4/$\overline{X1}$** Logic Low | $V_{IL}$ | - | | 0.3$V_{DD}$ | V |
| **A,B** Logic Low | $V_{IL}$ | - | 0.6 | V | $V_{DD}$ = 4.75V |
| | | - | 1.0 | V | $V_{DD}$ = 9V |
| | | - | 1.1 | V | $V_{DD}$ = 10.5V |
| **X4/X1** Logic High | $V_{IH}$ | 0.7$V_{DD}$ | - | V | - |
| **A,B** Logic High | $V_{IH}$ | 3.1 | - | V | $V_{DD}$ = 4.75V |
| | | 5.0 | - | V | $V_{DD}$ = 9V |
| | | 5.6 | - | V | $V_{DD}$ = 10.5V |
| **ALL OUTPUTS:** | | | | | |
| Sink Current | $I_{OL}$ | 1.75 | - | mA | $V_{DD}$ = 4.75V |
| $V_{OL}$ = 0.4V | | 5.0 | - | mA | $V_{DD}$ = 9V |
| | | 5.7 | - | mA | $V_{DD}$ = 10.5V |
| Source Current | $I_{OH}$ | 1.0 | - | mA | $V_{DD}$ = 4.75V |
| $V_{OH}$ = $V_{DD}$ - 0.5V | | 2.5 | - | mA | $V_{DD}$ = 9V |

**TRANSIENT CHARACTERISTICS:**

($T_A$ = 0°C to 70°C)

| PARAMETER | SYMBOL | MIN | MAX | UNITS | CONDITION |
|---|---|---|---|---|---|
| **A,B** inputs: | | | | | |
| Validation Delay | $T_{VD}$ | - | 85 | ns | $V_{DD}$ = 10.5V |
| | | - | 100 | ns | $V_{DD}$ = 9V |
| | | - | 160 | ns | $V_{DD}$ = 4.75V |
| **A,B** inputs: | | | | | |
| Pulse Width | $T_{PW}$ | $T_{VD}$+$T_{OW}$ | Infinite | ns | - |
| **A to B** or **B to A** | | | | | |
| Phase Delay | $T_{PS}$ | $T_{OW}$ | Infinite | ns | - |
| **A,B** frequency | $f_{A,B}$ | - | $\frac{1}{2T_{PW}}$ | Hz | $T_{OW}$ < $T_{DD}$ |
| | | - | $\frac{1}{4T_{OW}}$ | Hz | $T_{OW}$ ≥ $T_{DD}$ |
| Input to Output Delay | $T_{DS}$ | - | 120 | ns | $V_{DD}$ = 10.5V |
| | | - | 150 | ns | $V_{DD}$ = 9V |
| | | - | 235 | ns | $V_{DD}$ = 4.75V Includes input validation delay |
| Output Clock Pulse Width | $T_{OW}$ | 50 | - | ns | See Fig. 4 & 5 |

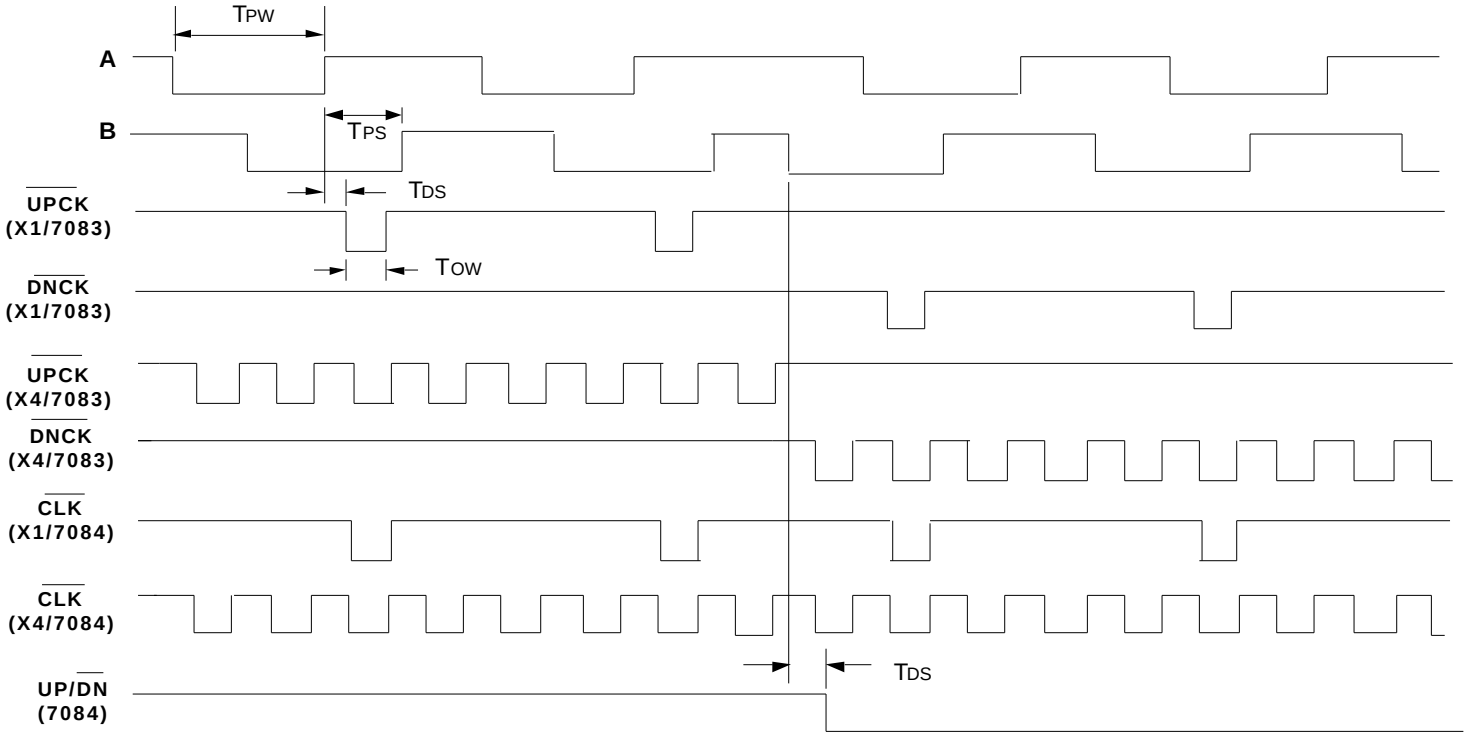


**FIGURE 2. LS7083/LS7084 INPUT/OUTPUT TIMING DIAGRAM**

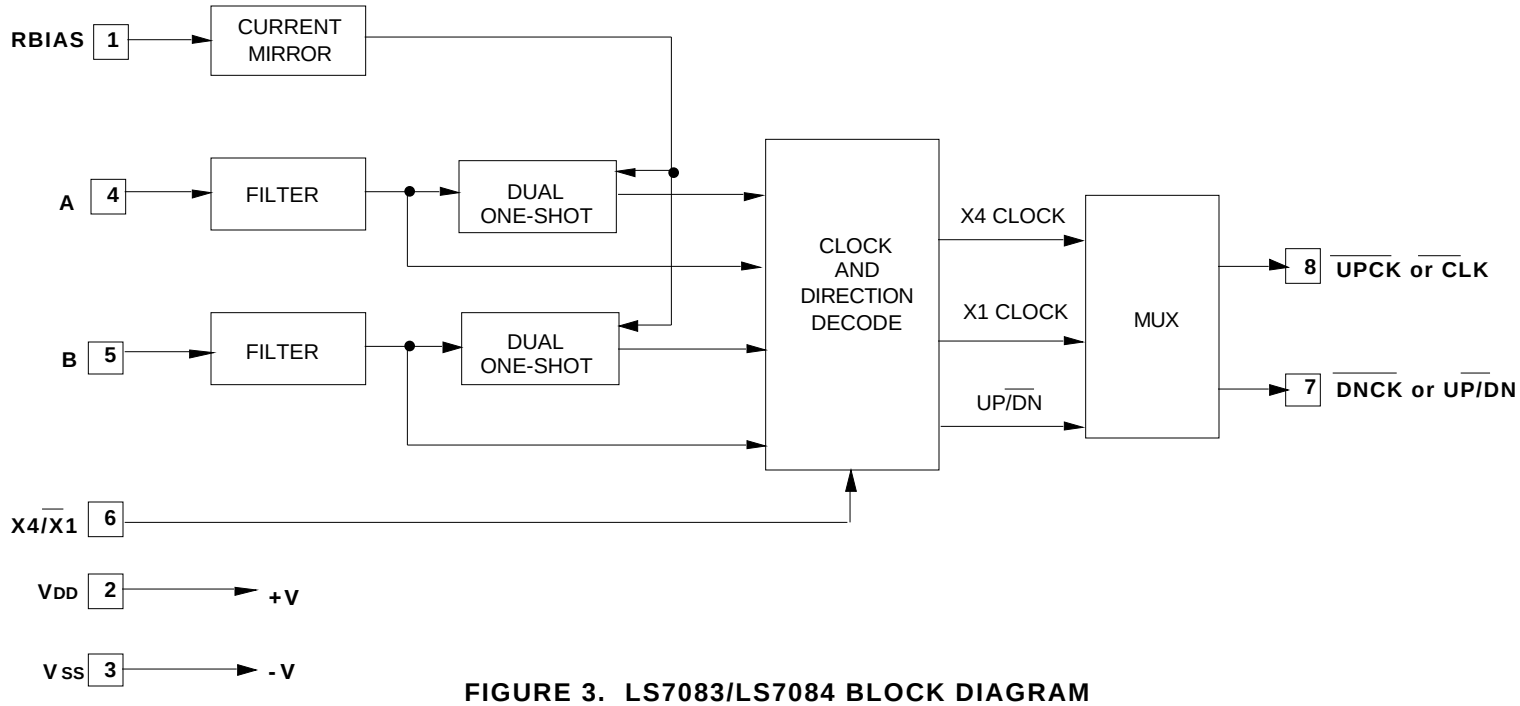


**FIGURE 3. LS7083/LS7084 BLOCK DIAGRAM**

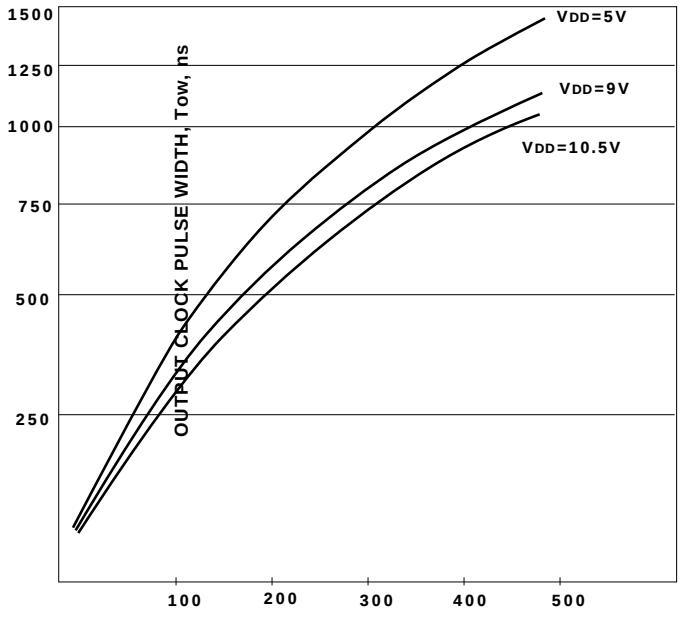


Figure 4. Tow vs RBIAS, KΩ

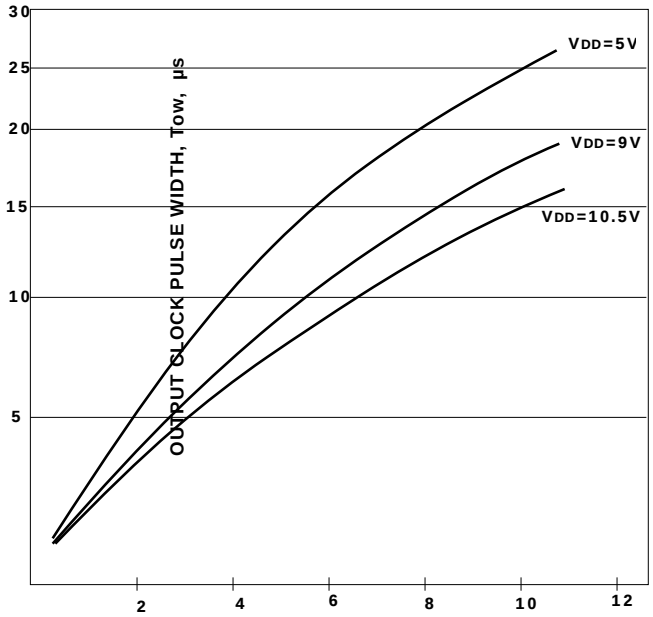


Figure 5. Tow vs RBIAS, MΩ

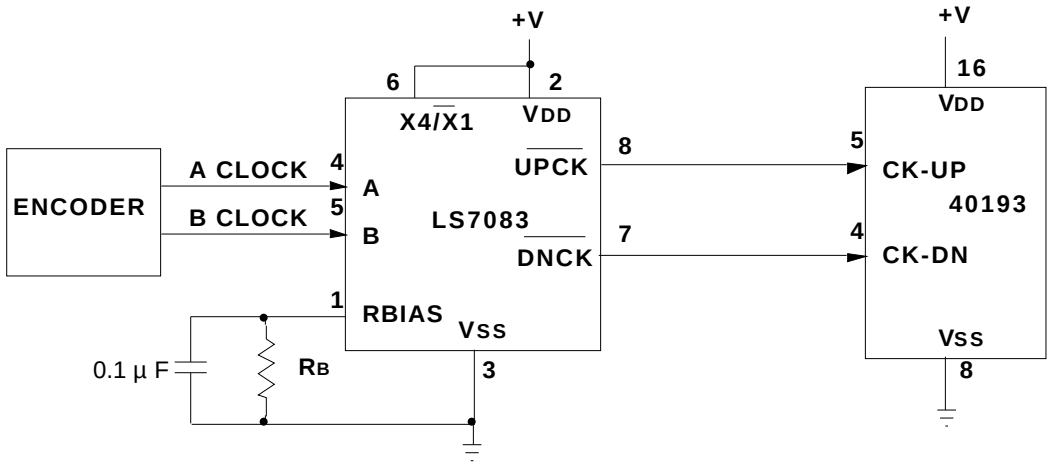


**FIGURE 6A.**
**TYPICAL APPLICATION FOR LS7083 IN X4 MODE**

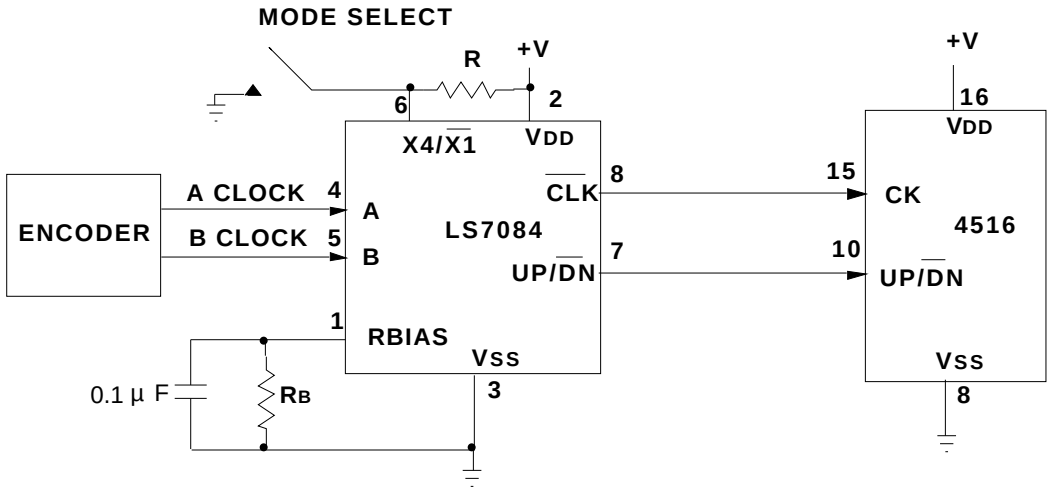


**FIGURE 6B.**
**TYPICAL APPLICATION FOR LS7084 WITH X4/X1 MODE SELECTION**