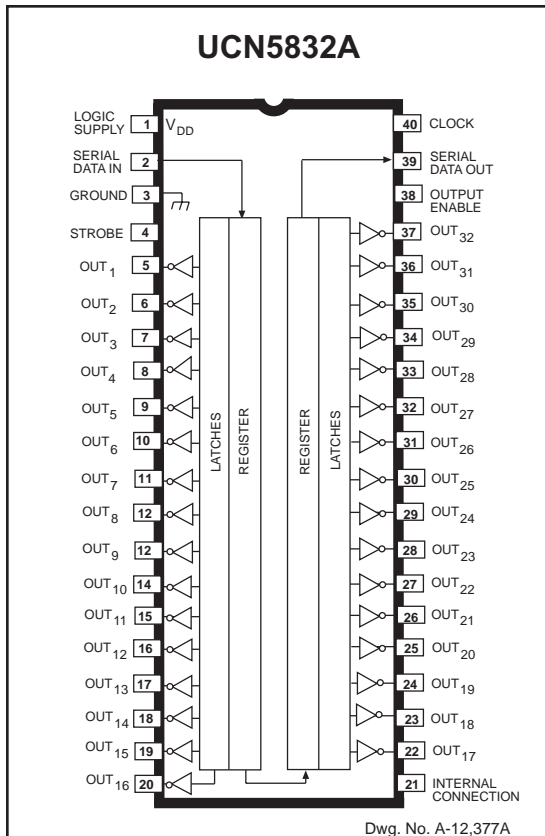


BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS



ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT}	40 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3 V$
Continuous Output Current, I_{OUT}	150 mA
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	-20°C to +85°C
Storage Temperature Range, T_S	-55°C to +150°C

Caution: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Intended originally to drive thermal printheads, the UCN5832A and UCN5832EP have been optimized for low output-saturation voltage, high-speed operation, and pin configurations most convenient for the tight space requirements of high-resolution printheads. These integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. The combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar NPN open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. MOS serial data outputs permit cascading for interface applications requiring additional drive lines.

The UCN5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, this device will allow all outputs to sustain 100 mA continuously without derating. The UCN5832EP is supplied in a 44-lead plastic leaded chip carrier for minimum area, surface-mount applications. Both devices are also available for operation from -40°C to +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

Similar 32-bit serial-input latched source drivers are available as the UCN5818AF/EPF. Other high-voltage, high-current 8-bit devices are available as the UCN5821A, UCN5841A/LW, and UCN5842A.

FEATURES

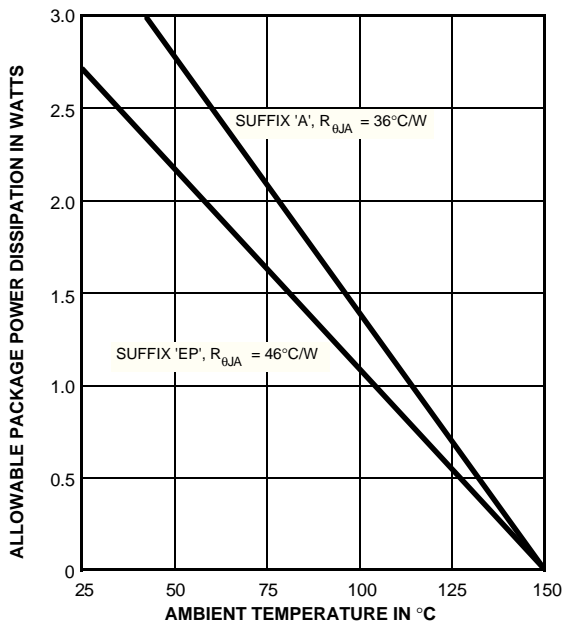
- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current Sink Outputs
- Low Saturation Voltage
- Automotive Capable

Always order by complete part number:

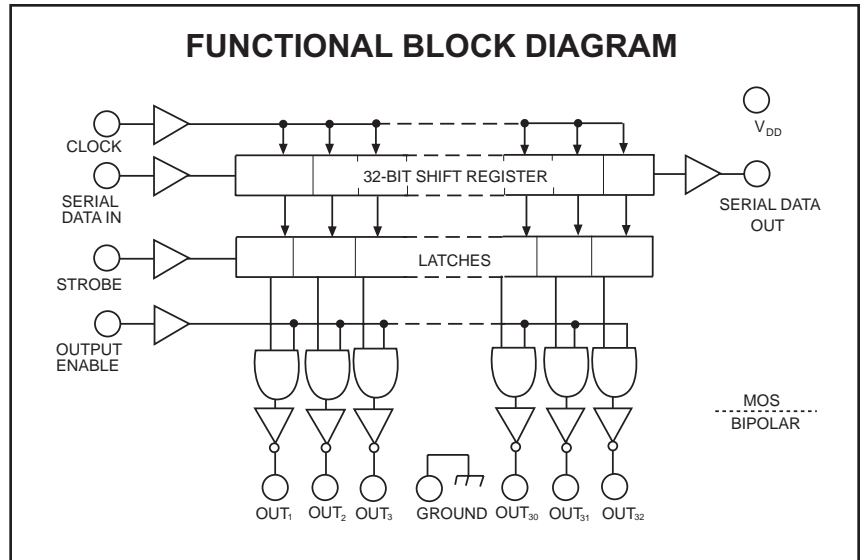
Part Number	Package
UCN5832A	40-Pin DIP
UCN5832EP	44-Lead PLCC

5832

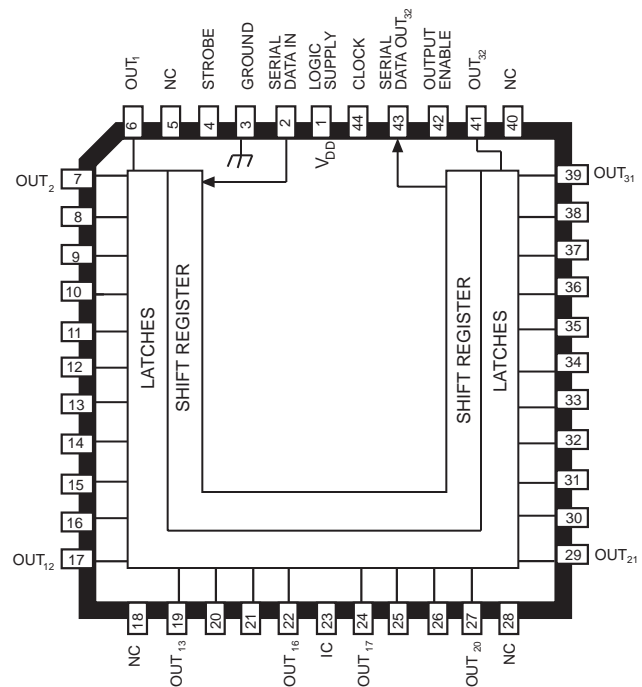
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. GP-025A



UCN5832EP



Dwg. No. A-14,360



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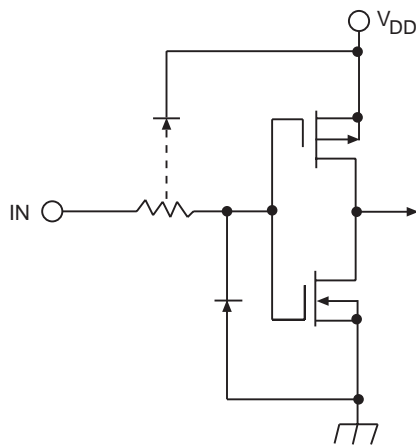
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 40\text{ V}$, $T_A = 70^\circ\text{C}$	—	10	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50\text{ mA}$	—	275	mV
		$I_{OUT} = 100\text{ mA}$, "A" package	150	550	mV
		$I_{OUT} = 100\text{ mA}$, "EP" package	—	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 3.5\text{ V}$	—	1.0	μA
	$I_{IN(0)}$	$V_{IN} = 0.8\text{ V}$	—	-1.0	μA
Input Impedance	Z_{IN}	$V_{IN} = 3.5\text{ V}$	3.5	—	$\text{M}\Omega$
Serial Data Output Resistance	R_{OUT}		—	20	$\text{k}\Omega$
Supply Current	I_{DD}	One output ON, $I_{OUT} = 100\text{ mA}$	—	5.0	mA
		All outputs OFF	—	50	μA
Output Rise Time	t_r	$I_{OUT} = 100\text{ mA}$, 10% to 90%	—	1.0	μs
Output Fall Time	t_f	$I_{OUT} = 100\text{ mA}$, 90% to 10%	—	1.0	μs

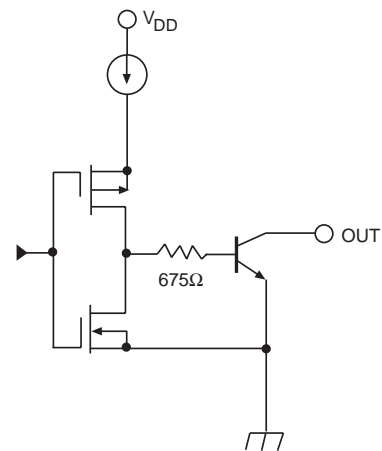
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,379A

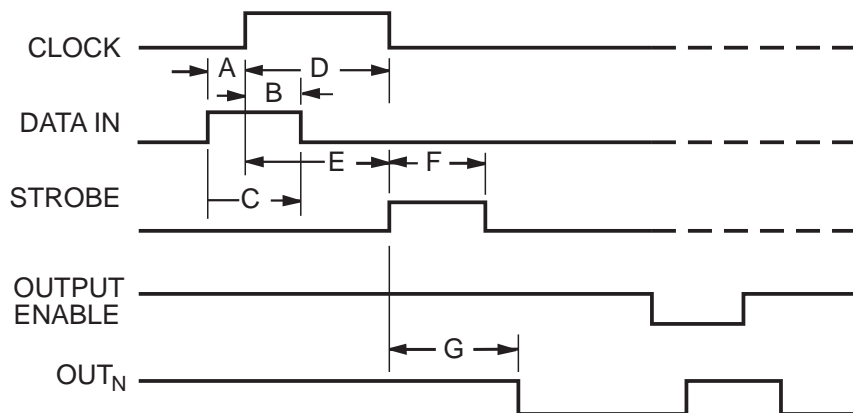
TYPICAL OUTPUT DRIVER



Dwg. No. A-12,380A

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BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. No. A-12,276A

TIMING CONDITIONS

($V_{DD} = 5.0\text{ V}$, Logic Levels are V_{DD} and Ground)

- A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) **75 ns**
- B. Minimum Data Active Time After Clock Pulse (Data Hold Time) **75 ns**
- C. Minimum Data Pulse Width **150 ns**
- D. Minimum Clock Pulse Width **150 ns**
- E. Minimum Time Between Clock Activation and Strobe **300 ns**
- F. Minimum Strobe Pulse Width **100 ns**
- G. Typical Time Between Strobe Activation and Output Transition **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

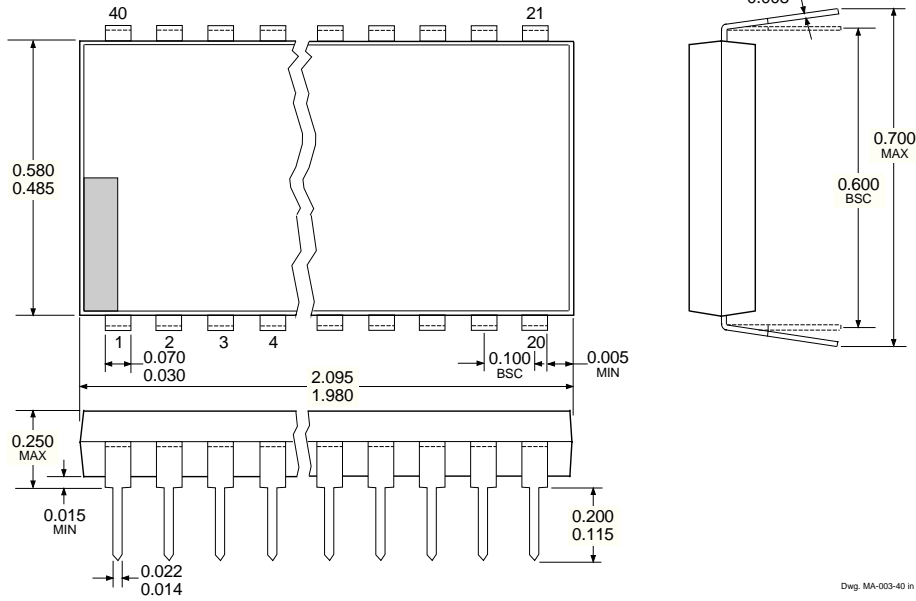
Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable Input	Output Contents					
		I ₁	I ₂	I ₃	...	I _{N-1}	I _N			O ₁	O ₂	O ₃	...	O _{N-1}	O _N		O ₁	O ₂	O ₃	...	O _{N-1}	O _N
H	┌	H	R ₁	R ₂	...	R _{N-2}	R _{N-1}	R _{N-1}														
L	└	L	R ₁	R ₂	...	R _{N-2}	R _{N-1}	R _{N-1}														
X	┐	R ₁	R ₂	R ₃	...	R _{N-1}	R _N	R _N														
		X	X	X	...	X	X	X	L	R ₁	R ₂	R ₃	...	R _{N-1}	R _N							
		P ₁	P ₂	P ₃	...	P _{N-1}	P _N	P _N	H	P ₁	P ₂	P ₃	...	P _{N-1}	P _N	H						
					...					X	X	X	...	X	X	L	H	H	H	...	H	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



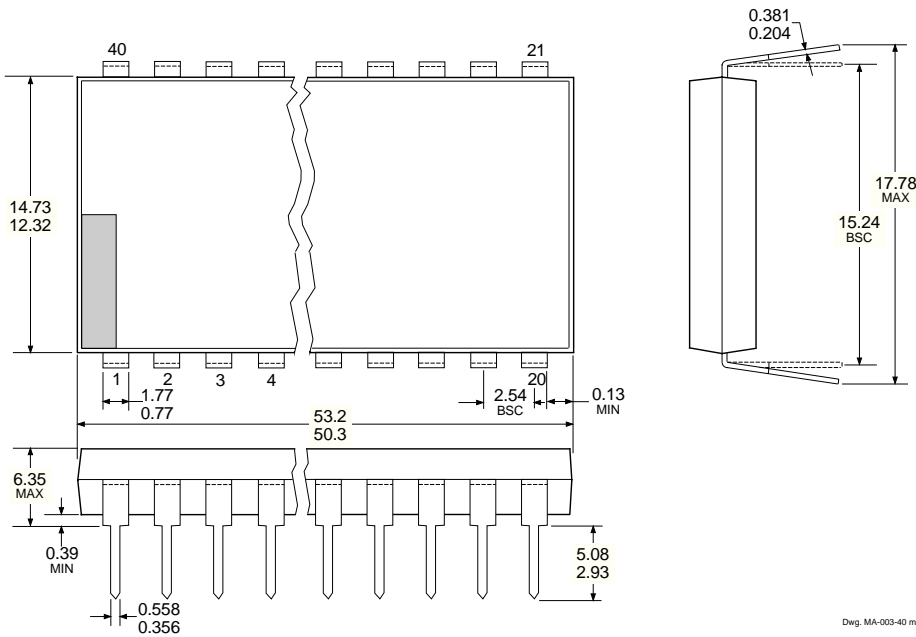
5832
BiMOS II 32-BIT
SERIAL-INPUT,
LATCHED DRIVERS

UCN5832A
 Dimensions in Inches
 (controlling dimensions)



Dwg. MA-003-40 in

Dimensions in Millimeters
 (for reference only)



Dwg. MA-003-40 mm

- NOTES: 1. Lead thickness is measured at seating plane or below.
 2. Lead spacing tolerance is non-cumulative.
 3. Exact body and lead configuration at vendor's option within limits shown.

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***BiMOS II 32-BIT
SERIAL-INPUT,
LATCHED DRIVERS***

5832
BiMOS II 32-BIT
SERIAL-INPUT,
LATCHED DRIVERS

BiMOS II (Series 5800) & DABiC IV (Series 6800)
INTELLIGENT POWER INTERFACE DRIVERS
SELECTION GUIDE

Function	Output Ratings *		Part Number †
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
9-Bit	1.6 A	50 V	5829
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
SPECIAL-PURPOSE FUNCTIONS			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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