Bt106

50 MHz Monolithic CMOS Single 8-bit VIDEODAC™

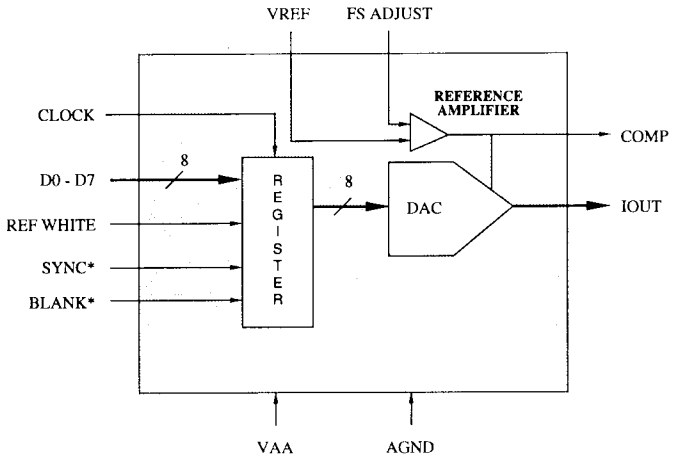
Distinguishing Features

- 50, 30 MHz Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170-Compatible Output
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 20-pin DIP Package
- Typical Power Dissipation: 400 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Functional Block Diagram



Product Description

The Bt106 is an 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog output to the reference white level, regardless of the data inputs.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt106 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load, and RS-170-compatible video signals into a singly- terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1 LSB over the full temperature range.

6

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L106001 Rev. H

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt106 contains an 8-bit D/A converter, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown in Figure 1, 8 bits of data are latched into the device and presented to the 8-bit D/A converter. The REF WHITE input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog output, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output level.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 Ω for generation of RS-343A video into a 37.5 Ω load. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and should provide a low-impedance output.

The D/A converter on the Bt106 uses a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt106 can directly drive a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

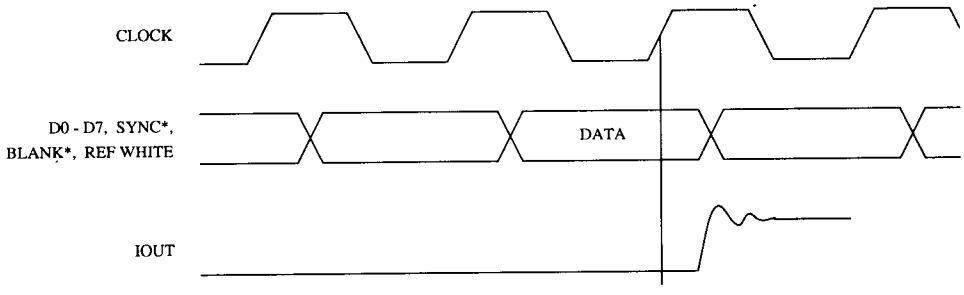
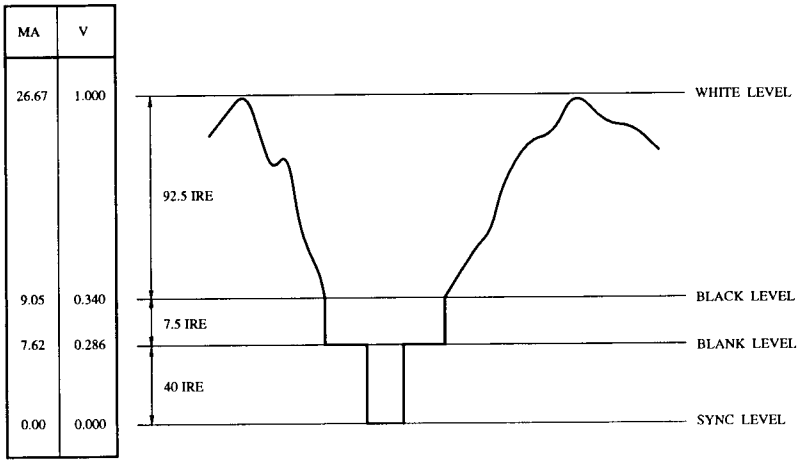


Figure 1. Input/Output Timing.

Circuit Description *(continued)*



Note: 75 Ω doubly-terminated load, RSET = 542 Ω, and VREF = 1.2 V. RS-343A levels and tolerances are assumed on all levels.

Figure 2. Composite Video Output Waveform.

6

Description	IOUT (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	1	$xx
WHITE	26.67	0	1	1	$FF
DATA	data + 9.05	0	1	1	data
DATA - SYNC	data + 1.44	0	0	1	data
BLACK	9.05	0	1	1	$00
BLACK - SYNC	1.44	0	0	1	$00
BLANK	7.62	x	1	0	$xx
SYNC	0	x	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 542 Ω and VREF = 1.2 V.

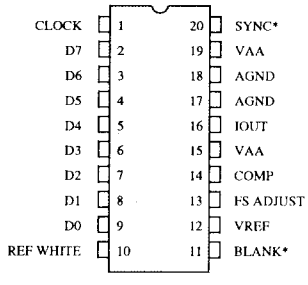
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOUT output to the blanking level, as specified in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0–D7 and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the output (see Figure 2). SYNC* does not override any other control or data input, as specified in Table 1; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the output to the white level, regardless of the D0–D7 inputs. It is latched on the rising edge of CLOCK (see Table 1).
D0–D7	Data inputs (TTL compatible). D0 is the least significant data bit. D0–D7 are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the D0–D7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOUT	Current output. This high-impedance current source can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 3).
AGND	Analog ground. All AGND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
FSADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). The IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: RSET (Ω) = 12,046 * VREF (V) / IOUT (mA)

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as that shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The Bt106 has an internal pullup resistor between VAA and VREF. As the value of this resistor may vary slightly because of process variations, the use of a resistor network to generate the reference is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to AGND, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.



6

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt106 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated VIDEODAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt106 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt106 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt106. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each VAA pin to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 3 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

To optimize the settling time of the Bt106, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time. An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

The COMP pin and series resistor must also be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

To reduce low-frequency supply noise a larger COMP capacitor value may be required.

PC Board Layout Considerations *(continued)*

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt106 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt106 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the VIDEODAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Analog Signal Interconnect

The Bt106 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt106 to minimize reflections. Unused analog outputs should be connected to GND.

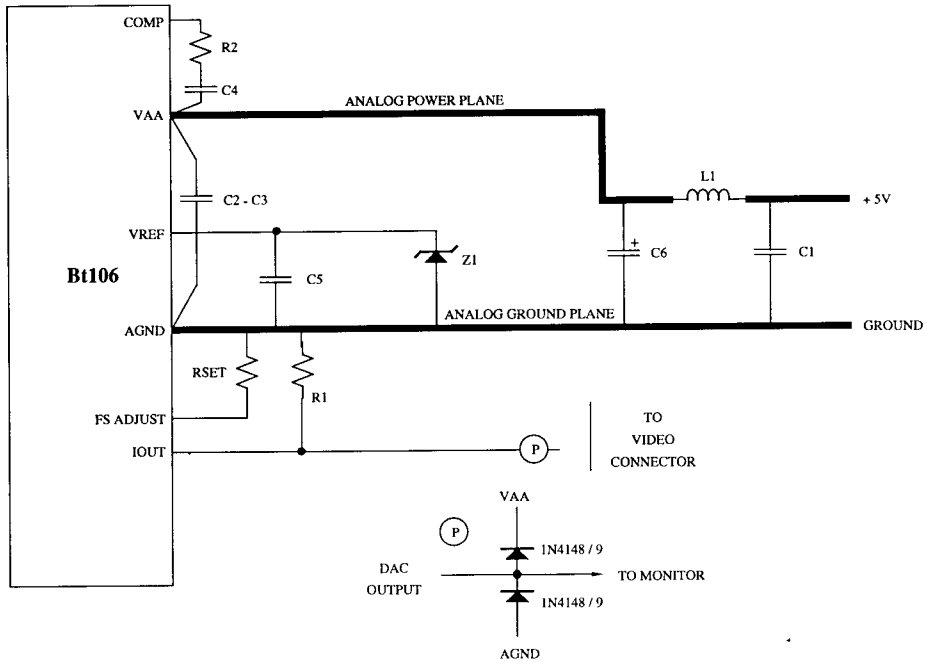
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt106 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	12 Ω 1% metal film resistor	Dale CMF-55C
RSET	542 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt106.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170-compatible video, it is recommended that a singly-terminated 75 Ω load be used with an RSET value of about 774 Ω. If the Bt106 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75 Ω and singly-terminated 75 Ω loads.

If the user is driving a large capacitive load [i.e., if load RC > 1/(20 fcπ) (where fc = clock frequency)], it is recommended that an output buffer be used to drive a doubly-terminated 75 Ω load.

Color Applications

In color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may be logical zeros. If SYNC* is always logical zeros, the relationship between RSET and the full-scale output current is:

$$IOUT\ (mA) = 8{,}604 * VREF\ (V) / RSET\ (\Omega)$$

Using Multiple Devices

If they are close together on the same PC board, multiple Bt106 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt106 must still have its own RSET resistor, IOUT termination resistor (R1 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R2 in Figure 3).

Nonvideo Applications

The Bt106 may be used in nonvideo applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be logical zeros and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$RSET\ (\Omega) = 7{,}958 * VREF\ (V) / IOUT\ (mA)$$

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$Imin\ (mA) = 650 * VREF\ (V) / RSET\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a force-to-full-scale control.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA				
Bt106KC30		0		+70	°C
Bt106BC		–25		+85	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.14	1.20	1.26	V
FS ADJUST Resistor	RSET		542		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	V
Voltage on Any Signal Pin (Note 1)		AGND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	AGND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	–0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω and VREF = 1.200 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

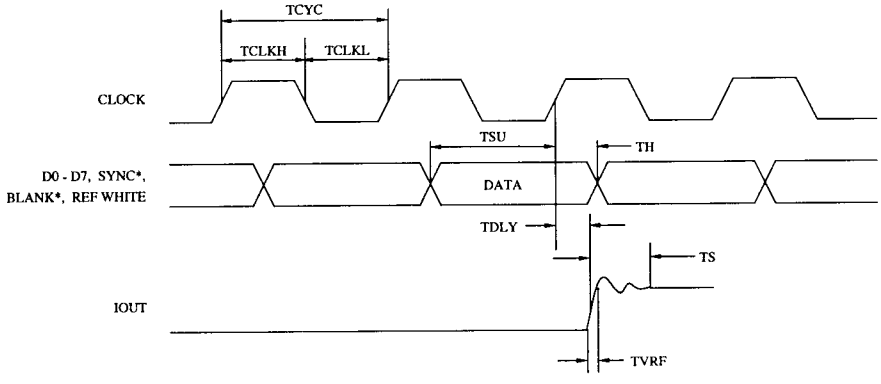
Parameter	Symbol	50 MHz Devices			30 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time Data and Control Hold Time	TSU TH	8 2			8 2			ns ns
Clock Cycle Time Clock Pulse Width High Time Clock Pulse Width Low Time	TCYC TCLKH TCLKL	20 8 8			33.3 10 10			ns ns ns
Analog Output Delay Analog Output Rise/Fall Time Analog Output Settling Time (Note 1) Clock and Data Feedthrough (Note 1) Glitch Impulse (Note 1)	TDLY TVRF TS		25 20 –33 50	8		25 25 –33 50	9	ns ns ns dB pV - sec
Differential Gain Error Differential Phase Error	DG DP		1.8 1.2			1.8 1.2		% Gray Scale Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current (Note 2)	IAA		80	100		60	75	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω and VREF = 1.200 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. COMP resistor = 12 Ω. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

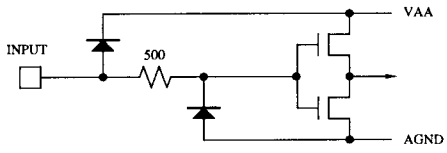
Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 4. Input/Output Timing.

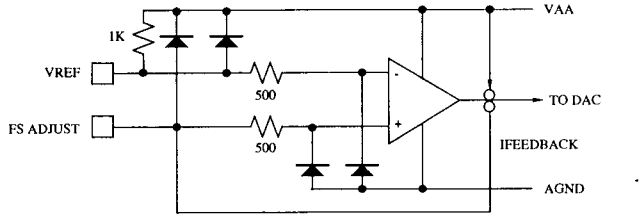
6

Ordering Information

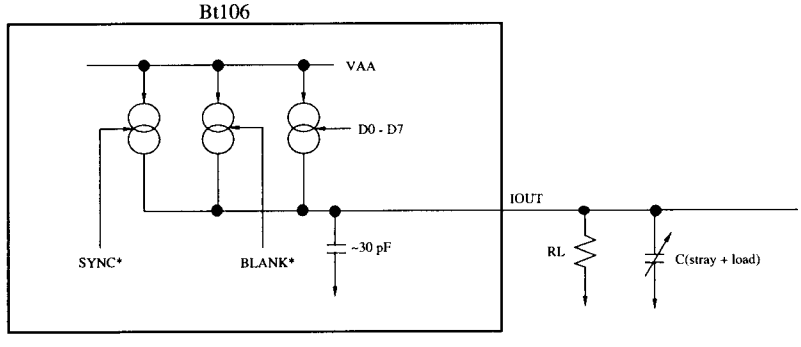
Model Number	Speed	Package	Ambient Temperature Range
Bt106BC	50 MHz	20-pin 0.3" CERDIP	–25° to +85° C
Bt106KC30	30 MHz	20-pin 0.3" CERDIP	0° to +70° C
Bt106EVM	Evaluation Board for the Bt106		



Equivalent Circuit of the Digital Inputs.



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output.