TMS320VC5510/5510A Fixed-Point Digital Signal Processors

Data Manual

Literature Number: SPRS076O
June 2000 − Revised September 2007

TEXAS INSTRUMENTS

This page intentionally left blank

REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS076N device-specific data sheet to make it an SPRS076O revision.

PAGE(s) NO.	ADDITIONS/CHANGES/DELETIONS
27	Section 3.2.1 System Register (SYSR), Table 3−5, System Register (SYSR) Bit Functions: Added $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ to “Enables the internal pullups on the . . .” sentence in the HPE function description.

Contents

Section Page

List of Figures

List of Tables

1 Features

- **High-Performance, Low-Power, Fixed-Point TMS320C55x™ Digital Signal Processor (DSP)**
  - **6.25-/5-ns Instruction Cycle Time**
  - **160-/200-MHz Clock Rate**
  - **One/Two Instructions Executed per Cycle**
  - **Dual Multipliers (Up to 400 Million Multiply-Accumulates Per Second (MMACS))**
  - **Two Arithmetic/Logic Units**
  - **One Internal Program Bus**
  - **Three Internal Data/Operand Read Buses**
  - **Two Internal Data/Operand Write Buses**
- **Instruction Cache (24K Bytes)**
- **160K x 16-Bit On-Chip RAM Composed of:**
  - **Eight Blocks of 4K × 16-Bit Dual-Access RAM (DARAM) (64K Bytes)**
  - **32 Blocks of 4K × 16-Bit Single-Access RAM (SARAM) (256K Bytes)**
- **16K × 16-Bit On-Chip ROM (32K Bytes)**
- **8M × 16-Bit Maximum Addressable External Memory Space**
- **32-Bit External Memory Interface (EMIF) With Glueless Interface to:**
  - **Asynchronous Static RAM (SRAM)**
  - **Asynchronous EPROM**
  - **Synchronous DRAM (SDRAM)**
  - **Synchronous Burst SRAM (SBSRAM)**
- **Programmable Low-Power Control of Six Device Functional Domains**
- **On-Chip Peripherals**
  - **Two 20-Bit Timers**
  - **Six-Channel Direct Memory Access (DMA) Controller**
  - **Three Multichannel Buffered Serial Ports (McBSPs)**
  - **16-Bit Parallel Enhanced Host-Port Interface (EHPI)**
  - **Programmable Digital Phase-Locked Loop (DPLL) Clock Generator**
  - **Eight General-Purpose I/O (GPIO) Pins and Dedicated General-Purpose Output (XF)**
- **On-Chip Scan-Based Emulation Logic**
- **IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **240-Terminal MicroStar BGA™ (Ball Grid Array) (GGW Suffix)**
- **240-Terminal MicroStar BGA™ (Ball Grid Array) (ZGW Suffix) [Lead-Free]**
- **3.3-V I/O Supply Voltage**
- **1.6-V Core Supply Voltage**

TMS320C55x and MicroStar BGA are trademarks of Texas Instruments.
Other trademarks are the property of their respective owners.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

2 Introduction

This section describes the main features of the TMS320VC5510/5510A digital signal processors (DSPs), lists the pin assignments, and describes the function of each pin. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

NOTE: This data manual is designed to be used in conjunction with the *TMS320C55x™ DSP Functional Overview* (literature number SPRU312).

2.1 Description

The TMS320VC5510/5510A (5510/5510A) fixed-point digital signal processors (DSPs) are based on the TMS320C55x DSP generation CPU processor core. The C55x™ DSP architecture achieves high performance and low power through increased parallelism and total focus on reduction in power dissipation. The CPU supports an internal bus structure composed of one program bus, three data read buses, two data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to three data reads and two data writes in a single cycle. In parallel, the DMA controller can perform up to two data transfers per cycle independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the address unit (AU) and data unit (DU) of the C55x CPU.

The C55x™ DSP generation supports a variable byte width instruction set for improved code density. The instruction unit (IU) performs 32-bit program fetches from internal or external memory and queues instructions for the program unit (PU). The program unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions. The 5510/5510A also includes a 24K-byte instruction cache to minimize external memory accesses, improving data throughput and conserving system power.

The 5510/5510A peripheral set includes an external memory interface (EMIF) that provides glueless access to asynchronous memories like EPROM and SRAM, as well as to high-speed, high-density memories such as synchronous DRAM and synchronous burst SRAM. Three full-duplex multichannel buffered serial ports (McBSPs) provide glueless interface to a variety of industry-standard serial devices, and multichannel communication with up to 128 separately enabled channels. The enhanced host-port interface (EHPI) is a 16-bit parallel interface used to provide host processor access to internal memory on the 5510/5510A. The EHPI can be configured in either multiplexed or non-multiplexed mode to provide glueless interface to a wider variety of host processors. The DMA controller provides data movement for six independent channel contexts without CPU intervention, providing DMA throughput of up to two 16-bit words per cycle. Two general-purpose timers, eight general-purpose I/O (GPIO) pins, and digital phase-locked loop (DPLL) clock generation are also included.

The 5510/5510A is supported by the industry's leading eXpressDSP™ software environment including the Code Composer Studio™ integrated development environment, DSP/BIOS™ software kernel foundation, the TMS320™ DSP Algorithm Standard, and the industry's largest third-party network. Code Composer Studio features code generation tools including a C-Compiler, Visual Linker, simulator, Real-Time Data Exchange (RTDX™), XDS510™ emulation device drivers, and Chip Support Libraries (CSL). DSP/BIOS is a scalable real-time software foundation available for no cost to users of Texas Instruments' DSP products providing a pre-emptive task scheduler and real-time analysis capabilities with very low memory and megahertz overhead. The TMS320 DSP Algorithm Standard is a specification of coding conventions allowing fast integration of algorithms from different teams, sites, or third parties into the application framework. Texas Instruments' extensive DSP third-party network of over 400 providers brings focused competencies and complete solutions to customers.

Texas Instruments (TI) has also developed foundation software available for the 5510/5510A. The C55x DSP Library (DSPLIB) features over 50 C-callable software kernels (FIR/IIR filters, Fast Fourier Transforms (FFTs), and various computational functions). The DSP Image/Video Processing Library (IMGLIB) contains over 20 software kernels highly optimized for C55x DSPs and is compiled with the latest revision of the C55x DSP code generation tools. These imaging functions support a wide range of applications that include compression, video processing, machine vision, and medical imaging.

The TMS320C55x DSP core was created with an open architecture that allows the addition of application-specific hardware to boost performance on specific algorithms. The hardware extensions on the 5510/5510A strike the perfect balance of fixed function performance with programmable flexibility, while achieving low-power consumption, and cost that traditionally has been difficult to find in the video-processor market. The extensions allow the 5510/5510A to deliver exceptional video codec performance with more than half its bandwidth available for performing additional functions such as color space conversion, user-interface operations, security, TCP/IP, voice recognition, and text-to-speech conversion. As a result, a single 5510/5510A DSP can power most portable digital video applications with processing headroom to spare. For more information, see the *TMS320C55x Hardware Extensions for Image/Video Applications Programmer's Reference* (literature number SPRU098). For more information on using the the DSP Image Processing Library, see the *TMS320C55x Image/Video Processing Library Programmer's Reference* (literature number SPRU037).

2.2 Pin Assignments

Figure 2−1 illustrates the ball locations for the 240-pin GGW and ZGW ball grid array (BGA) packages and is used in conjunction with Table 2−1 to locate signal names and ball grid numbers.

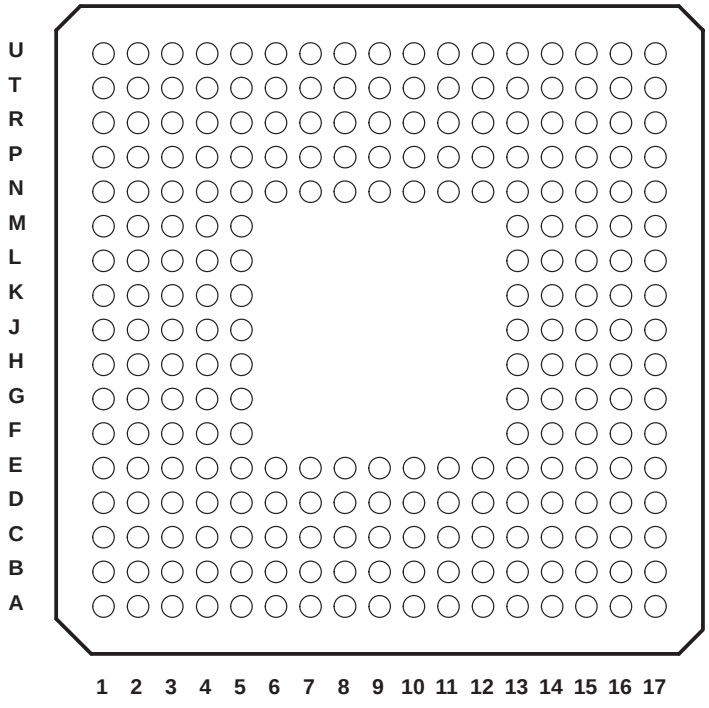


Figure 2−1. TMS320VC5510/5510A GGW and ZGW MicroStar BGA™ Packages (Bottom View)

Table 2−1. Pin Assignments

BGA BALL #	SIGNAL	BGA BALL #	SIGNAL	BGA BALL #	SIGNAL	BGA BALL #	SIGNAL
A1	V_{SS}	A2	A9	A3	DV_{DD}	A4	A8
A5	CV_{DD}	A6	A4	A7	DV_{DD}	A8	D2
A9	V_{SS}	A10	V_{SS}	A11	$\overline{SDRAS}$	A12	DV_{DD}
A13	$\overline{SDCAS}$	A14	CV_{DD}	A15	HD10	A16	V_{SS}
A17	V_{SS}	B1	V_{SS}	B2	XF	B3	D9
B4	D7	B5	D5	B6	D3	B7	A2
B8	A0	B9	CLKMEM	B10	SDA10	B11	HD2
B12	$\overline{SDWE}$	B13	$\overline{HD1}$	B14	HDRY	B15	HD3
B16	HD0	B17	$\overline{HDS1}$	C1	A10	C2	D13
C3	D10	C4	A6	C5	A7	C6	A5
C7	A3	C8	D0	C9	HD4	C10	HD5
C11	HD6	C12	HD7	C13	HD8	C14	HD9
C15	HR/$\overline{W}$	C16	$\overline{HCS}$	C17	$\overline{TRST}$	D1	DV_{DD}
D2	D14	D3	D11	D4	D8	D5	D6
D6	D4	D7	D1	D8	A1	D9	HD15
D10	HD14	D11	HD13	D12	HD12	D13	HD11
D14	$\overline{HDS2}$	D15	HA11	D16	HA0	D17	DV_{DD}
E1	A11	E2	D15	E3	D12	E4	$\overline{CE3}$
E5	BOOTM3	E6	CV_{DD}	E7	CV_{DD}	E8	NC
E9	NC	E10	CV_{DD}	E11	NC	E12	NC
E13	RSVD9	E14	HA12	E15	HA10	E16	HA1/HCNTL1
E17	RST_MODE	F1	DV_{DD}	F2	A13	F3	A12
F4	A16	F5	CV_{DD}	F13	RSVD8	F14	HA9
F15	HA2/$\overline{HAS}$	F16	CLKIN	F17	CV_{DD}	G1	$\overline{CE2}$
G2	A17	G3	A15	G4	A14	G5	NC
G13	RSVD7	G14	HA8	G15	HA3	G16	$\overline{RESET}$
G17	HA13	H1	V_{SS}	H2	$\overline{CE1}$	H3	A19
H4	A18	H5	NC	H13	RSVD6	H14	HA4
H15	CLKOUT	H16	HA14	H17	V_{SS}	J1	V_{SS}
J2	$\overline{CE0}$	J3	A21	J4	A20	J5	NC
J13	RSVD5	J14	HA5	J15	HA15	J16	HA7
J17	V_{SS}	K1	IO7	K2	$\overline{BE0}$	K3	$\overline{BE1}$
K4	IO0	K5	CV_{DD}	K13	RSVD4	K14	TMS
K15	$\overline{HBE0}$	K16	HA16	K17	HA6	L1	CV_{DD}
L2	IO6	L3	$\overline{BE2}$	L4	$\overline{BE3}$	L5	NC
L13	RSVD3	L14	EMU1/$\overline{OFF}$	L15	TDO	L16	TDI
L17	TCK	M1	IO5	M2	$\overline{SSWE}$	M3	$\overline{SSOE}$
M4	IO1/BOOTM0	M5	NC	M13	RSVD2	M14	HA18
M15	HA17	M16	$\overline{HBE1}$	M17	DV_{DD}	N1	DV_{DD}
N2	IO4	N3	D16	N4	$\overline{SSADS}$	N5	NC
N6	CV_{DD}	N7	NC	N8	NC	N9	NC
N10	CV_{DD}	N11	NC	N12	NC	N13	RSVD1
N14	$\overline{HINT}$	N15	HCNTL0	N16	HMODE	N17	HA19
P1	IO3/BOOTM2	P2	CLKS1	P3	DR1	P4	D19
P5	D22	P6	D23	P7	D24	P8	CLKS2
P9	FSX0	P10	D31	P11	D28	P12	$\overline{INT4}$
P13	ARDY	P14	$\overline{HOLDA}$	P15	TIN/TOUT0	P16	CLKMD

Table 2−1. Pin Assignments (Continued)

BGA BALL #	SIGNAL	BGA BALL #	SIGNAL	BGA BALL #	SIGNAL	BGA BALL #	SIGNAL
P17	CV_{DD}	R1	CV_{DD}	R2	FSR1	R3	D18
R4	D20	R5	CLKR2	R6	FSR2	R7	DR2
R8	D26	R9	FSX2	R10	DX0	R11	$\overline{\text{INT5}}$
R12	$\overline{\text{INT0}}$	R13	$\overline{\text{INT2}}$	R14	$\overline{\text{ARE}}$	R15	CLKX1
R16	EMU0	R17	TIN/TOUT1	T1	D17	T2	IO2/BOOTM1
T3	CLKR1	T4	D21	T5	FSR0	T6	DR0
T7	D25	T8	D27	T9	D29	T10	D30
T11	NC	T12	$\overline{\text{NMI}}$	T13	$\overline{\text{AWE}}$	T14	$\overline{\text{INT3}}$
T15	FSX1	T16	DX1	T17	V_{SS}	U1	V_{SS}
U2	V_{SS}	U3	CLKR0	U4	CV_{DD}	U5	CLKS0
U6	DV_{DD}	U7	CLKX0	U8	CLKX2	U9	V_{SS}
U10	V_{SS}	U11	DX2	U12	CV_{DD}	U13	$\overline{\text{INT1}}$
U14	DV_{DD}	U15	$\overline{\text{AOE}}$	U16	$\overline{\text{HOLD}}$	U17	V_{SS}

2.3 Signal Descriptions

Table 2−2 lists each signal, function, and operating mode(s) grouped by function. See Section 2.2 for exact pin locations based on package type.

Table 2−2. Signal Descriptions

SIGNAL NAME	TYPE†	OTHER‡	DESCRIPTION
EMIF - ADDRESS BUS			
A[21:0]	O/Z	E,F	**External memory address bus (byte address).** Address all external memory (program and data). Since A[23:22] are redundant to the $\overline{CE}$[3:0] memory space selects in terms of memory addressing capability, A[23:22] are not externally provided.
EMIF - CONTROL SIGNALS COMMON TO ALL MEMORY TYPES			
$\overline{CE0}$ $\overline{CE1}$ $\overline{CE2}$ $\overline{CE3}$	O/Z	E,F	**External memory space enables.** Select one of four external memory ranges based on the address.
$\overline{BE0}$ $\overline{BE1}$ $\overline{BE2}$ $\overline{BE3}$	O/Z	E,F	**Byte-enable control.** Can be used as chip selects for external memory. These signals respond according to the data width of the memory access. 8-bit accesses cause a single byte enable to respond. 16-bit accesses cause two byte enables to respond. 32-bit accesses cause all four byte enables to respond.
CLKMEM	O/Z	E,F	**Memory interface clock (for SDRAM / SBSRAM).** Clock for synchronizing the external synchronous memories to the C55x external memory interface.
EMIF - DATA BUS			
D[31:0]	I/O/Z	D,E,F	**External data bus.** Provides data exchange between external memories and the C55x external memory interface. The bus holders on D[31:0] are controlled by the BH bit in the system register (SYSR).
EMIF - BUS ARBITRATION			
$\overline{HOLD}$	I	−	**Hold request.** $\overline{HOLD}$ is asserted by an external host to request control of the address, data and control signals.
$\overline{HOLDA}$	O/Z	F	**Hold acknowledge.** $\overline{HOLDA}$ is asserted by the DSP to indicate that the DSP is in the HOLD state and that the EMIF address, data and control signals are in a high-impedance state, allowing the external memory interface to be accessed by other devices.
EMIF - ASYNCHRONOUS MEMORY CONTROL SIGNALS			
$\overline{ARE}$	O/Z	E,F	**Asynchronous memory read enable.** $\overline{ARE}$ acts as a strobe during asynchronous memory reads only.
$\overline{AOE}$			**Asynchronous memory output enable.** $\overline{AOE}$ indicates whether a memory access is a read (low) or a write (high).
$\overline{AWE}$			**Asynchronous memory write enable.** $\overline{AWE}$ acts as a strobe during asynchronous memory writes only.
ARDY	I		**Asynchronous memory ready input.** ARDY indicates that an external device is ready for a bus transaction to be completed. If the device is not ready (ARDY is low), the processor extends the memory access by one cycle and checks ARDY again. The ARDY signal is sampled at the end of the STROBE period in the memory access.

† I = Input, O = Output, S = Supply, Z = High impedance

‡ Other Pin Characteristics:

A − Internal pullup (always enabled)
B − Internal pulldown (always enabled)
C − Hysteresis input
D − Pin has bus holder
E − Pin is high impedance in HOLD mode (due to $\overline{HOLD}$ pin).
F − Pin is high impedance in OFF mode (due to EMU1/$\overline{OFF}$ pin).
G − Pin can be configured as a general-purpose input.
H − PIn can be configured as a general-purpose output.
J − Internal pullup enabled by the HPE bit in the system register (SYSR)
K − Internal pulldown enabled by the HPE bit in the system register (SYSR)

Table 2−2. Signal Descriptions (Continued)

SIGNAL NAME	TYPE†	OTHER‡	DESCRIPTION
EMIF - SYNCHRONOUS BURST SRAM CONTROL SIGNALS			
$\overline{\text{SSADS}}$	O/Z	E,F	**SBSRAM address strobe.** $\overline{\text{SSADS}}$ is active (low) during the period of the SBSRAM access when the address is made available to the external memory by the DSP.
$\overline{\text{SSOE}}$			**SBSRAM output enable.** $\overline{\text{SSOE}}$ is active (low) during read accesses to SBSRAM.
$\overline{\text{SSWE}}$			**SBSRAM write enable.** $\overline{\text{SSWE}}$ is active (low) during write accesses to SBSRAM.
EMIF - SYNCHRONOUS DRAM CONTROL SIGNALS			
$\overline{\text{SDRAS}}$	O/Z	E,F	**SDRAM row address strobe.** $\overline{\text{SDRAS}}$ is active (low) during the ACTV, DCAB, REFR, and MRS commands.
$\overline{\text{SDCAS}}$			**SDRAM address column strobe.** $\overline{\text{SDCAS}}$ is active (low) during reads, writes, and the REFR and MRS commands.
$\overline{\text{SDWE}}$			**SDRAM write enable.** $\overline{\text{SDWE}}$ is active (low) during writes, and the DCAB and MRS commands.
SDA10			**SDRAM A10 address (address/autoprecharge disable).** SDA10 is used during reads, writes, and all commands.
MULTICHANNEL BUFFERED SERIAL PORT SIGNALS			
CLKR0 CLKR1 CLKR2	I/O/Z	C,F,G,H	**Serial shift clock reference for the receiver**
DR0 DR1 DR2	I	G	**Serial receive data input**
FSR0 FSR1 FSR2	I/O/Z	F,G,H	**Frame synchronization signal for the receiver**
CLKX0 CLKX1 CLKX2	I/O/Z	C,F,G,H	**Serial shift clock reference for the transmitter**
DX0 DX1 DX2	O/Z	F,H	**Serial transmit data output**
FSX0 FSX1 FSX2	I/O/Z	F,G,H	**Frame synchronization signal for the transmitter**
CLKS0 CLKS1 CLKS2	I	G	**External clock source to the sample rate generator**

† I = Input, O = Output, S = Supply, Z = High impedance

‡ Other Pin Characteristics:

A − Internal pullup (always enabled)
B − Internal pulldown (always enabled)
C − Hysteresis input
D − Pin has bus holder
E − Pin is high impedance in HOLD mode (due to $\overline{\text{HOLD}}$ pin).
F − Pin is high impedance in OFF mode (due to EMU1/$\overline{\text{OFF}}$ pin).
G − Pin can be configured as a general-purpose input.
H − PIn can be configured as a general-purpose output.
J − Internal pullup enabled by the HPE bit in the system register (SYSR)
K − Internal pulldown enabled by the HPE bit in the system register (SYSR)

Table 2−2. Signal Descriptions (Continued)

SIGNAL NAME	TYPE†	OTHER‡	DESCRIPTION
ENHANCED HOST-PORT INTERFACE (EHPI)			
HA[19:3] HA2/HAS HA1/HCNTL1 HA0	I	J	**Host address bus:** In ***non-multiplexed mode*** (HMODE pin high): HA[19:0] functions as the host address bus only In ***multiplexed mode*** (HMODE pin low): HA[19:3] are disabled HA2/HAS functions as HAS (Host Address Strobe). Hosts with multiplexed address and data pins may require HAS to latch the address in the HPIA register. HA1/HCNTL1 functions as HCNTL1 (Host Control Input) and with HCNTL0 determines the type of transaction being performed.
HD[15:0]	I/O/Z	D,F	**Host data bus.** Provides data exchange between the host and C55x EHPI. The bus holders on HD[15:0] are controlled by the HBH bit in the system register (SYSR).
HCS	I	J	**Host chip select.** HCS is the select input for the EHPI and must be driven low during accesses. If the EHPI is not used, HCS must be driven high.
HA2/HAS	I	J	**Host address strobe.** Operates as HAS when HMODE is low (multiplexed mode). Hosts with multiplexed address and data pins may require HAS to latch the address in the HPIA register.
HR/W	I	J	**Host read or write select.** Controls the direction of the EHPI transfer.
HDS1 HDS2	I	J	**Host data strobes.** HDS1 and HDS2 are driven by the host read and write strobes to control data transfers.
HRDY	O/Z	F,J	**Host ready (from DSP to host).** HRDY informs the host when the EHPI is ready for the next transfer.
HBE0 HBE1	I	K	**EHPI byte enables.** HBE0 and HBE1 are driven low selectively by the host to indicate whether the transaction involves the lower byte only, the upper byte only, or both. As of revision 2.1, the byte-enable function on the EHPI will no longer be supported. These pins must be driven low by an external device, by external pulldown resistors or by the internal pulldown circuit controlled by the HPE bit in the SYSR register.
HMODE	I	J	**Host multiplexed/non-multiplexed mode select.** When HMODE is high, the EHPI operates in nonmultiplexed mode. When HMODE is low, the EHPI operates in multiplexed mode.
HCNTL0 HA1/HCNTL1	I	J	**Host control selects.** HCNTL0 and HCNTL1 select host accesses to EHPI address, data or control registers. HA1/HCNTL operates as HCNTL when HMODE is low (multiplexed mode).
HINT	O/Z	F	**Host interrupt (from DSP to host).** This output is used to interrupt the host. HINT is high following reset.

† I = Input, O = Output, S = Supply, Z = High impedance

‡ Other Pin Characteristics:

A − Internal pullup (always enabled)
B − Internal pulldown (always enabled)
C − Hysteresis input
D − Pin has bus holder
E − Pin is high impedance in HOLD mode (due to HOLD pin).
F − Pin is high impedance in OFF mode (due to EMU1/OFF pin).
G − Pin can be configured as a general-purpose input.
H − PIn can be configured as a general-purpose output.
J − Internal pullup enabled by the HPE bit in the system register (SYSR)
K − Internal pulldown enabled by the HPE bit in the system register (SYSR)

Table 2−2. Signal Descriptions (Continued)

SIGNAL NAME	TYPE†	OTHER‡	DESCRIPTION
INTERRUPT AND RESET SIGNALS			
$\overline{\text{RESET}}$	I	C	**Device reset.** $\overline{\text{RESET}}$ causes the DSP to terminate execution and causes reinitialization of the CPU and peripherals. The response of the DSP after reset is determined by the RST_MODE pin.
RST_MODE	I		**Device reset mode control.** RST_MODE controls how a device reset is handled. As of revision 2.1, the RST_MODE function will no longer be supported. RST_MODE will be driven low internally. After reset, the CPU will branch to the reset vector and begin execution. The external state of the RST_MODE pin will have no effect on device operation.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$ $\overline{\text{INT4}}$ $\overline{\text{INT5}}$	I	C	**Maskable external interrupts.** $\overline{\text{INT0}}$−$\overline{\text{INT5}}$ are prioritized and are maskable via the interrupt enable registers (IER0 and IER1) and the Interrupt Mode bit (INTM in ST1_55). $\overline{\text{INT0}}$−$\overline{\text{INT5}}$ can be polled and reset via the Interrupt Flag Registers (IFR0 and IFR1).
$\overline{\text{NMI}}$	I	C	**Nonmaskable external interrupt.** $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by the interrupt enable registers (IER0 and IER1). When $\overline{\text{NMI}}$ is activated, the interrupt is always performed.
JTAG EMULATION			
TCK	I	A,C	**IEEE Standard 1149.1 test clock.** TCK is normally a free-running clock signal with a 50% duty cycle. The changes on the test access port (TAP) of input signals TDI and TMS are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal TDO occur on the falling edge of TCK.
TDI	I	A	**IEEE Standard 1149.1 test data input.** TDI is clocked into the selected register (instruction or data) on the rising edge of TCK.
TDO	O	−	**IEEE Standard 1149.1 test data output.** The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress.
TMS	I	A	**IEEE Standard 1149.1 test mode select.** This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	B	**IEEE Standard 1149.1 test reset.** $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected, or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. This pin has an on-chip pulldown circuit to provide control of the pin when it is not externally connected. An external pullup resistor should not be connected to this pin.

† I = Input, O = Output, S = Supply, Z = High impedance

‡ Other Pin Characteristics:

A − Internal pullup (always enabled)
B − Internal pulldown (always enabled)
C − Hysteresis input
D − Pin has bus holder
E − Pin is high impedance in HOLD mode (due to $\overline{\text{HOLD}}$ pin).
F − Pin is high impedance in OFF mode (due to EMU1/$\overline{\text{OFF}}$ pin).
G − Pin can be configured as a general-purpose input.
H − PIn can be configured as a general-purpose output.
J − Internal pullup enabled by the HPE bit in the system register (SYSR)
K − Internal pulldown enabled by the HPE bit in the system register (SYSR)

Table 2−2. Signal Descriptions (Continued)

SIGNAL NAME	TYPE†	OTHER‡	DESCRIPTION
JTAG EMULATION (CONTINUED)			
EMU0	I/O/Z	A	**Emulation pin 0.** When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1449.1 scan system.
EMU1/$\overline{\text{OFF}}$	I/O/Z	A	**Emulation pin 1 / disable all outputs.** When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system. When $\overline{\text{TRST}}$ is driven low, EMU1/$\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. The EMU1/$\overline{\text{OFF}}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the $\overline{\text{OFF}}$ feature, the following apply: $\overline{\text{TRST}}$ = low EMU0 = high EMU1/$\overline{\text{OFF}}$ = low
RSVD[1:9]	I/O		**Reserved.** Reserved for future emulation purposes. These pins should be left unconnected.
CLOCK SIGNALS			
CLKIN	I	C	**Clock input**
CLKOUT	O/Z	F	**Clock output.** CLKOUT can represent the internal CPU clock or can be divided down to generate a slower clock by programming the CLKDIV field in the system register (SYSR).
CLKMD	I	C	**Clock mode select.** CLKMD selects the mode of the clock generator after reset. When CLKMD is low after reset, the clock generator will run at the same frequency as CLKIN. If CLKMD is high after reset, the clock generator will run at one-half of the frequency of CLKIN. The clock generator can later be reprogrammed in software.
TIMERS			
TIN/TOUT0	I/O/Z	F,H	**Timer 0 input/output.** When configured as an output, TIN/TOUT0 generates a pulse or toggles when on-chip Timer 0 counts down to zero. When configured as an input, TIN/TOUT0 is used as a clock reference for Timer 0. The operation of this pin is configured in the timer control register (TCR0).
TIN/TOUT1		F,H	**Timer 1 input/output.** When configured as an output, TIN/TOUT1 generates a pulse or toggles when on-chip Timer 1 counts down to zero. When configured as an input, TIN/TOUT1 is used as a clock reference for Timer 1. The operation of this pin is configured in the timer control register (TCR1).
GENERAL-PURPOSE I/O SIGNALS			
IO7 IO6 IO5 IO4 IO3/BOOTM2 IO2/BOOTM1 IO1/BOOTM0 IO0	I/O/Z	F,G,H	**General-purpose configurable inputs/outputs.** IO[7:0] can be individually configured as inputs or outputs via the GPIO direction register (IODIR). Data can be read from inputs or data written to outputs via the GPIO Data Register (IODATA). In addition, the bootloader uses IO4 as an output during the boot process. For detailed information on the operation of the bootloader, see the *Using the TMS320VC5510 Bootloader* application report (literature number SPRA763). **Boot Mode Selection signals.** BOOTM[2:0] are sampled following reset to configure the boot mode for the DSP. These signals are shared with IO[3:1]. After boot is complete, these signals can be used as general-purpose inputs/outputs.
BOOTM3	I	A	**Boot Mode Selection signal.** BOOTM3 is sampled during the operation of the on-chip bootloader in conjunction with BOOTM[2:0] to configure the boot mode.
XF	O/Z	F,H	**External flag output**

† I = Input, O = Output, S = Supply, Z = High impedance

‡ Other Pin Characteristics:

A − Internal pullup (always enabled)
B − Internal pulldown (always enabled)
C − Hysteresis input
D − Pin has bus holder
E − Pin is high impedance in HOLD mode (due to $\overline{\text{HOLD}}$ pin).
F − Pin is high impedance in OFF mode (due to EMU1/$\overline{\text{OFF}}$ pin).
G − Pin can be configured as a general-purpose input.
H − PIn can be configured as a general-purpose output.
J − Internal pullup enabled by the HPE bit in the system register (SYSR)
K − Internal pulldown enabled by the HPE bit in the system register (SYSR)

Table 2−2. Signal Descriptions (Continued)

SIGNAL NAME	TYPE†	OTHER‡	DESCRIPTION
SUPPLY VOLTAGE PINS			
CV_{DD}	S		**Dedicated power supply for the internal logic (CPU and peripherals)**
DV_{DD}	S		**Dedicated power supply for the I/O pins**
V_{SS}	S		**Ground**
MISCELLANEOUS PINS			
NC			**No connection − do not connect**

† I = Input, O = Output, S = Supply, Z = High impedance

‡ Other Pin Characteristics:

A − Internal pullup (always enabled)
B − Internal pulldown (always enabled)
C − Hysteresis input
D − Pin has bus holder
E − Pin is high impedance in HOLD mode (due to $\overline{\text{HOLD}}$ pin).
F − Pin is high impedance in OFF mode (due to EMU1/$\overline{\text{OFF}}$ pin).
G − Pin can be configured as a general-purpose input.
H − PIn can be configured as a general-purpose output.
J − Internal pullup enabled by the HPE bit in the system register (SYSR)
K − Internal pulldown enabled by the HPE bit in the system register (SYSR)

3 Functional Overview

The following functional overview is based on the block diagram in Figure 3−1.

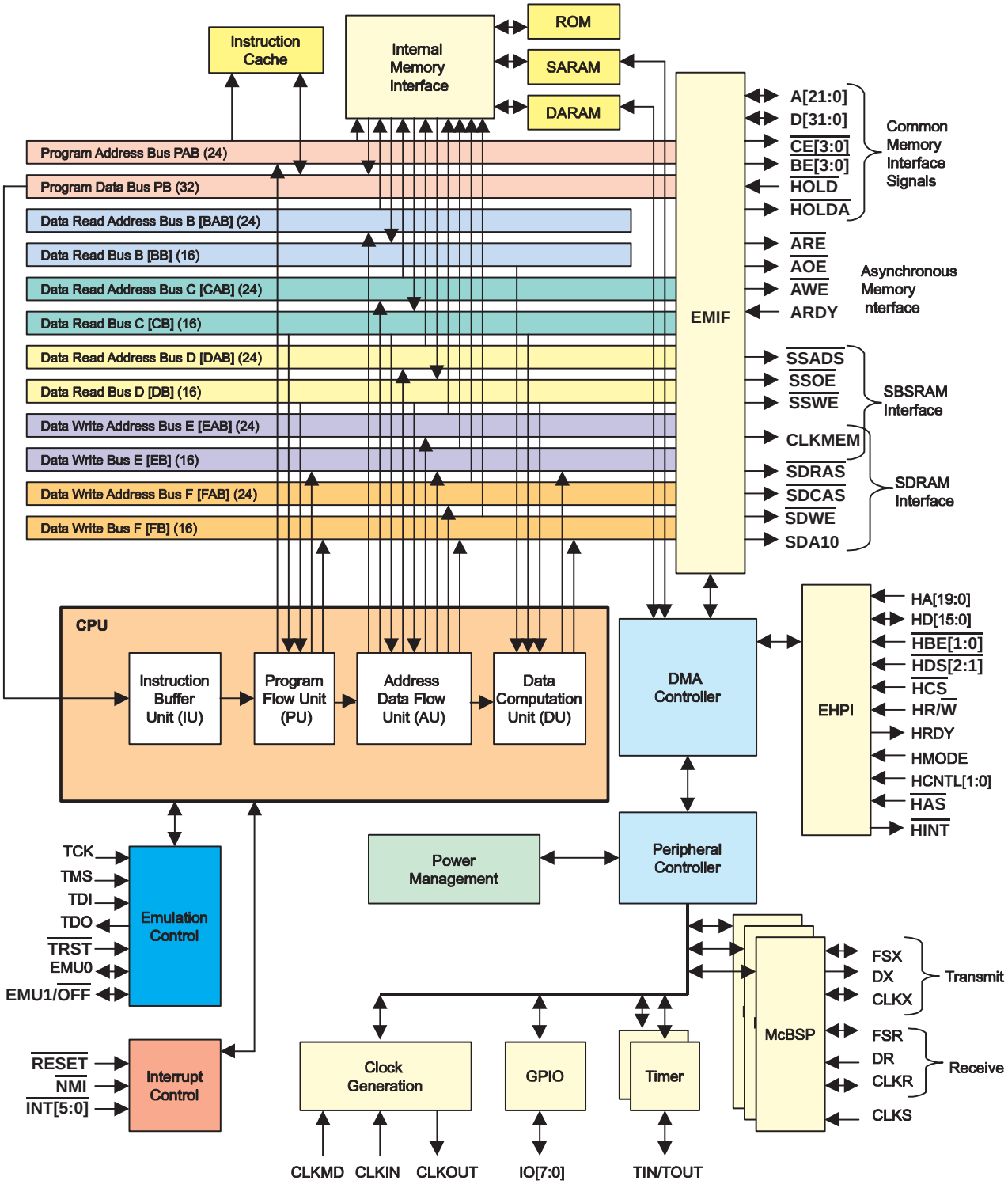


Figure 3−1. TMS320VC5510/5510A Functional Block Diagram

3.1 Memory

The 5510/5510A supports a unified memory map (program and data accesses are made to the same physical space). The total on-chip memory is 352K bytes (176K 16-bit words).

3.1.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 000000h−00FFFFh and is composed of eight blocks of 8K-bytes each (see Table 3−1). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). DARAM can be accessed by the internal program, data, or DMA buses.

Table 3−1. DARAM Blocks

BYTE ADDRESS RANGE	MEMORY BLOCK
000000h − 001FFFh	DARAM 0†
002000h − 003FFFh	DARAM 1
004000h − 005FFFh	DARAM 2
006000h − 007FFFh	DARAM 3
008000h − 009FFFh	DARAM 4
00A000h − 00BFFFh	DARAM 5
00C000h − 00DFFFh	DARAM 6
00E000h − 00FFFFh	DARAM 7

† First 192 bytes are reserved for Memory-Mapped Registers (MMRs).

3.1.2 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 010000h−04FFFFh and is composed of 32 blocks of 8K-bytes each (see Table 3−2). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses.

Table 3−2. SARAM Blocks

BYTE ADDRESS RANGE	MEMORY BLOCK	BYTE ADDRESS RANGE	MEMORY BLOCK
010000h − 011FFFh	SARAM 0	030000h − 031FFFh	SARAM 16
012000h − 013FFFh	SARAM 1	032000h − 033FFFh	SARAM 17
014000h − 015FFFh	SARAM 2	034000h − 035FFFh	SARAM 18
016000h − 017FFFh	SARAM 3	036000h − 037FFFh	SARAM 19
018000h − 019FFFh	SARAM 4	038000h − 039FFFh	SARAM 20
01A000h − 01BFFFh	SARAM 5	03A000h − 03BFFFh	SARAM 21
01C000h − 01DFFFh	SARAM 6	03C000h − 03DFFFh	SARAM 22
01E000h − 01FFFFh	SARAM 7	03E000h − 03FFFFh	SARAM 23
020000h − 021FFFh	SARAM 8	040000h − 041FFFh	SARAM 24
022000h − 023FFFh	SARAM 9	042000h − 043FFFh	SARAM 25
024000h − 025FFFh	SARAM 10	044000h − 045FFFh	SARAM 26
026000h − 027FFFh	SARAM 11	046000h − 047FFFh	SARAM 27
028000h − 029FFFh	SARAM 12	048000h − 049FFFh	SARAM 28
02A000h − 02BFFFh	SARAM 13	04A000h − 04BFFFh	SARAM 29
02C000h − 02DFFFh	SARAM 14	04C000h − 04DFFFh	SARAM 30
02E000h − 02FFFFh	SARAM 15	04E000h − 04FFFFh	SARAM 31

3.1.3 On-Chip ROM

The ROM is located at the byte address range FF8000h−FFFFFFh when MPNMC = 0 at reset. The ROM is composed of a single block of 32K bytes. When MPNMC = 1 at reset, the on-chip ROM is disabled and not present in the memory map, and byte address range FF8000h−FFFFFFh is directed to external memory space. MPNMC is a bit located in the ST3 status register, and its status is determined by the logic level on the BOOTM[2:0] pins when sampled at reset. If BOOTM[2:0] are all logic 0 at reset, the MPNMC bit is set to 1 and the on-chip ROM is disabled; otherwise, the MPNMC bit is cleared to 0 and the on-chip ROM is enabled. These pins are not sampled again until the next hardware reset. The software reset instruction does not affect the MPNMC bit. Software can also be used to set or clear the MPNMC bit. ROM can be accessed by the program, data, or DMA buses. The first 16-bit word access to ROM requires three cycles. Subsequent accesses require two cycles per 16-bit word.

The standard on-chip ROM contains a bootloader which provides a variety of methods to load application code automatically after power up or a hardware reset. For more information, see Section 3.1.5 of this document. The vector table associated with the bootloader is also contained in the ROM.

A sine look-up table is provided containing 256 values (crossing 360 degrees) expressed in Q15 format.

The remaining components are used during factory testing purposes.

Table 3−3. Standard On-Chip ROM Contents

BYTE ADDRESS RANGE	DESCRIPTION
FF8000h − FF8FFFh	Bootloader
FF9000h − FFF9FFh	Reserved
FFFA00h − FFFBFFh	Sine look-up table
FFFC00h − FFFEFFh	Factory Test Code
FFFF00h − FFFFFBh	Vector Table
FFFFFCh − FFFFFFh	ID Code

3.1.4 Instruction Cache

The 24K-byte instruction cache provides three configurations:

- One 2-way cache block only
- One 2-way cache block plus one RAMSET block
- One 2-way cache block plus two RAMSET blocks

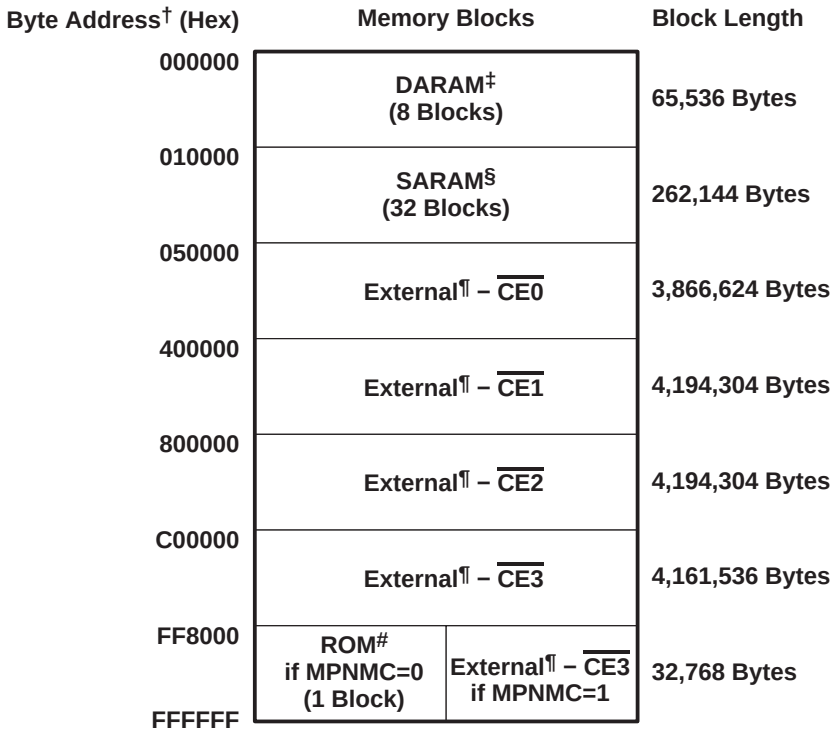
The 2-way cache uses 2-way set associative mapping and holds up to 16K bytes. It is organized as 512 sets of two cache lines per set. Each cache line contains 16 bytes. Each tag has two corresponding cache lines, providing two opportunities for a hit on a given tag. The 2-way cache is updated based on a least-recently-used algorithm.

Each RAMSET block provides a 4K-byte bank of memory to hold a continuous image of code. Each RAMSET is composed of 256 lines with 16 bytes per line. Each RAMSET uses a single tag to define a continuous memory image in the RAMSET. The tag defines the start address of the RAMSET. Once the TAG is loaded, the RAMSET is filled. The RAMSET contents remain constant until the tag is changed. The RAMSETs provide an efficient method to cache frequently used functions.

Control bits in CPU status register ST3_55 provide the ability to enable, freeze, and flush the cache.

For more information on the instruction cache, see the *TMS320VC5510 DSP Instruction Cache Reference Guide* (literature number SPRU576).

3.1.5 Memory Map



† Address shown represents the first byte address in each block.
‡ Dual-access RAM (DARAM): two accesses per cycle per block, 8 blocks of 8K bytes.
§ Single-access RAM (SARAM): one access per cycle per block, 32 blocks of 8K bytes.
¶ External memory spaces are selected by the chip-enable signal shown ($\overline{CE}$[0:3]). Supported memory types include: asynchronous, synchronous DRAM (SDRAM), and synchronous burst SRAM (SBSRAM).
# Read-only memory (ROM): one access every two cycles, one block of 32K bytes.

Figure 3−2. TMS320VC5510/5510A Memory Map

3.1.6 Bootloader

The on-chip bootloader provides a method to transfer application code and tables from an external source to the on-chip RAM at power up. The 5510/5510A provides several options to download the code to accommodate varying system requirements. These options include:

- Enhanced Host-Port Interface (EHPI) boot
- External memory boot from 8-/16-/32-bit-wide asynchronous memory
- Serial slave boot from McBSP0 with 8- or 16-bit element length
- Serial EEPROM boot from McBSP0 in 8-bit SPI format

External pins BOOTM3, BOOTM2, BOOTM1, and BOOTM0 select the boot configuration. The values of BOOTM[2:0] are latched with the rising edge of the $\overline{RESET}$ input. BOOTM[0] is shared with general-purpose IO1. BOOTM[1] is shared with general-purpose IO2. BOOTM[2] is shared with general-purpose IO3.

The boot configurations available are summarized in Table 3−4. For detailed information on the bootloader functions, refer to the *Using the TMS320VC5510 Bootloader* Application Report (literature number SPRA763).

Table 3−4. TMS320VC5510/5510A Boot Configurations

BOOTM[3:0]	BOOT PROCESS	EXECUTION START BYTE ADDRESS AFTER BOOT IS COMPLETE
0000	No boot	FFFF00h (reset vector)
0001	Serial SPI EEPROM boot from McBSP0 supporting 24-bit address	Destination specified in the boot table
0010	Reserved	−
0011	Reserved	−
0100	Reserved	−
0101	Reserved	−
0110	Reserved	−
0111	Reserved	−
1000	No boot	FFFF00h (reset vector)
1001	Serial SPI EEPROM boot from McBSP0 supporting 16-bit address	Destination specified in the boot table
1010	Parallel EMIF boot from 8-bit asynchronous memory	Destination specified in the boot table
1011	Parallel EMIF boot from 16-bit asynchronous memory	Destination specified in the boot table
1100	Parallel EMIF boot from 32-bit asynchronous memory	Destination specified in the boot table
1101	EHPI boot	010000h (on-chip SARAM)
1110	Standard serial boot from McBSP0, 16-bit element length	Destination specified in the boot table
1111	Standard serial boot from McBSP0, 8-bit element length	Destination specified in the boot table

3.2 Peripherals

The 5510/5510A supports the following peripherals:

- An external memory interface (EMIF)
- A six-channel direct memory access (DMA) controller
- 16-bit parallel Enhanced Host-Port Interface (EHPI)
- A digital phase-locked loop (DPLL) clock generator
- Two timers
- Three multichannel buffered serial ports (McBSPs)
- Eight configurable general-purpose I/O pins

Peripheral information specific to the 5510/5510A peripherals is included in the following sections. For detailed information on the C55x™ DSP peripherals, see the following documents:

- *TMS320C55x™ DSP Functional Overview* (literature number SPRU312)
- *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317)
- *TMS320VC5510 DSP Instruction Cache Reference Guide* (literature number SPRU576)
- *TMS320VC5501/5502/5503/5507/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide* (literature number SPRU592)
- *TMS320VC5503/5507/5509/5510 DSP Direct Memory Access (DMA) Controller Reference Guide* (literature number SPRU587)
- *TMS320VC5510 DSP Host Port Interface (HPI) Reference Guide* (literature number SPRU588)
- *TMS320VC5503/5507/5509/5510 DSP Timers Reference Guide* (literature number SPRU595)

3.2.1 System Register (SYSR)

The 5510/5510A system register (SYSR) provides control over certain device-specific functions. SYSR is located at port address 07FDh.

15 10	9	8	7	6	5	4	3	2 0
Reserved	HPE	BH	HBH	BOOTM3	Reserved	Reserved	Reserved	CLKDIV
R−000000	R/W−1	R/W−0	R/W−0	R−0	R−0	R/W−0	R/W−0	R/W−000

LEGEND: R = Read, W = Write, *n* = value after reset

Figure 3−3. System Register (SYSR) Bit Layout

Table 3−5. System Register (SYSR) Bit Functions

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15−10	Reserved	000000	These bits are reserved and are unaffected by writes.
9	HPE	1	**EHPI pullup/pulldown enable.** Enables the internal pullups on the EHPI control pins $\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, $\overline{\text{HCS}}$, $\overline{\text{HAS}}$, HR/$\overline{\text{W}}$, HMODE, HCNTL0, and HA1/HCNTL1. Enables the internal pulldowns on EHPI control pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$. HPE = 0 Pullups and pulldowns disabled HPE = 1 Pullups and pulldowns enabled.
8	BH	0	**EMIF data bus holder enable.** Enables internal bus holders on D[31:0]. BH = 0 EMIF data bus holders disabled. BH = 1 EMIF data bus holders enabled.
7	HBH	0	**EHPI data bus holder enable.** Enables internal bus holders on HD[15:0]. HBH = 0 EHPI data bus holders disabled. HBH = 1 EHPI data bus holders enabled.
6	BOOTM3	0	**BOOTM3 status.** This read-only bit represents the state of the BOOTM3 pin.
5	Reserved	0	This bit is reserved and is unaffected by writes.
4	Reserved	0	This bit is reserved and must be written as 0.
3	Reserved	0	This bit is reserved and is unaffected by writes.
2−0	CLKDIV	000	**CLKOUT divide factor.** Allows the clock present on the CLKOUT pin to be a divided-down version of the internal CPU clock. This field does not affect the programming of the PLL CLKDIV = 000 CLKOUT represents the CPU clock divided by 1 CLKDIV = 001 CLKOUT represents the CPU clock divided by 2 CLKDIV = 010 CLKOUT represents the CPU clock divided by 4 CLKDIV = 011 CLKOUT represents the CPU clock divided by 6 CLKDIV = 100 CLKOUT represents the CPU clock divided by 8 CLKDIV = 101 CLKOUT represents the CPU clock divided by 10 CLKDIV = 110 CLKOUT represents the CPU clock divided by 12 CLKDIV = 111 CLKOUT represents the CPU clock divided by 14

3.2.2 Direct Memory Access (DMA)

The 5510/5510A DMA provides the following features:

- Four standard ports, one for each of the following data resources: DARAM, SARAM, Peripherals, and External Memory
- Six channels, which allow the DMA controller to track the context of six independent DMA channels
- Programmable low/high priority for each DMA channel
- One interrupt for each DMA channel
- Event synchronization. DMA transfers in each channel can be dependent on the occurrence of selected events.
- Programmable address modification for source and destination addresses
- Dedicated Idle Domain allows the DMA controller to be placed in a low-power (idle) state under software control.
- DMA controller supports EHPI accesses to internal/external memory

The 5510/5510A DMA controller allows transfers to be synchronized to selected events. The 5510/5510A supports 14 separate sync events and each channel can be tied to separate sync events independent of the other channels. Sync events are selected by programming the SYNC field in the channel-specific DMA Channel Control Register (DMA_CCR). The sync events available on the 5510/5510A are shown in Table 3−6.

For more information on the 5510/5510A DMA, see the *TMS320VC5503/5507/5509/5510 DSP Direct Memory Access (DMA) Controller Reference Guide* (literature number SPRU587).

Table 3−6. DMA Sync Events

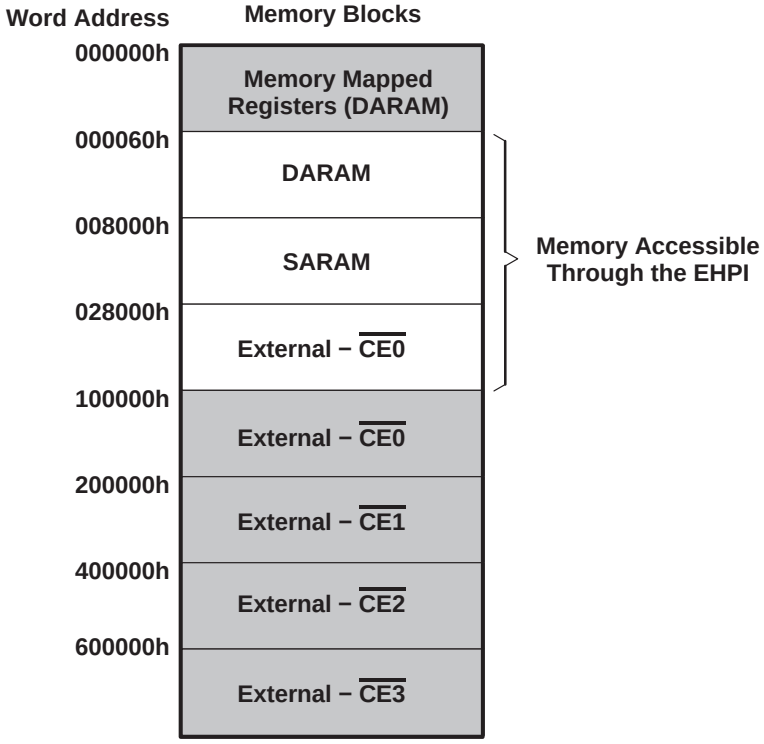
SYNC FIELD IN DMA_CCR	SYNC EVENT
00000b	No sync event
00001b	McBSP0 receive event (REVT0)
00010b	McBSP0 transmit event (XEVT0)
00101b	McBSP1 receive event (REVT1)
00110b	McBSP1 transmit event (XEVT1)
01001b	McBSP2 receive event (REVT2)
01010b	McBSP2 transmit event (XEVT2)
01101b	Timer 0 event
01110b	Timer 1 event
01111b	External Interrupt 0
10000b	External Interrupt 1
10001b	External Interrupt 2
10010b	External Interrupt 3
10011b	External Interrupt 4
10100b	External Interrupt 5
Other values	Reserved (do not use these values)

3.2.3 Enhanced Host Port Interface (EHPI)

The 5510/5510A EHPI provides a 16-bit parallel interface to a host with the following features:

- 20-bit host address bus
- 16-bit host data bus
- Multiplexed and non-multiplexed bus modes
- Host access to on-chip SARAM, on-chip DARAM, and external memory
- 20-bit address register (in multiplexed mode) with autoincrement capability for faster transfers
- Multiple address/data strobes provide a glueless interface to a variety of hosts
- HRDY signal for handshaking with host

The 5510/5510A EHPI can access internal DARAM, internal SARAM and a portion of the external memory space. The EHPI cannot directly access the on-chip peripherals and cannot access the memory-mapped registers below word address 000060h in DARAM. Note that all memory accesses made though the EHPI are word-addressed. A map of the memory space accessible by the EHPI is shown in Figure 3−4. The EHPI can access from word address 000060h to 0FFFFFh. The shaded areas of the memory map are not accessible by the EHPI.



NOTE A: The shaded areas of the memory map are not accessible by the EHPI.

Figure 3−4. EHPI Memory Map

When the EHPI inputs are uncontrolled, noise on the inputs can cause spurious accesses that may corrupt internal memory. If the EHPI is not driven by a host, the $\overline{\text{HCS}}$ pin should be driven high by one of the following methods:

- An external device
- External pullup resistor, or
- The on-chip pullup circuit controlled by the HPE bit in the System Register (SYSR). See Section 3.2.1 for more information on how to configure this control.

As of revision 2.1, the byte-enable function of the EHPI is no longer supported. Pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$ must be driven low at all times.

For more information on the 5510/5510A EHPI, see the *TMS320VC5510 DSP Host Port Interface (HPI) Reference Guide* (literature number SPRU588).

3.2.4 General-Purpose Input/Output Port (GPIO)

The 5510/5510A provides eight dedicated general-purpose input/output pins, IO0−IO7. Each pin can be independently configured as an input or an output using the I/O Direction Register (IODIR). The I/O Data Register (IODATA) is used to monitor the logic state of pins configured as inputs and control the logic state of pins configured as outputs. IODIR and IODATA are accessible to the CPU and to the DMA controller at addresses in I/O space. See Table 3−19 for address information. The description of the IODIR is shown in Figure 3−5 and Table 3−7. The description of IODATA is shown in Figure 3−6 and Table 3−8.

To configure a GPIO pin as an input, clear the direction bit that corresponds to the pin in IODIR to 0. To read the logic state of the input pin, read the corresponding bit in IODATA.

To configure a GPIO pin as an output, set the direction bit that corresponds to the pin in IODIR to 1. To control the logic state of the output pin, write to the corresponding bit in IODATA.

15	8	7	6	5	4	3	2	1	0
Reserved		IO7DIR	IO6DIR	IO5DIR	IO4DIR	IO3DIR	IO2DIR	IO1DIR	IO0DIR
R−00000000		R/W−0	R/W−0	R/W−0	R/W−0	R/W−0	R/W−0	R/W−0	R/W−0

LEGEND: R = Read, W = Write, *n* = value after reset

Figure 3−5. I/O Direction Register (IODIR) Bit Layout

Table 3−7. I/O Direction Register (IODIR) Bit Functions

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15−8	Reserved	0	These bits are reserved and are unaffected by writes.
7−0	IOxDIR	0	**IOx Direction Control Bit.** Controls whether IOx operates as an input or an output. IOxDIR = 0 IOx is configured as an input. IOxDIR = 1 IOx is configured as an output.

15	8	7	6	5	4	3	2	1	0
Reserved		IO7D	IO6D	IO5D	IO4D	IO3D	IO2D	IO1D	IO0D
R−00000000		R/W−pin	R/W−pin	R/W−pin	R/W−pin	R/W−pin	R/W−pin	R/W−pin	R/W−pin

LEGEND: R = Read, W = Write, *pin* = value present on the pin (IO7−IO0 default to inputs after reset)

Figure 3−6. I/O Data Register (IODATA) Bit Layout

Table 3−8. I/O Data Register (IODATA) Bit Functions

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15−8	Reserved	0	These bits are reserved and are unaffected by writes.
7−0	IOxD	pin†	**IOx Data Bit.** If IOx is configured as an input (IOxDIR = 0 in IODIR): IOxD = 0 The signal on the IOx pin is low. IOxD = 1 The signal on the IOx pin is high. If IOx is configured as an output (IOxDIR = 1 in IODIR): IOxD = 0 Drive the signal on the IOx pin low. IOxD = 1 Drive the signal on the IOx pin high.

† *pin* = value present on the pin (IO7−IO0 default to inputs after reset)

3.3 CPU Register Description

The 5510/5510A CPU registers are shown in Table 3−9. For code compatibility, many TMS320C55x (C55x) CPU registers map to comparable TMS320C54x™ (C54x™) CPU register addresses. The corresponding TMS320C54x (C54x) CPU registers are indicated in these instances.

Table 3−9. CPU Registers

C54x REGISTER	VC5510/5510A REGISTER	WORD ADDRESS (HEX)	DESCRIPTION
IMR	IER0	00	Interrupt Mask Register 0
IFR	IFR0	01	Interrupt Flag Register 0
−	ST0_55	02	Status Register 0 for C55x
−	ST1_55	03	Status Register 1 for C55x
−	ST3_55	04	Status Register 3 for C55x
−	−	05	Reserved
ST0	ST0	06	Status Register ST0 (for 54x compatibility)
ST1	ST1	07	Status Register ST1 (for 54x compatibility)
AL	AC0L	08	Accumulator 0 (equivalent to Accumulator A on C54x)
AH	AC0H	09	
AG	AC0G	0A	
BL	AC1L	0B	Accumulator 1 (equivalent to Accumulator A on C54x)
BH	AC1H	0C	
BG	AC1G	0D	
TREG	T3	0E	Temporary Register
TRN	TRN0	0F	Transition Register
AR0	AR0	10	Auxiliary Register 0
AR1	AR1	11	Auxiliary Register 1
AR2	AR2	12	Auxiliary Register 2
AR3	AR3	13	Auxiliary Register 3
AR4	AR4	14	Auxiliary Register 4
AR5	AR5	15	Auxiliary Register 5
AR6	AR6	16	Auxiliary Register 6
AR7	AR7	17	Auxiliary Register 7
SP	SP	18	Stack Pointer Register
BK	BK03	19	Circular Buffer Size Register
BRC	BRC0	1A	Block Repeat Counter
RSA	RSA0L	1B	Block Repeat Start Address
REA	REA0L	1C	Block Repeat End Address
PMST	PMST	1D	Processor Mode Status Register
XPC	XPC	1E	Program Counter Extension Register
−	−	1F	Reserved
−	T0	20	Temporary Data Register 0
−	T1	21	Temporary Data Register 1
−	T2	22	Temporary Data Register 2
−	T3	23	Temporary Data Register 3

TMS320C54x and C54x are trademarks of Texas Instruments.

Table 3−9. CPU Registers (Continued)

C54x REGISTER	VC5510/5510A REGISTER	WORD ADDRESS (HEX)	DESCRIPTION
−	AC2L	24	Accumulator 2
−	AC2H	25	
−	AC2G	26	
−	CDP	27	Coefficient Data Pointer
−	AC3L	28	Accumulator 3
−	AC3H	29	
−	AC3G	2A	
−	DPH	2B	Extended Data Page Pointer
−	MDP05	2C	Reserved
−	MDP67	2D	Reserved
−	DP	2E	Memory Data Page Start Address
−	PDP	2F	Peripheral Data Page Start Address
−	BK47	30	Circular Buffer Size Register for AR[4−7]
−	BKC	31	Circular Buffer Size Register for CDP
−	BSA01	32	Circular Buffer Start Address Register for AR[0−1]
−	BSA23	33	Circular Buffer Start Address Register for AR[2−3]
−	BSA45	34	Circular Buffer Start Address Register for AR[4−5]
−	BSA67	35	Circular Buffer Start Address Register for AR[6−7]
−	BSAC	36	Circular Buffer Coefficient Start Address Register
−	BIOS	37	Data Page Pointer Storage Location for 128-word Data Table
−	TRN1	38	Transition Register 1
−	BRC1	39	Block Repeat Counter 1
−	BRS1	3A	Block Repeat Save 1
−	CSR	3B	Computed Single Repeat
−	RSA0H	3C	Repeat Start Address 0
−	RSA0L	3D	
−	REA0H	3E	Repeat End Address 0
−	REA0L	3F	
−	RSA1H	40	Repeat Start Address 1
−	RSA1L	41	
−	REA1H	42	Repeat End Address 1
−	REA1L	43	
−	RPTC	44	Repeat Counter
−	IER1	45	Interrupt Mask Register 1
−	IFR1	46	Interrupt Flag Register 1
−	DBIER0	47	Debug IER0
−	DBIER1	48	Debug IER1
−	IVPD	49	Interrupt Vector Pointer DSP
−	IVPH	4A	Interrupt Vector Pointer HOST
−	ST2_55	4B	Status Register 2 for C55x
−	SSP	4C	System Stack Pointer
−	SP	4D	User Stack Pointer
−	SPH	4E	Extended Data Page Pointer for the SP and the SSP
−	CDPH	4F	Main Data Page Pointer for the CDP

3.4 Peripheral Register Description

Peripheral registers on the 5510/5510A are accessed using the port qualifier. For more information on the use of the port qualifier, see the *TMS320C55x Assembly Language Tools User's Guide* (literature number SPRU280). For detailed information on the operation of the peripherals and the functions of each of the peripheral registers, refer to the *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317).

NOTE: The CPU access latency to the peripheral memory-mapped registers is 6 CPU cycles. Following peripheral register update(s), the CPU must wait at least 6 CPU cycles before attempting to use that peripheral. When more than one peripheral register is updated in a sequence, the CPU only needs to wait following the final register write. For example, if the EMIF is being reconfigured, the CPU must wait until the very last EMIF register update takes effect before trying to access the external memory. The users should consult the respective peripheral user's guide to determine if a peripheral requires additional time to initialize itself to the new configuration after the register updates take effect.

Table 3−10. Peripheral Bus Controller Configuration Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x0001	ICR	Idle Control Register
0x0002	ISTR	Idle Status Register
0x000F	BOOT_MOD	Boot Mode Register (read only)

Table 3−11. Instruction Cache Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x1400	ICGC	I-Cache Global Control Register
0x1401	ICFL0	I-Cache Flush Line Address Register 0
0x1402	ICFL1	I-Cache Flush Line Address Register 1
0x1403	ICWC	I-Cache N-Way Control Register
0x1404	ICSTAT	I-Cache Status Register
0x1405	ICRC1	I-Cache Ramset 1 Control Register
0x1406	ICRTAG1	I-Cache Ramset 1 Tag Register
0x1407	ICRC2	I-Cache Ramset 2 Control Register
0x1408	ICRTAG2	I-Cache Ramset 2 Tag Register

Table 3−12. External Memory Interface Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x0800	EGCR	EMIF Global Control Register
0x0801	EMIRST	EMIF Global Reset Register
0x0802	EMIBE	EMIF Bus Error Status Register
0x0803	CE01	EMIF CE0 Space Control Register 1
0x0804	CE02	EMIF CE0 Space Control Register 2
0x0805	CE03	EMIF CE0 Space Control Register 3
0x0806	CE11	EMIF CE1 Space Control Register 1
0x0807	CE12	EMIF CE1 Space Control Register 2
0x0808	CE13	EMIF CE1 Space Control Register 3
0x0809	CE21	EMIF CE2 Space Control Register 1
0x080A	CE22	EMIF CE2 Space Control Register 2
0x080B	CE23	EMIF CE2 Space Control Register 3
0x080C	CE31	EMIF CE3 Space Control Register 1
0x080D	CE32	EMIF CE3 Space Control Register 2
0x080E	CE33	EMIF CE3 Space Control Register 3
0x080F	SDC1	EMIF SDRAM Control Register 1
0x0810	SDPER	EMIF SDRAM Period Register
0x0811	SDCNT	EMIF SDRAM Counter Register
0x0812	INIT	EMIF SDRAM Init Register
0x0813	SDC2	EMIF SDRAM Control Register 2

Table 3−13. DMA Configuration Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
GLOBAL REGISTER		
0x0E00	DMAGCR	DMA Global Control Register
0x0E02	DMAGSCR	DMA Software Compatibility Register
0x0E03	DMAGTCR	DMA Timeout Control Register
CHANNEL #0 REGISTERS		
0x0C00	DMACSDP0	DMA Channel 0 Source / Destination Parameters Register
0x0C01	DMACCR0	DMA Channel 0 Control Register
0x0C02	DMACICR0	DMA Channel 0 Interrupt Control Register
0x0C03	DMACSR0	DMA Channel 0 Status Register
0x0C04	DMACSSAL0	DMA Channel 0 Source Start Address Register (lower bits)
0x0C05	DMACSSAU0	DMA Channel 0 Source Start Address Register (upper bits)
0x0C06	DMACDSAL0	DMA Channel 0 Source Destination Address Register (lower bits)
0x0C07	DMACDSAU0	DMA Channel 0 Source Destination Address Register (upper bits)
0x0C08	DMACEN0	DMA Channel 0 Element Number Register
0x0C09	DMACFN0	DMA Channel 0 Frame Number Register
0x0C0A	DMACFI0/ DMACSFI0†	DMA Channel 0 Frame Index Register/ DMA Channel 0 Source Frame Index Register†
0x0C0B	DMACEI0/ DMACSEI0‡	DMA Channel 0 Element Index Register/ DMA Channel 0 Source Element Index Register‡
0x0C0C	DMACSAC0	DMA Channel 0 Source Address Counter
0x0C0D	DMACDAC0	DMA Channel 0 Destination Address Counter
0x0C0E	DMACDEI0	DMA Channel 0 Destination Element Index Register
0x0C0F	DMACDFI0	DMA Channel 0 Destination Frame Index Register
CHANNEL #1 REGISTERS		
0x0C20	DMACSDP1	DMA Channel 1 Source / Destination Parameters Register
0x0C21	DMACCR1	DMA Channel 1 Control Register
0x0C22	DMACICR1	DMA Channel 1 Interrupt Control Register
0x0C23	DMACSR1	DMA Channel 1 Status Register
0x0C24	DMACSSAL1	DMA Channel 1 Source Start Address Register (lower bits)
0x0C25	DMACSSAU1	DMA Channel 1 Source Start Address Register (upper bits)
0x0C26	DMACDSAL1	DMA Channel 1 Source Destination Address Register (lower bits)
0x0C27	DMACDSAU1	DMA Channel 1 Source Destination Address Register (upper bits)
0x0C28	DMACEN1	DMA Channel 1 Element Number Register
0x0C29	DMACFN1	DMA Channel 1 Frame Number Register
0x0C2A	DMACFI1/ DMACSFI1†	DMA Channel 1 Frame Index Register/ DMA Channel 1 Source Frame Index Register†
0x0C2B	DMACEI1/ DMACSEI1‡	DMA Channel 1 Element Index Register/ DMA Channel 1 Source Element Index Register‡
0x0C2C	DMACSAC1	DMA Channel 1 Source Address Counter
0x0C2D	DMACDAC1	DMA Channel 1 Destination Address Counter
0x0C2E	DMACDEI1	DMA Channel 1 Destination Element Index Register
0x0C2F	DMACDFI1	DMA Channel 1 Destination Frame Index Register

† On revision 1.x, the channel frame index applies to both source and destination and this register behaves as DMACFIn. On revision 2.0 and later, DMACSFIn and DMACDFIn provide separate source and destination frame indexing. Revision 2.0 and later can be programmed for software compatibility with revision 1.x through the Software Compatibility Register (DMAGSCR).

‡ On revision 1.x, the channel element index applies to both source and destination and this register behaves as DMACEIn. On revision 2.0 and later, DMACSEIn and DMACDEIn provide separate source and destination frame indexing. Revision 2.0 and later can be programmed for software compatibility with revision 1.x through the Software Compatibility Register (DMAGSCR).

Table 3−13. DMA Configuration Registers (Continued)

PORT ADDRESS	REGISTER NAME	DESCRIPTION
CHANNEL #2 REGISTERS		
0x0C40	DMACSDP2	DMA Channel 2 Source / Destination Parameters Register
0x0C41	DMACCR2	DMA Channel 2 Control Register
0x0C42	DMACICR2	DMA Channel 2 Interrupt Control Register
0x0C43	DMACSR2	DMA Channel 2 Status Register
0x0C44	DMACSSAL2	DMA Channel 2 Source Start Address Register (lower bits)
0x0C45	DMACSSAU2	DMA Channel 2 Source Start Address Register (upper bits)
0x0C46	DMACDSAL2	DMA Channel 2 Source Destination Address Register (lower bits)
0x0C47	DMACDSAU2	DMA Channel 2 Source Destination Address Register (upper bits)
0x0C48	DMACEN2	DMA Channel 2 Element Number Register
0x0C49	DMACFN2	DMA Channel 2 Frame Number Register
0x0C4A	DMACFI2/ DMACSFI2†	DMA Channel 2 Frame Index Register/ DMA Channel 2 Source Frame Index Register†
0x0C4B	DMACEI2/ DMACSEI2‡	DMA Channel 2 Element Index Register/ DMA Channel 2 Source Element Index Register‡
0x0C4C	DMACSAC2	DMA Channel 2 Source Address Counter
0x0C4D	DMACDAC2	DMA Channel 2 Destination Address Counter
0x0C4E	DMACDEI2	DMA Channel 2 Destination Element Index Register
0x0C4F	DMACDFI2	DMA Channel 2 Destination Frame Index Register
CHANNEL #3 REGISTERS		
0x0C60	DMACSDP3	DMA Channel 3 Source / Destination Parameters Register
0x0C61	DMACCR3	DMA Channel 3 Control Register
0x0C62	DMACICR3	DMA Channel 3 Interrupt Control Register
0x0C63	DMACSR3	DMA Channel 3 Status Register
0x0C64	DMACSSAL3	DMA Channel 3 Source Start Address Register (lower bits)
0x0C65	DMACSSAU3	DMA Channel 3 Source Start Address Register (upper bits)
0x0C66	DMACDSAL3	DMA Channel 3 Source Destination Address Register (lower bits)
0x0C67	DMACDSAU3	DMA Channel 3 Source Destination Address Register (upper bits)
0x0C68	DMACEN3	DMA Channel 3 Element Number Register
0x0C69	DMACFN3	DMA Channel 3 Frame Number Register
0x0C6A	DMACFI3/ DMACSFI3†	DMA Channel 3 Frame Index Register/ DMA Channel 3 Source Frame Index Register†
0x0C6B	DMACEI3/ DMACSEI3‡	DMA Channel 3 Element Index Register/ DMA Channel 3 Source Element Index Register‡
0x0C6C	DMACSAC3	DMA Channel 3 Source Address Counter
0x0C6D	DMACDAC3	DMA Channel 3 Destination Address Counter
0x0C6E	DMACDEI3	DMA Channel 3 Destination Element Index Register
0x0C6F	DMACDFI3	DMA Channel 3 Destination Frame Index Register

† On revision 1.x, the channel frame index applies to both source and destination and this register behaves as DMACFIn. On revision 2.0 and later, DMACSFIn and DMACDFIn provide separate source and destination frame indexing. Revision 2.0 and later can be programmed for software compatibility with revision 1.x through the Software Compatibility Register (DMAGSCR).

‡ On revision 1.x, the channel element index applies to both source and destination and this register behaves as DMACEIn. On revision 2.0 and later, DMACSEIn and DMACDEIn provide separate source and destination frame indexing. Revision 2.0 and later can be programmed for software compatibility with revision 1.x through the Software Compatibility Register (DMAGSCR).

Table 3−13. DMA Configuration Registers (Continued)

PORT ADDRESS	REGISTER NAME	DESCRIPTION
CHANNEL #4 REGISTERS		
0x0C80	DMACSDP4	DMA Channel 4 Source / Destination Parameters Register
0x0C81	DMACCR4	DMA Channel 4 Control Register
0x0C82	DMACICR4	DMA Channel 4 Interrupt Control Register
0x0C83	DMACSR4	DMA Channel 4 Status Register
0x0C84	DMACSSAL4	DMA Channel 4 Source Start Address Register (lower bits)
0x0C85	DMACSSAU4	DMA Channel 4 Source Start Address Register (upper bits)
0x0C86	DMACDSAL4	DMA Channel 4 Source Destination Address Register (lower bits)
0x0C87	DMACDSAU4	DMA Channel 4 Source Destination Address Register (upper bits)
0x0C88	DMACEN4	DMA Channel 4 Element Number Register
0x0C89	DMACFN4	DMA Channel 4 Frame Number Register
0x0C8A	DMACFI4/ DMACSFI4†	DMA Channel 4 Frame Index Register/ DMA Channel 4 Source Frame Index Register†
0x0C8B	DMACEI4/ DMACSEI4‡	DMA Channel 4 Element Index Register/ DMA Channel 4 Source Element Index Register‡
0x0C8C	DMACSAC4	DMA Channel 4 Source Address Counter
0x0C8D	DMACDAC4	DMA Channel 4 Destination Address Counter
0x0C8E	DMACDEI4	DMA Channel 4 Destination Element Index Register
0x0C8F	DMACDFI4	DMA Channel 4 Destination Frame Index Register
CHANNEL #5 REGISTERS		
0x0CA0	DMACSDP5	DMA Channel 5 Source / Destination Parameters Register
0x0CA1	DMACCR5	DMA Channel 5 Control Register
0x0CA2	DMACICR5	DMA Channel 5 Interrupt Control Register
0x0CA3	DMACSR5	DMA Channel 5 Status Register
0x0CA4	DMACSSAL5	DMA Channel 5 Source Start Address Register (lower bits)
0x0CA5	DMACSSAU5	DMA Channel 5 Source Start Address Register (upper bits)
0x0CA6	DMACDSAL5	DMA Channel 5 Source Destination Address Register (lower bits)
0x0CA7	DMACDSAU5	DMA Channel 5 Source Destination Address Register (upper bits)
0x0CA8	DMACEN5	DMA Channel 5 Element Number Register
0x0CA9	DMACFN5	DMA Channel 5 Frame Number Register
0x0CAA	DMACFI5/ DMACSFI5†	DMA Channel 5 Frame Index Register/ DMA Channel 5 Source Frame Index Register†
0x0CAB	DMACEI5/ DMACSEI5‡	DMA Channel 5 Element Index Register/ DMA Channel 5 Source Element Index Register‡
0x0CAC	DMACSAC5	DMA Channel 5 Source Address Counter
0x0CAD	DMACDAC5	DMA Channel 5 Destination Address Counter
0x0CAE	DMACDEI5	DMA Channel 5 Destination Element Index Register
0x0CAF	DMACDFI5	DMA Channel 5 Destination Frame Index Register

† On revision 1.x, the channel frame index applies to both source and destination and this register behaves as DMACFIn. On revision 2.0 and later, DMACSFIn and DMACDFIn provide separate source and destination frame indexing. Revision 2.0 and later can be programmed for software compatibility with revision 1.x through the Software Compatibility Register (DMAGSCR).

‡ On revision 1.x, the channel element index applies to both source and destination and this register behaves as DMACEIn. On revision 2.0 and later, DMACSEIn and DMACDEIn provide separate source and destination frame indexing. Revision 2.0 and later can be programmed for software compatibility with revision 1.x through the Software Compatibility Register (DMAGSCR).

Table 3−14. Clock Generator Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x1C00	CLKMD	Clock Mode Register

Table 3−15. Timer Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x1000	TIM0	Timer 0 Count Register
0x1001	PRD0	Timer 0 Period Register
0x1002	TCR0	Timer 0 Timer Control Register
0x1003	PRSC0	Timer 0 Timer Prescaler Register
0x2400	TIM1	Timer 1 Timer Count Register
0x2401	PRD1	Timer 1 Period Register
0x2402	TCR1	Timer 1 Timer Control Register
0x2403	PRSC1	Timer 1 Timer Prescaler Register

Table 3−16. Multichannel Serial Port #0 Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x2800	DRR20	McBSP 0 Data Receive Register 2
0x2801	DRR10	McBSP 0 Data Receive Register 1
0x2802	DXR20	McBSP 0 Data Transmit Register 2
0x2803	DXR10	McBSP 0 Data Transmit Register 1
0x2804	SPCR20	McBSP 0 Serial Port Control Register 2
0x2805	SPCR10	McBSP 0 Serial Port Control Register 1
0x2806	RCR20	McBSP 0 Receive Control Register 2
0x2807	RCR10	McBSP 0 Receive Control Register 1
0x2808	XCR20	McBSP 0 Transmit Control Register 2
0x2809	XCR10	McBSP 0 Transmit Control Register 1
0x280A	SRGR20	McBSP 0 Sample Rate Generator Register 2
0x280B	SRGR10	McBSP 0 Sample Rate Generator Register 1
0x280C	MCR20	McBSP 0 Multichannel Control Register 2
0x280D	MCR10	McBSP 0 Multichannel Control Register 1
0x280E	RCERA0	McBSP 0 Receive Channel Enable Register Partition A
0x280F	RCERB0	McBSP 0 Receive Channel Enable Register Partition B
0x2810	XCERA0	McBSP 0 Transmit Channel Enable Register Partition A
0x2811	XCERB0	McBSP 0 Transmit Channel Enable Register Partition B
0x2812	PCR0	McBSP 0 Pin Control Register
0x2813	RCERC0	McBSP 0 Receive Channel Enable Register Partition C
0x2814	RCERD0	McBSP 0 Receive Channel Enable Register Partition D
0x2815	XCERC0	McBSP 0 Transmit Channel Enable Register Partition C
0x2816	XCERD0	McBSP 0 Transmit Channel Enable Register Partition D
0x2817	RCERE0	McBSP 0 Receive Channel Enable Register Partition E
0x2818	RCERF0	McBSP 0 Receive Channel Enable Register Partition F
0x2819	XCERE0	McBSP 0 Transmit Channel Enable Register Partition E
0x281A	XCERF0	McBSP 0 Transmit Channel Enable Register Partition F
0x281B	RCERG0	McBSP 0 Receive Channel Enable Register Partition G
0x281C	RCERH0	McBSP 0 Receive Channel Enable Register Partition H
0x281D	XCERG0	McBSP 0 Transmit Channel Enable Register Partition G
0x281E	XCERH0	McBSP 0 Transmit Channel Enable Register Partition H

Table 3−17. Multichannel Serial Port #1 Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x2C00	DRR21	McBSP 1 Data Receive Register 2
0x2C01	DRR11	McBSP 1 Data Receive Register 1
0x2C02	DXR21	McBSP 1 Data Transmit Register 2
0x2C03	DXR11	McBSP 1 Data Transmit Register 1
0x2C04	SPCR21	McBSP 1 Serial Port Control Register 2
0x2C05	SPCR11	McBSP 1 Serial Port Control Register 1
0x2C06	RCR21	McBSP 1 Receive Control Register 2
0x2C07	RCR11	McBSP 1 Receive Control Register 1
0x2C08	XCR21	McBSP 1 Transmit Control Register 2
0x2C09	XCR11	McBSP 1 Transmit Control Register 1
0x2C0A	SRGR21	McBSP 1 Sample Rate Generator Register 2
0x2C0B	SRGR11	McBSP 1 Sample Rate Generator Register 1
0x2C0C	MCR21	McBSP 1 Multichannel Control Register 2
0x2C0D	MCR11	McBSP 1 Multichannel Control Register 1
0x2C0E	RCERA1	McBSP 1 Receive Channel Enable Register Partition A
0x2C0F	RCERB1	McBSP 1 Receive Channel Enable Register Partition B
0x2C10	XCERA1	McBSP 1 Transmit Channel Enable Register Partition A
0x2C11	XCERB1	McBSP 1 Transmit Channel Enable Register Partition B
0x2C12	PCR1	McBSP 1 Pin Control Register
0x2C13	RCERC1	McBSP 1 Receive Channel Enable Register Partition C
0x2C14	RCERD1	McBSP 1 Receive Channel Enable Register Partition D
0x2C15	XCERC1	McBSP 1 Transmit Channel Enable Register Partition C
0x2C16	XCERD1	McBSP 1 Transmit Channel Enable Register Partition D
0x2C17	RCERE1	McBSP 1 Receive Channel Enable Register Partition E
0x2C18	RCERF1	McBSP 1 Receive Channel Enable Register Partition F
0x2C19	XCERE1	McBSP 1 Transmit Channel Enable Register Partition E
0x2C1A	XCERF1	McBSP 1 Transmit Channel Enable Register Partition F
0x2C1B	RCERG1	McBSP 1 Receive Channel Enable Register Partition G
0x2C1C	RCERH1	McBSP 1 Receive Channel Enable Register Partition H
0x2C1D	XCERG1	McBSP 1 Transmit Channel Enable Register Partition G
0x2C1E	XCERH1	McBSP 1 Transmit Channel Enable Register Partition H

Table 3−18. Multichannel Serial Port #2 Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x3000	DRR22	McBSP 2 Data Receive Register 2
0x3001	DRR12	McBSP 2 Data Receive Register 1
0x3002	DXR22	McBSP 2 Data Transmit Register 2
0x3003	DXR12	McBSP 2 Data Transmit Register 1
0x3004	SPCR22	McBSP 2 Serial Port Control Register 2
0x3005	SPCR12	McBSP 2 Serial Port Control Register 1
0x3006	RCR22	McBSP 2 Receive Control Register 2
0x3007	RCR12	McBSP 2 Receive Control Register 1
0x3008	XCR22	McBSP 2 Transmit Control Register 2
0x3009	XCR12	McBSP 2 Transmit Control Register 1
0x300A	SRGR22	McBSP 2 Sample Rate Generator Register 2
0x300B	SRGR12	McBSP 2 Sample Rate Generator Register 1
0x300C	MCR22	McBSP 2 Multichannel Control Register 2
0x300D	MCR12	McBSP 2 Multichannel Control Register 1
0x300E	RCERA2	McBSP 2 Receive Channel Enable Register Partition A
0x300F	RCERB2	McBSP 2 Receive Channel Enable Register Partition B
0x3010	XCERA2	McBSP 2 Transmit Channel Enable Register Partition A
0x3011	XCERB2	McBSP 2 Transmit Channel Enable Register Partition B
0x3012	PCR2	McBSP 2 Pin Control Register
0x3013	RCERC2	McBSP 2 Receive Channel Enable Register Partition C
0x3014	RCERD2	McBSP 2 Receive Channel Enable Register Partition D
0x3015	XCERC2	McBSP 2 Transmit Channel Enable Register Partition C
0x3016	XCERD2	McBSP 2 Transmit Channel Enable Register Partition D
0x3017	RCERE2	McBSP 2 Receive Channel Enable Register Partition E
0x3018	RCERF2	McBSP 2 Receive Channel Enable Register Partition F
0x3019	XCERE2	McBSP 2 Transmit Channel Enable Register Partition E
0x301A	XCERF2	McBSP 2 Transmit Channel Enable Register Partition F
0x301B	RCERG2	McBSP 2 Receive Channel Enable Register Partition G
0x301C	RCERH2	McBSP 2 Receive Channel Enable Register Partition H
0x301D	XCERG2	McBSP 2 Transmit Channel Enable Register Partition G
0x301E	XCERH2	McBSP 2 Transmit Channel Enable Register Partition H

Table 3−19. GPIO Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x3400	IODIR	General-purpose I/O Direction Register
0x3401	IODATA	General-purpose I/O Data Register

Table 3−20. Device Revision ID Registers

PORT ADDRESS	REGISTER NAME	DESCRIPTION
0x3800 − 0x3803	DieID[63:0]	Factory Die Identification†
0x3804	RevID[15:0]	Identifies silicon revision Revision 2.1: 0x6511 Revision 2.2: 0x6512

† The Die_ID register contains factory identification information and does not require any intervention from the user. When the DIE_ID register is used, at least 3 TCK clocks after reset are required to properly initialize the register contents.

3.5 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 3−21. The locations of the interrupt vectors are defined as an offset from the location defined in the interrupt vector pointers (IVPD and IVPH). For more detailed information about the interrupt vector pointers and interrupts, see the *TMS320C55x DSP CPU Reference Guide* (literature number SPRU371).

Table 3−21. Interrupt Table

NAME	SOFTWARE (TRAP) EQUIVALENT	OFFSET LOCATION (HEX BYTES)	PRIORITY	FUNCTION
$\overline{\text{RESET}}$	SINT0	0	0	Reset (hardware and software)
$\overline{\text{NMI}}$	SINT1	8	1	Nonmaskable interrupt
$\overline{\text{INT0}}$	SINT2	10	3	External interrupt #0
$\overline{\text{INT2}}$	SINT3	18	5	External interrupt #2
TINT0	SINT4	20	6	Timer #0 interrupt
RINT0	SINT5	28	7	McBSP #0 receive interrupt
RINT1	SINT6	30	9	McBSP #1 receive interrupt
XINT1	SINT7	38	10	McBSP #1 transmit interrupt
−	SINT8	40	11	Software interrupt #8
DMAC1	SINT9	48	13	DMA Channel #1 interrupt
DSPINT	SINT10	50	14	Interrupt from host (EHPI)
$\overline{\text{INT3}}$	SINT11	58	15	External interrupt #3
RINT2	SINT12	60	17	McBSP #2 receive interrupt
XINT2	SINT13	68	18	McBSP #2 transmit interrupt
DMAC4	SINT14	70	21	DMA Channel #4 interrupt
DMAC5	SINT15	78	22	DMA Channel #5 interrupt
$\overline{\text{INT1}}$	SINT16	80	4	External interrupt #1
XINT0	SINT17	88	8	McBSP #0 transmit interrupt
DMAC0	SINT18	90	12	DMA Channel #0 interrupt
INT4	SINT19	98	16	External interrupt #4
DMAC2	SINT20	A0	19	DMA Channel #2 interrupt
DMAC3	SINT21	A8	20	DMA Channel #3 interrupt
TINT1	SINT22	B0	23	Timer #1 interrupt
$\overline{\text{INT5}}$	SINT23	B8	24	External interrupt #5
BERR	SINT24	C0	2	Bus Error interrupt
DLOG	SINT25	C8	25	Data Log interrupt
RTOS	SINT26	D0	26	Real-time Operating System interrupt
−	SINT27	D8	27	Software interrupt #27
−	SINT28	E0	28	Software interrupt #28
−	SINT29	E8	29	Software interrupt #29
−	SINT30	F0	30	Software interrupt #30
	SINT31	F8	31	Software interrupt #31

3.5.1 IFR and IER Registers

The Interrupt Enable Registers (IER0 and IER1) control which interrupts will be masked or enabled during normal operation. The Interrupt Flag Registers (IFR0 and IFR1) contain flags that indicate interrupts that are currently pending.

The Debug Interrupt Enable Registers (DBIER0 and DBIER1) are used only when the CPU is *halted* in the real-time emulation mode. If the CPU is *running* in real-time mode, the standard interrupt processing (IER0/1) is used and DBIER0/1 are ignored.

A maskable interrupt enabled in a DBIER0/1 is defined as a time-critical interrupt. When the CPU is halted in the real-time mode, the only interrupts that are serviced are time-critical interrupts that are also enabled in an interrupt enable register (IER0 or IER1)

Write the DBIER0/1 to enable or disable time-critical interrupts. To enable an interrupt, set its corresponding bit. To disable an interrupt, clear its corresponding bit. Note that DBIER0/1 are not affected by a software reset instruction or by a DSP hardware reset. Initialize these registers before using the real-time emulation mode.

The bit layouts of these registers for each interrupt are shown in Figure 3−7.

15	14	13	12	11	10	9	8
DMAC5	DMAC4	XINT2	RINT2	INT3	DSPINT	DMAC1	Reserved

7	6	5	4	3	2	1	0
XINT1	RINT1	RINT0	TINT0	INT2	INT0	Reserved	

Figure 3−7. IFR0, IER0, DBIFR0, and DBIER0 Bit Locations

The IFR1 (Interrupt Flag Register 1) and IER1 (Interrupt Enable Register 1) bit layouts are shown in Figure 3−8.

15	11	10	9	8
Reserved		RTOS	DLOG	BERR

7	6	5	4	3	2	1	0
INT5	TINT1	DMAC3	DMAC2	INT4	DMAC0	XINT0	INT1

Figure 3−8. IFR1, IER1, DBIFR1, and DBIER1 Bit Locations

3.5.2 Interrupt Timing

The external interrupts ($\overline{\text{NMI}}$ and $\overline{\text{INTx}}$) are automatically synchronized to the CPU. The interrupt inputs are sampled on the falling edges of the CPU clock. A sequence on the interrupt pin of 1-0-0-0 on consecutive cycles is required for an interrupt to be detected. Therefore, the minimum low pulse duration on the external interrupts on the 5510/5510A is three CPU clock periods.

3.6 Notices Concerning CLKOUT Operation

3.6.1 CLKOUT Voltage Level

On the TMS320VC5510/5510A, CLKOUT is driven at CV_{DD} supply voltage. This voltage level may be too low to interface to some devices. In that event, buffers may need to be employed to support interfacing CLKOUT.

3.6.2 CLKOUT Value During Reset

During reset, the CLKOUT pin is driven to a logic 1.

4 Support

4.1 Notices Concerning JTAG (IEEE 1149.1) Boundary Scan Test Capability

4.1.1 Initialization Requirements for Boundary Scan Test

The TMS320VC5510/5510A uses the JTAG port for boundary scan tests, emulation capability and factory test purposes. To use boundary scan test, the EMU0 and EMU1/$\overline{\text{OFF}}$ pins must be held LOW through a rising edge of the $\overline{\text{TRST}}$ signal prior to the first scan. This operation selects the appropriate TAP control for boundary scan. If at any time during a boundary scan test a rising edge of $\overline{\text{TRST}}$ occurs when EMU0 or EMU1/$\overline{\text{OFF}}$ are not low, a factory test mode may be selected preventing boundary scan test from being completed. For this reason, it is recommended that EMU0 and EMU1/$\overline{\text{OFF}}$ be pulled or driven low at all times during boundary scan test.

4.1.2 Boundary Scan Description Language (BSDL) Model

BSDL models are available on the web in the TMS320VC5510/5510A product folder under the “simulation models” section.

4.2 Documentation Support

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the TMS320C5000™ platform of DSPs:

- *TMS320C55x™ DSP Functional Overview* (literature number SPRU312)
- *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317)
- *TMS320C55x DSP CPU Reference Guide* (literature number SPRU371)
- *TMS320C55x DSP CPU Programmer’s Reference Supplement* (literature number SPRU652)
- *TMS320C55x Assembly Language Tools User’s Guide* (literature number SPRU280)
- *TMS320C55x Hardware Extensions for Image/Video Applications Programmer’s Reference* (literature number SPRU098)
- *TMS320C55x Image/Video Processing Library Programmer’s Reference* (literature number SPRU037)
- *TMS320VC5510 DSP Instruction Cache Reference Guide* (literature number SPRU576)
- *TMS320VC5501/5502/5503/5507/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide* (literature number SPRU592)
- *TMS320VC5503/5507/5509/5510 DSP Direct Memory Access (DMA) Controller Reference Guide* (literature number SPRU587)
- *TMS320VC5510 DSP Host Port Interface (HPI) Reference Guide* (literature number SPRU588)
- *TMS320VC5503/5507/5509/5510 DSP Timers Reference Guide* (literature number SPRU595)
- *Using the TMS320VC5510 Bootloader* application report (literature number SPRA763)
- *TMS320VC5510/5510A Hardware Designer’s Resource Guide* (literature number SPRAA43)
- *TMS320VC5510/5510A Digital Signal Processors Silicon Errata* (literature number SPRZ008)
- Device-specific data sheets
- Complete user’s guides
- Development support tools
- Hardware and software application reports

The reference set describes in detail the TMS320C55x DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 DSP customers on product information.

Information regarding Texas Instruments (TI) DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

TMS320 and TMS320C5000 are trademarks of Texas Instruments.

4.3 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320VC5510A). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

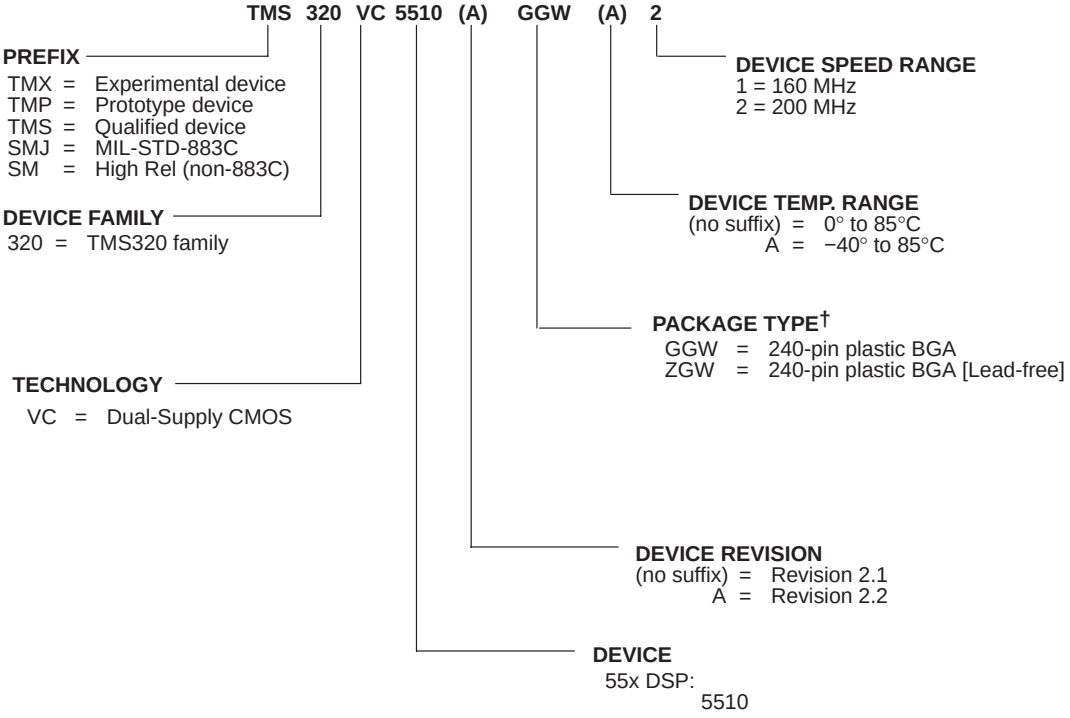
TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

4.4 TMS320VC5510/5510A Device Nomenclature



† BGA = Ball Grid Array

Figure 4−1. Device Nomenclature for the TMS320VC5510/5510A

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320VC5510/5510A DSPs.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions unless otherwise specified.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” (Section 5.2) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” (Section 5.3) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All supply voltage values (core and I/O) are with respect to V_{SS}. Figure 5−1 provides the test load circuit values for a 3.3-V device. Measured timing information contained in this data manual is based on the test load setup and conditions shown in Figure 5−1.

5.2 Electrical Specifications

This section provides the absolute maximum ratings for the TMS320VC5510/5510A DSPs.

Supply voltage I/O range, DV_{DD} . . . . . − 0.3 V to 4.0 V
Supply voltage core range, CV_{DD} . . . . . − 0.3 V to 2.0 V
Input voltage range, V_I . . . . . − 0.3 V to 4.5 V
Output voltage range, V_O . . . . . − 0.3 V to 4.5 V
Operating case temperature range, T_C: (Commercial) . . . . . 0°C to 85°C
(Extended) . . . . . − 40°C to 85°C
Storage temperature range T_{stg} . . . . . − 55°C to 150°C

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage, I/O		3.0	3.3	3.6	V
CV_{DD}	Device supply voltage, core	Prototype revisions 2.1 and 2.2 and production silicon†	1.55	1.6	1.65	V
V_{SS}	Supply voltage, GND			0		V
V_{IH}	High-level input voltage, I/O	Hysteresis inputs DV_{DD} = 3.3 ± 0.3 V	2.4		DV_{DD} + 0.3	V
		All other inputs	2.0		DV_{DD} + 0.3	
V_{IL}	Low-level input voltage, I/O	Hysteresis inputs DV_{DD} = 3.3 ± 0.3 V	−0.3		0.8	V
		All other inputs	−0.3		0.8	
I_{OH}	High-level output current	All outputs			−8	mA
I_{OL}	Low-level output current	All outputs			8	mA
T_C	Operating case temperature	Prototype (TMX) and Commercial Temperature Range Production Devices	0		85	°C
		Extended Temperature Range Production (TMS) devices	−40		85	

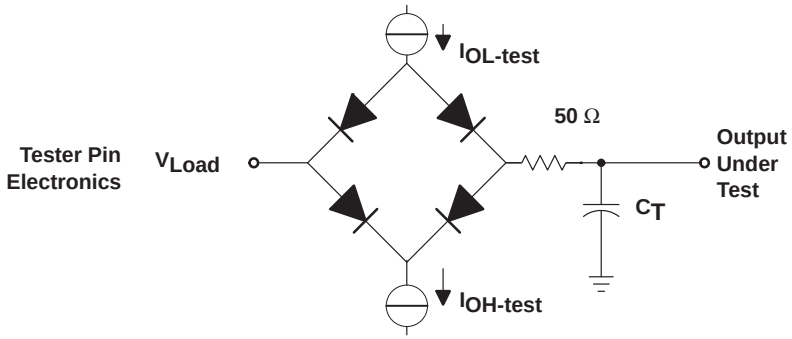
† See the *TMS320VC5510/5510A Digital Signal Processors Silicon Errata* (literature number SPRZ008) for further clarification and distinguishing markings.

5.4 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All output except CLKOUT	DV_{DD} = 3.3 ± 0.3 V, I_{OH} = MAX	2.4			V
		CLKOUT	CV_{DD} = 1.6 ± 0.05 V, I_{OH} = MAX	1.24			
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.4	V
I_{IZ}	Input current for outputs in high impedance	Output-only or input/output pins with bus holders	Bus holders enabled CV_{DD} = MAX, V_O = V_{SS} to V_{DD}	− 275		275	µA
		All other output-only or input/output pins	Bus holders disabled CV_{DD} = MAX, V_O = V_{SS} to V_{DD}	− 5		5	
I_I	Input current	Input pins with internal pulldown	CV_{DD} = MAX, V_I = V_{SS} to V_{DD}	− 5		300	µA
		Input pins with internal pullup	Pullup enabled CV_{DD} = MAX, V_I = V_{SS} to V_{DD}	− 300		5	
		All other input-only pins or input-only pins with pullup/pulldown disabled	CV_{DD} = MAX, V_I = V_{SS} to V_{DD}	− 5		5	
I_{DDC}	CV_{DD} supply current, CPU + internal memory access †		CV_{DD} = 1.6 V, CPU clock = 200 MHz T_C = 25°C		112		mA
I_{DDP}	DV_{DD} supply current, pins active ‡		DV_{DD} = 3.3 V CPU clock = 100 MHz T_C = 25°C		8		mA
I_{DDC}	CV_{DD} supply current, standby Only CLKGEN domain enabled, PLL enabled.		CV_{DD} = 1.6 V 10-MHz clock input, DPLL mode = x 20 T_C = 25°C		32		mA
I_{DDC}	CV_{DD} supply current, standby All domains idled.		CV_{DD} = 1.6 V input clock stopped, T_C = 25°C		69		µA
			CV_{DD} = 1.6 V input clock stopped, T_C = 55°C		374		µA
			CV_{DD} = 1.6 V input clock stopped, T_C = 85°C		976		µA
I_{DDP}	DV_{DD} supply current, standby All domains idled.		DV_{DD} = 3.3 V no pin activity, T_C = 25°C		10		µA
			DV_{DD} = 3.3 V no pin activity, T_C = 55°C		10		µA
			DV_{DD} = 3.3 V no pin activity, T_C = 85°C		10		µA
C_i	Input capacitance				3		pF
C_o	Output capacitance				3		pF

† Test Condition: CPU executing 75% Dual-MAC / 25% ADD with moderate data bus activity (table of sine values). CPU and CLKGEN domains are active. All other domains are idled. The DPLL is enabled.

‡ Test Condition: One word of a table of 16-bit sine values is written to the EMIF each microsecond (16 Mbps). Each EMIF output pin is connected to a 10-pF load capacitance.



Where: $I_{OL-test}$ = +2 mA (all outputs)
$I_{OH-test}$ = −2 mA (all outputs)
V_{Load} = 50% of DVdd
C_T = 15 pF typical load circuit capacitance.

Figure 5−1. 3.3-V Test Load Circuit

5.5 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:	
a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don't care level

Letters and symbols and their meanings:	
H	High
L	Low
V	Valid
Z	High impedance

5.6 Clock Options

This section provides the timing requirements and switching characteristics for the various clock options available on the 5510/5510A.

5.6.1 Clock Generation in Bypass Mode (DPLL Disabled)

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of one, two, or four to generate the internal CPU clock cycle. The divide factor (D) is set in the BYPASS_DIV field of the clock mode register. The contents of this field only affect clock generation while the device is in bypass mode. In this mode, the digital phase-locked loop (DPLL) clock synthesis is disabled.

Table 5−1 and Table 5−2 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−2).

Table 5−1. CLKIN in Bypass Mode Timing Requirements

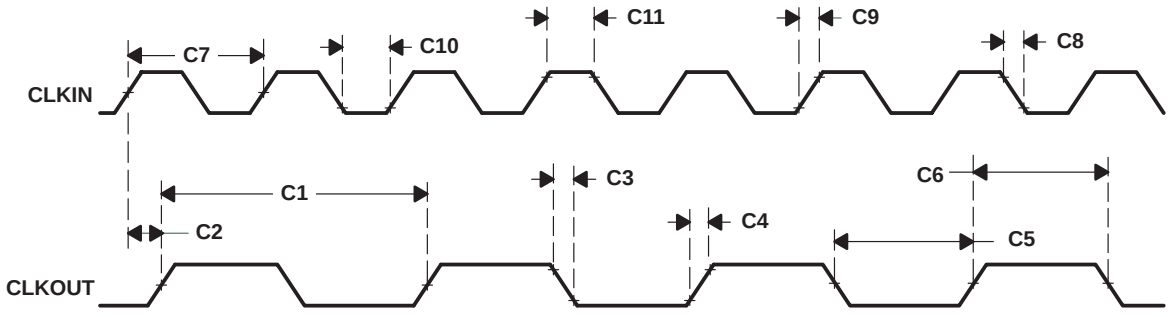
NO.			VC5510/5510A-160		VC5510/5510A-200		UNIT
			MIN	MAX	MIN	MAX	
C7	$t_{c(CI)}$	Cycle time, CLKIN	20	†	20	†	ns
C8	$t_{f(CI)}$	Fall time, CLKIN		6		6	ns
C9	$t_{r(CI)}$	Rise time, CLKIN		6		6	ns
C10	$t_{w(CIL)}$	Pulse duration, CLKIN low	4		4		ns
C11	$t_{w(CIH)}$	Pulse duration, CLKIN high	4		4		ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.

Table 5−2. CLKOUT in Bypass Mode Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160			VC5510/5510A-200			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
C1	$t_{c(CO)}$	Cycle time, CLKOUT	20	$t_{c(CI)}/N$‡		20	$t_{c(CI)}/N$‡		ns
C2	$t_{d(CI-CO)}$	Delay time, CLKIN high/low to CLKOUT high/low	1	7	14	1	7	14	ns
C3	$t_{f(CO)}$	Fall time, CLKOUT		1			1		ns
C4	$t_{r(CO)}$	Rise time, CLKOUT		1			1		ns
C5	$t_{w(COL)}$	Pulse duration, CLKOUT low	H−1		H+1	H−1		H+1	ns
C6	$t_{w(COH)}$	Pulse duration, CLKOUT high	H−1		H+1	H−1		H+1	ns

‡ N = Clock frequency synthesis factor



NOTE A: The relationship of CLKIN to CLKOUT depends on the divide factor chosen. The waveform relationship shown in Figure 5−2 is intended to illustrate the timing parameters only and may differ based on configuration.

Figure 5−2. Bypass Mode Clock Timing

5.6.2 Clock Generation in Lock Mode (DPLL Synthesis Enabled)

The frequency of the reference clock provided at the CLKIN pin can be multiplied by a synthesis factor of N to generate the internal CPU clock cycle. The synthesis factor is determined by:

$$N = \frac{M}{D_L}$$

where: M = the multiply factor set in the PLL_MULT field of the clock mode register,
D_L = the divide factor set in the PLL_DIV field of the clock mode register

Valid values for M are (multiply by) 2 to 31. Valid values for D_L are (divide by) 1, 2, 3, and 4.

For detailed information on clock generation configuration, see the *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317).

Table 5−3 and Table 5−4 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−3).

Table 5−3. CLKIN in Lock Mode Timing Requirements

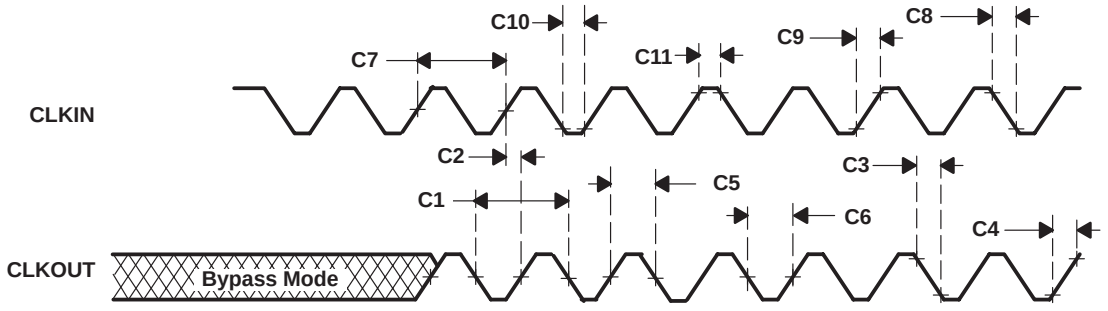
NO.				VC5510/5510A-160		VC5510/5510A-200		UNIT
				MIN	MAX	MIN	MAX	
C7	$t_{c(CI)}$	Cycle time, CLKIN	DPLL synthesis enabled	20†	400	20†	400	ns
C8	$t_{f(CI)}$	Fall time, CLKIN			6		6	ns
C9	$t_{r(CI)}$	Rise time, CLKIN			6		6	ns
C10	$t_{w(CIL)}$	Pulse duration, CLKIN low		4		4		ns
C11	$t_{w(CIH)}$	Pulse duration, CLKIN high		4		4		ns

† The clock frequency synthesis factor and minimum CLKIN cycle time should be chosen such that the resulting CLKOUT cycle time is within the specified range ($t_{c(CO)}$).

Table 5−4. CLKOUT in Lock Mode Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160			VC5510/5510A-200			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
C1	$t_{c(CO)}$	Cycle time, CLKOUT	6.25	$t_{c(CI)}/N$‡		5	$t_{c(CI)}/N$‡		ns
C2	$t_{d(CI-CO)}$	Delay time, CLKIN high/low to CLKOUT high/low	1	7	14	1	7	14	ns
C3	$t_{f(CO)}$	Fall time, CLKOUT		1			1		ns
C4	$t_{r(CO)}$	Rise time, CLKOUT		1			1		ns
C5	$t_{w(COL)}$	Pulse duration, CLKOUT low	H−1		H+1	H−1		H+1	ns
C6	$t_{w(COH)}$	Pulse duration, CLKOUT high	H−1		H+1	H−1		H+1	ns

‡ N = Clock frequency synthesis factor



NOTE A: The waveform relationship of CLKIN to CLKOUT depends on the multiply and divide factors chosen. The waveform relationship shown in Figure 5−3 is intended to illustrate the timing parameters only and may differ based on configuration.

Figure 5−3. External Multiply-by-N Clock Timing

5.7 Memory Timing

5.7.1 Asynchronous Memory Timing

Table 5−5 and Table 5−6 assume testing over recommended operating conditions (see Figure 5−4 and Figure 5−5). Note that the asynchronous memory interface is read-only when configured as 8-bit mode. Asynchronous writes in 8-bit mode are not supported.

Table 5−5. Asynchronous Memory Cycles Timing Requirements

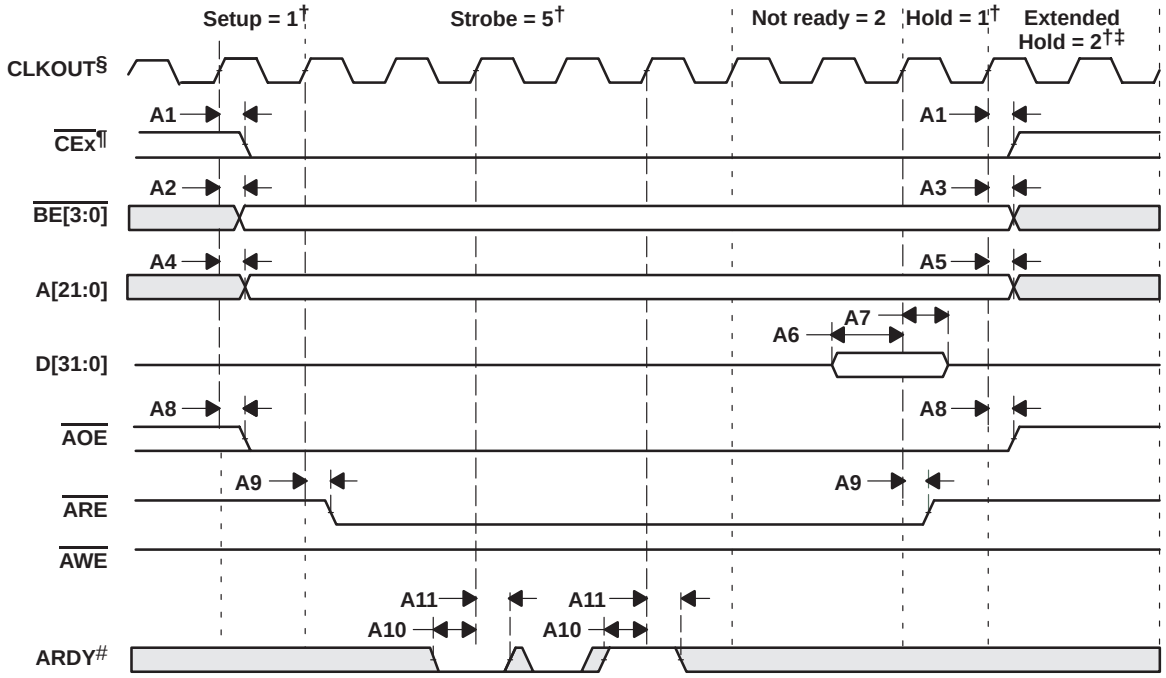
NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
A6	$t_{su(DV-COH)}$	Setup time, read data valid before CLKOUT high†	6		ns
A7	$t_{h(COH-DV)}$	Hold time, read data valid after CLKOUT high	0		ns
A10	$t_{su(ARDY-COH)}$	Setup time, ARDY valid before CLKOUT high	7		ns
A11	$t_{h(COH-ARDY)}$	Hold time, ARDY valid after CLKOUT high	0		ns

† To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.

Table 5−6. Asynchronous Memory Cycles Switching Characteristics‡§

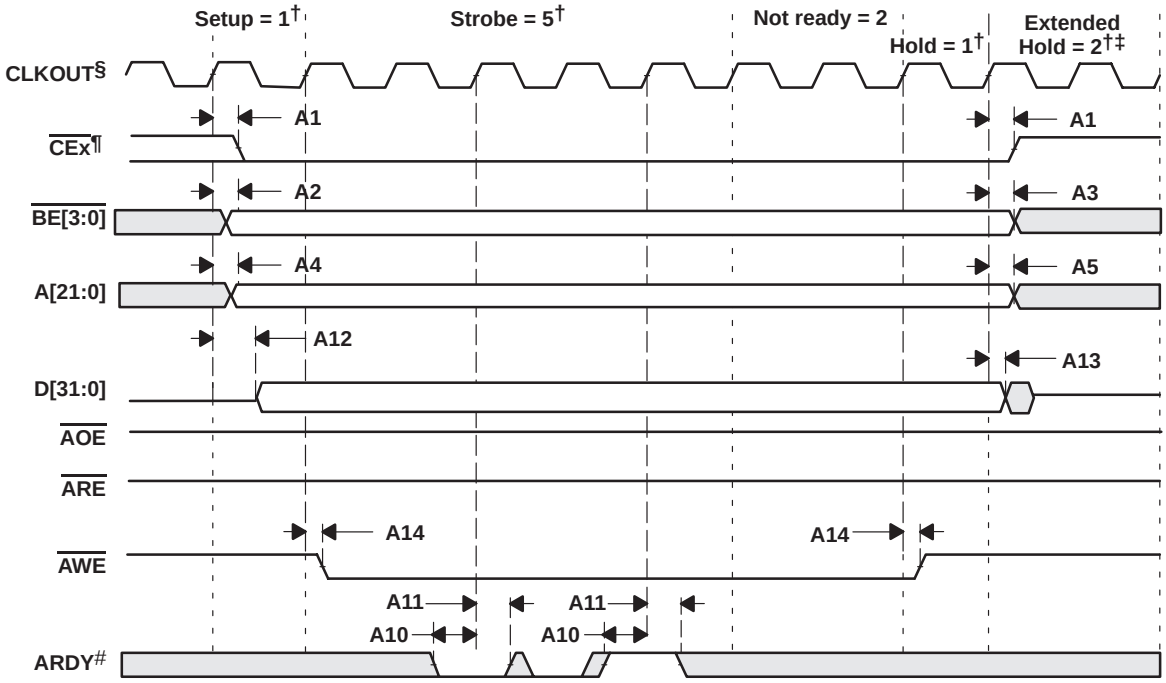
NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
A1	$t_{d(COH-CEV)}$	Delay time, CLKOUT high to $\overline{CEx}$ transition	−2	4	ns
A2	$t_{d(COH-BEV)}$	Delay time, CLKOUT high to $\overline{BEx}$ valid		4	ns
A3	$t_{d(COH-BEIV)}$	Delay time, CLKOUT high to $\overline{BEx}$ invalid	−2		ns
A4	$t_{d(COH-AV)}$	Delay time, CLKOUT high to address valid		4	ns
A5	$t_{d(COH-AIV)}$	Delay time, CLKOUT high to address invalid	−2		ns
A8	$t_{d(COH-AOEV)}$	Delay time, CLKOUT high to $\overline{AOE}$ valid	−2	4	ns
A9	$t_{d(COH-AREV)}$	Delay time, CLKOUT high to $\overline{ARE}$ valid	−2	4	ns
A12	$t_{d(COH-DV)}$	Delay time, CLKOUT high to data valid (write)		4	ns
A13	$t_{d(COH-DIV)}$	Delay time, CLKOUT high to data invalid (write)	−2		ns
A14	$t_{d(COH-AWEV)}$	Delay time, CLKOUT high to $\overline{AWE}$ valid	−2	4	ns

‡ The minimum delay is also the minimum output hold after CLKOUT high.
§ All timings referenced to CLKOUT assume CLKOUT represents the internal CPU clock (divide-by-1 mode).



† Setup, Strobe, Hold, and Extended Hold are programmable in the EMIF. The programmable Hold period is not associated with the activity of the HOLD and HOLDA signals.
‡ The extended hold time is programmable in the EMIF and is only present when consecutive memory accesses are made to different CEx spaces, or are of different types (read/write).
§ All timings referenced to CLKOUT assume CLKOUT is the same frequency as the internal CPU clock (divide-by-1 mode).
¶ The chip enable that becomes active depends on the address.
# ARDY is synchronized internally. If the setup time shown is not met, ARDY will be recognized on the next clock cycle.

Figure 5−4. Asynchronous Memory Read Timing



† Setup, Strobe, Hold, and Extended Hold are programmable in the EMIF. The programmable Hold period is not associated with the activity of the HOLD and HOLDA signals.
‡ The extended hold time is programmable in the EMIF and is only present when consecutive memory accesses are made to different CEx spaces, or are of different types (read/write).
§ All timings referenced to CLKOUT assume CLKOUT is the same frequency as the internal CPU clock (divide-by-1 mode).
¶ The chip enable that becomes active depends on the address.
# ARDY is synchronized internally. If the setup time shown is not met, ARDY will be recognized on the next clock cycle.

Figure 5−5. Asynchronous Memory Write Timing

5.7.2 Synchronous-Burst SRAM (SBSRAM) Timing

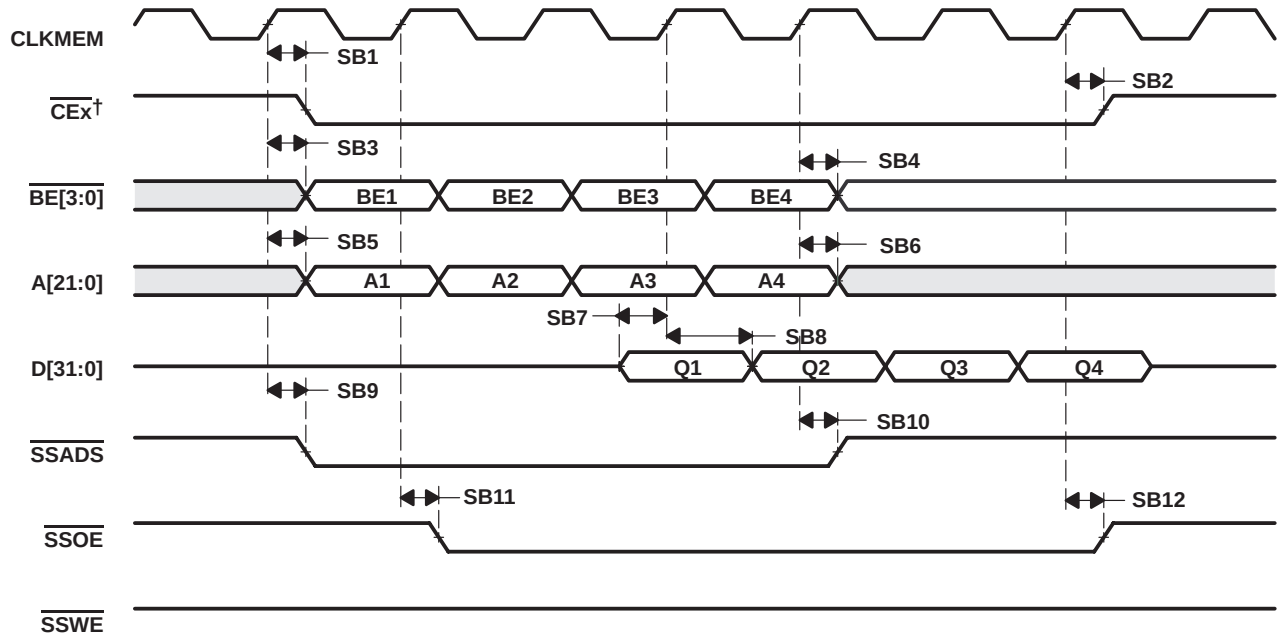
Table 5−7 and Table 5−8 assume testing over recommended operating conditions (see Figure 5−6 and Figure 5−7).

Table 5−7. Synchronous-Burst SRAM Cycle Timing Requirements

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
SB7	$t_{su(DV-CLKMEMH)}$	Setup time, read data valid before CLKMEM high	5		ns
SB8	$t_{h(CLKMEMH-DV)}$	Hold time, read data valid after CLKMEM high	2		ns

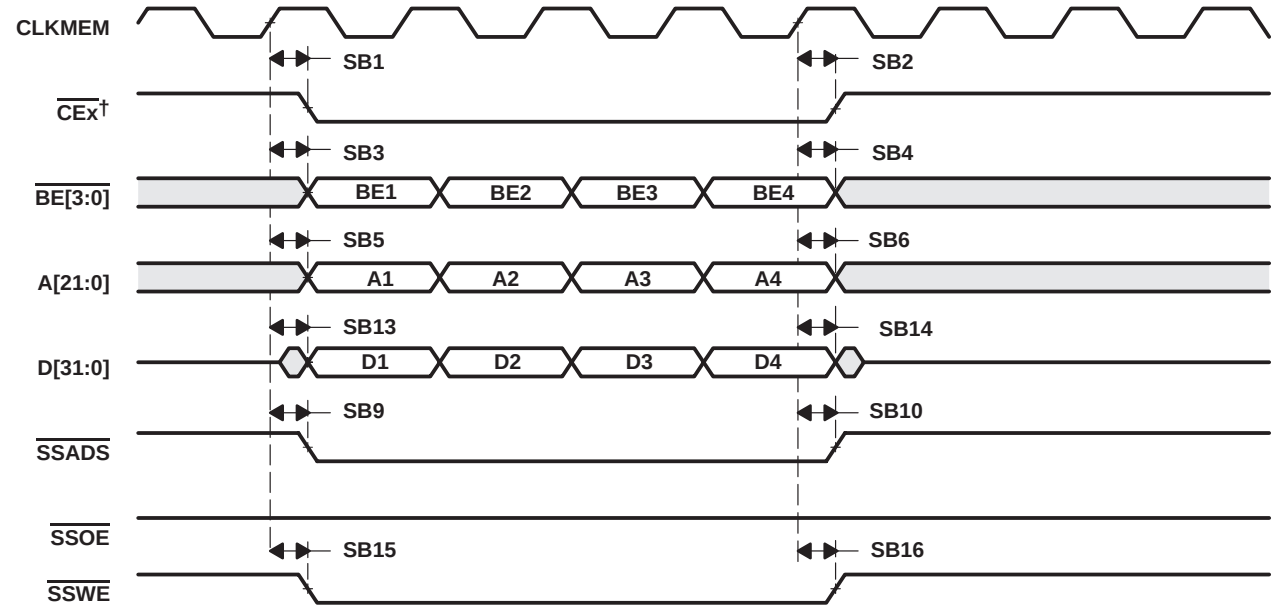
Table 5−8. Synchronous-Burst SRAM Cycle Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
SB1	$t_{d(CLKMEMH-CEL)}$	Delay time, CLKMEM high to $\overline{CEx}$ low	3	6	ns
SB2	$t_{d(CLKMEMH-CEH)}$	Delay time, CLKMEM high to $\overline{CEx}$ high	3	6	ns
SB3	$t_{d(CLKMEMH-BEV)}$	Delay time, CLKMEM high to $\overline{BEx}$ valid	3	6	ns
SB4	$t_{d(CLKMEMH-BEIV)}$	Delay time, CLKMEM high to $\overline{BEx}$ invalid	3	6	ns
SB5	$t_{d(CLKMEMH-AV)}$	Delay time, CLKMEM high to address valid	3	6	ns
SB6	$t_{d(CLKMEMH-AIV)}$	Delay time, CLKMEM high to address invalid	3	6	ns
SB9	$t_{d(CLKMEMH-ADSL)}$	Delay time, CLKMEM high to $\overline{SSADS}$ low	3	6	ns
SB10	$t_{d(CLKMEMH-ADSH)}$	Delay time, CLKMEM high to $\overline{SSADS}$ high	3	6	ns
SB11	$t_{d(CLKMEMH-OEL)}$	Delay time, CLKMEM high to $\overline{SSOE}$ low	3	6	ns
SB12	$t_{d(CLKMEMH-OEH)}$	Delay time, CLKMEM high to $\overline{SSOE}$ high	3	6	ns
SB13	$t_{d(CLKMEMH-DV)}$	Delay time, CLKMEM high to data valid	3	6	ns
SB14	$t_{d(CLKMEMH-DIV)}$	Delay time, CLKMEM high to data invalid	3	6	ns
SB15	$t_{d(CLKMEMH-WEL)}$	Delay time, CLKMEM high to $\overline{SSWE}$ low	3	6	ns
SB16	$t_{d(CLKMEMH-WEH)}$	Delay time, CLKMEM high to $\overline{SSWE}$ high	3	6	ns



† The chip enable that becomes active depends on the address.

Figure 5−6. SBSRAM Read Timing



† The chip enable that becomes active depends on the address.

Figure 5−7. SBSRAM Write Timing

5.7.3 Synchronous DRAM (SDRAM) Timing

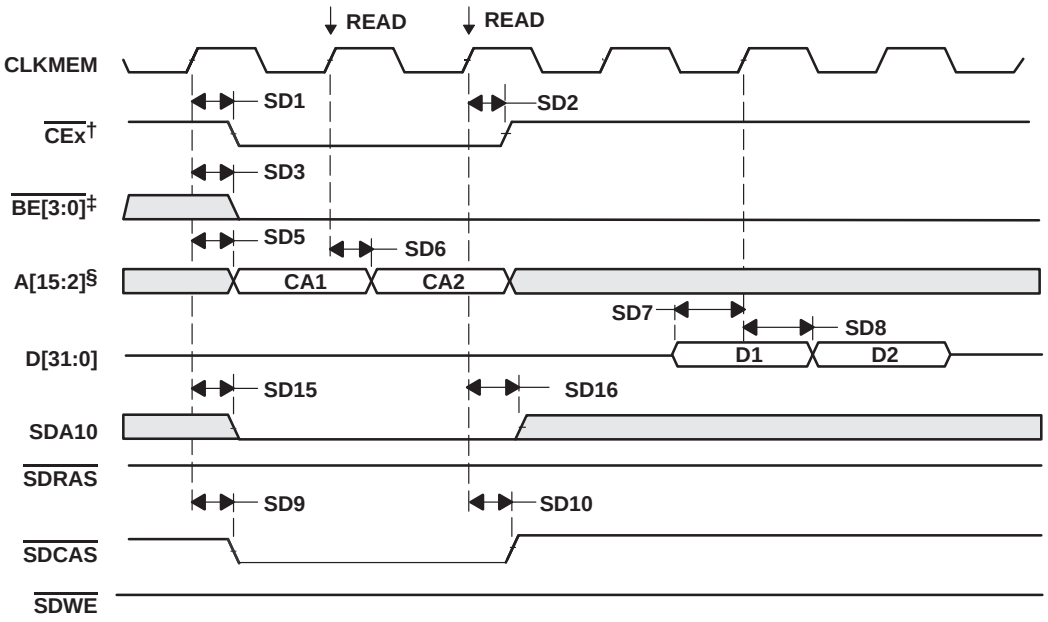
Table 5−9 and Table 5−10 assume testing over recommended operating conditions (see Figure 5−8 through Figure 5−13).

Table 5−9. Synchronous DRAM Cycle Timing Requirements

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
SD7	$t_{su(DV-CLKMEMH)}$	Setup time, read data valid before CLKMEM high	5		ns
SD8	$t_{h(CLKMEMH-DV)}$	Hold time, read data valid after CLKMEM high	2		ns

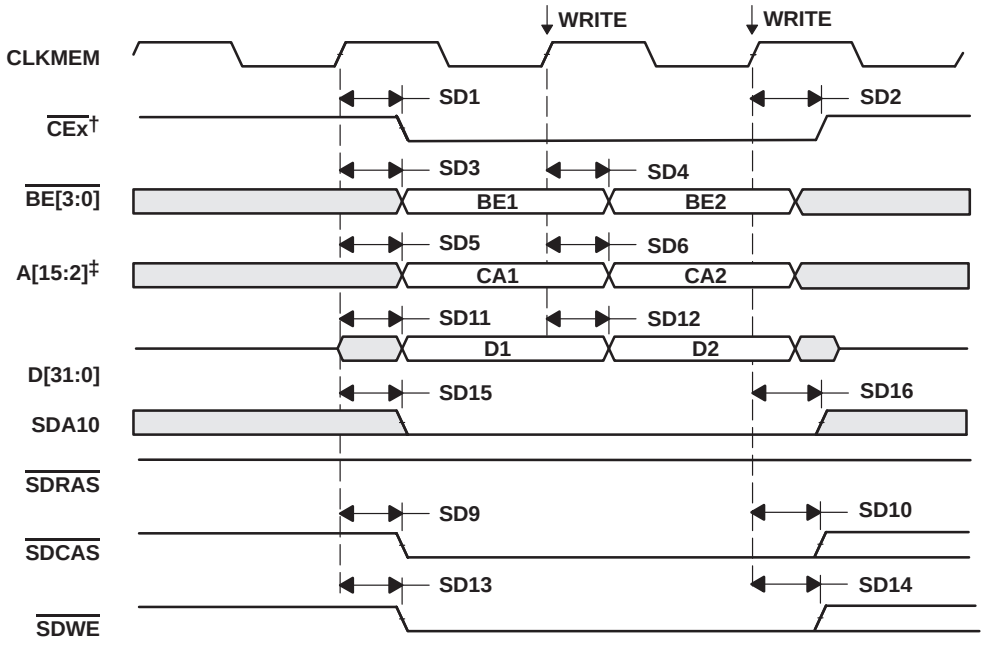
Table 5−10. Synchronous DRAM Cycle Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
SD1	$t_{d(CLKMEMH-CEL)}$	Delay time, CLKMEM high to $\overline{CEx}$ low	3	6	ns
SD2	$t_{d(CLKMEMH-CEH)}$	Delay time, CLKMEM high to $\overline{CEx}$ high	3	6	ns
SD3	$t_{d(CLKMEMH-BEV)}$	Delay time, CLKMEM high to $\overline{BEx}$ valid	3	6	ns
SD4	$t_{d(CLKMEMH-BEIV)}$	Delay time, CLKMEM high to $\overline{BEx}$ invalid	3	6	ns
SD5	$t_{d(CLKMEMH-AV)}$	Delay time, CLKMEM high to address valid	3	6	ns
SD6	$t_{d(CLKMEMH-AIV)}$	Delay time, CLKMEM high to address invalid	3	6	ns
SD9	$t_{d(CLKMEMH-SDCASL)}$	Delay time, CLKMEM high to $\overline{SDCAS}$ low	3	5	ns
SD10	$t_{d(CLKMEMH-SDCASH)}$	Delay time, CLKMEM high to $\overline{SDCAS}$ high	3	5	ns
SD11	$t_{d(CLKMEMH-DV)}$	Delay time, CLKMEM high to data valid	3	5	ns
SD12	$t_{d(CLKMEMH-DIV)}$	Delay time, CLKMEM high to data invalid	3	5	ns
SD13	$t_{d(CLKMEMH-SDWEL)}$	Delay time, CLKMEM high to $\overline{SDWE}$ low	3	5	ns
SD14	$t_{d(CLKMEMH-SDWEH)}$	Delay time, CLKMEM high to $\overline{SDWE}$ high	3	5	ns
SD15	$t_{d(CLKMEMH-SDA10V)}$	Delay time, CLKMEM high to SDA10 valid	3	5	ns
SD16	$t_{d(CLKMEMH-SDA10IV)}$	Delay time, CLKMEM high to SDA10 invalid	3	5	ns
SD17	$t_{d(CLKMEMH-SDRASL)}$	Delay time, CLKMEM high to $\overline{SDRAS}$ low	3	5	ns
SD18	$t_{d(CLKMEMH-SDRASH)}$	Delay time, CLKMEM high to $\overline{SDRAS}$ high	3	5	ns



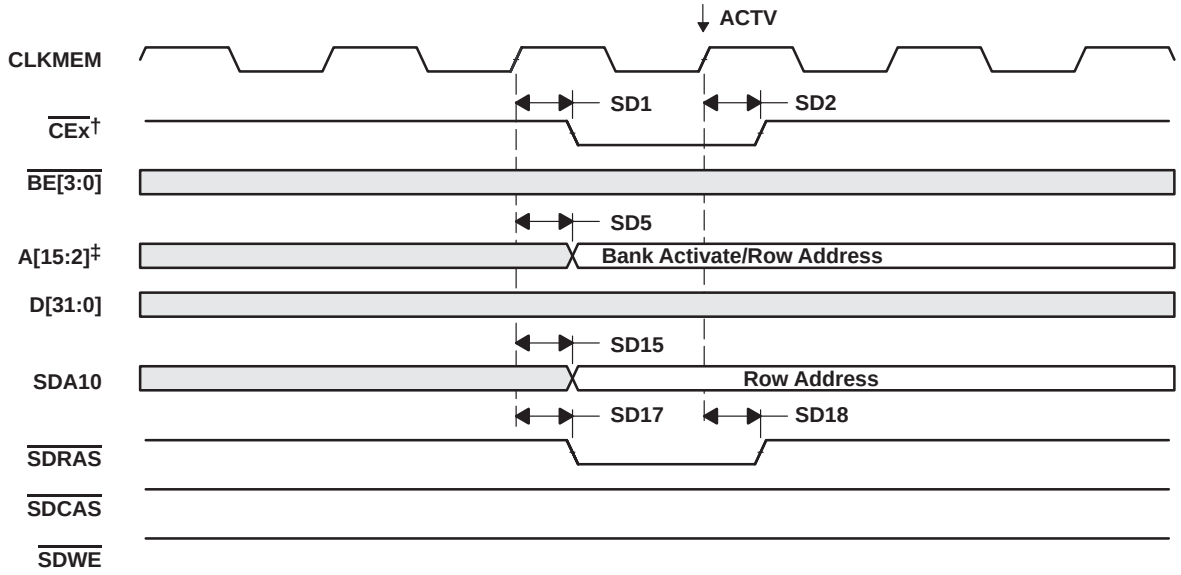
† The chip enable that becomes active depends on the address.
‡ All BE[3:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.
§ The number of address signals used depends on the SDRAM size and width.

Figure 5−8. Two SDRAM Read Commands (Active Row)



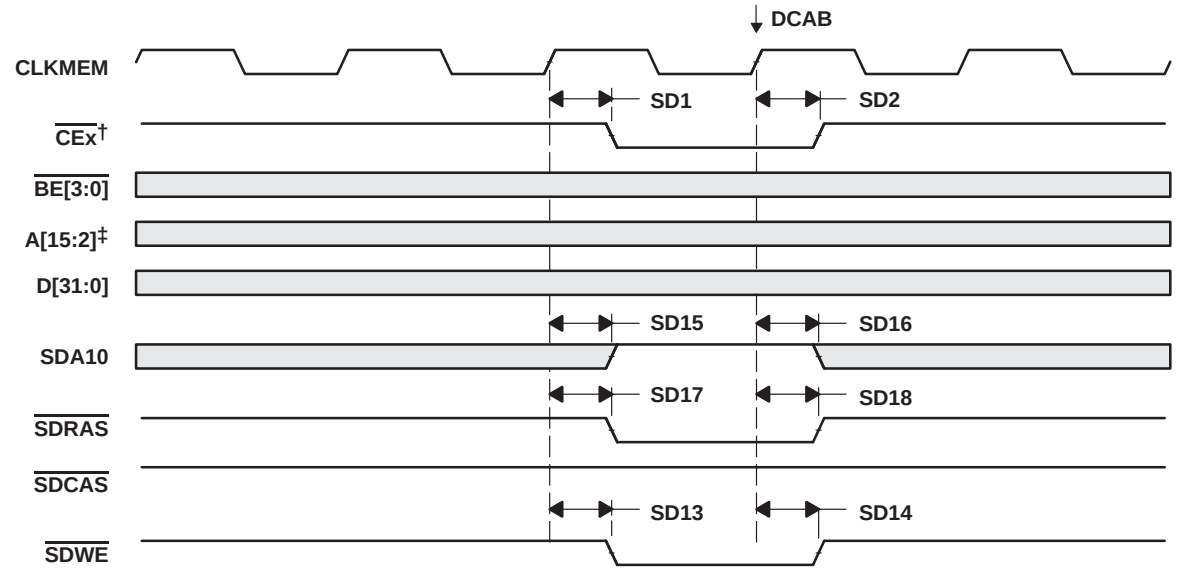
† The chip enable that becomes active depends on the address.
‡ The number of address signals used depends on the SDRAM size and width.

Figure 5−9. Two SDRAM WRT Commands (Active Row)



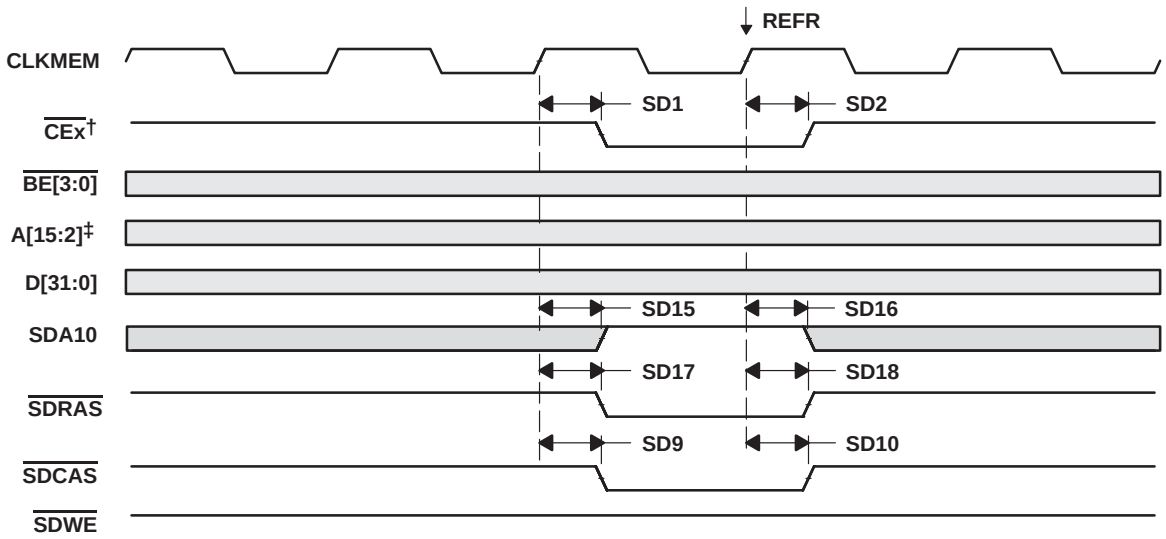
† The chip enable that becomes active depends on the address.
‡ The number of address signals used depends on the SDRAM size and width.

Figure 5−10. SDRAM ACTV Command



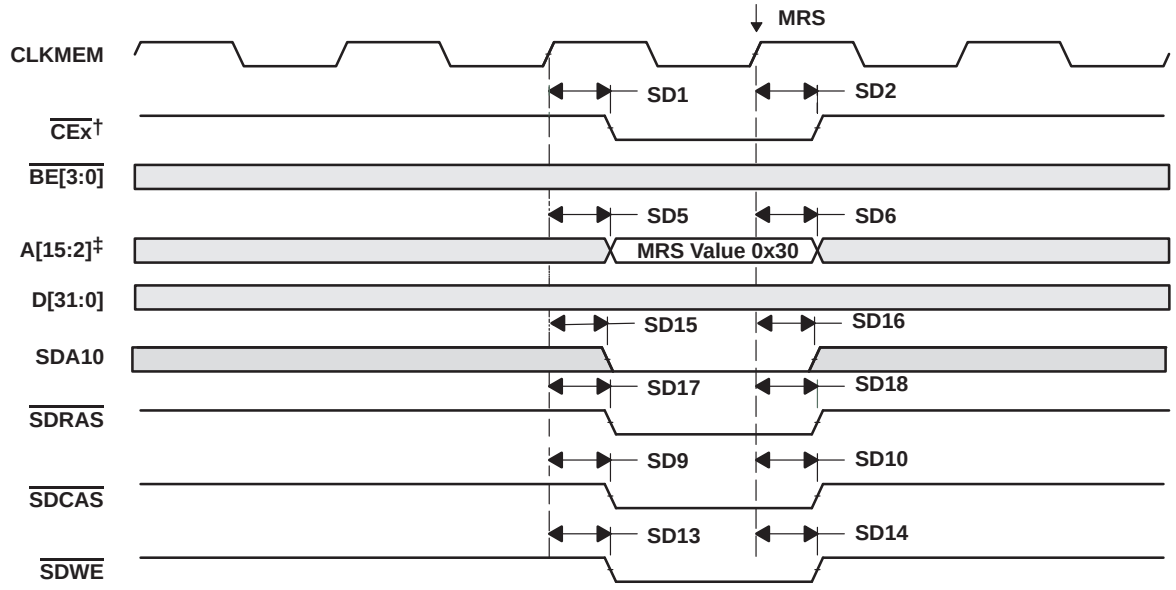
† The chip enable that becomes active depends on the address.
‡ The number of address signals used depends on the SDRAM size and width.

Figure 5−11. SDRAM DCAB Command



† The chip enable that becomes active depends on the address.
‡ The number of address signals used depends on the SDRAM size and width.

Figure 5−12. SDRAM REFR Command



† The chip enable that becomes active depends on the address.
‡ The number of address signals used depends on the SDRAM size and width.

Figure 5−13. SDRAM MRS Command

5.8 $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings

Table 5−11 and Table 5−12 assume testing over recommended operating conditions (see Figure 5−14).

Table 5−11. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing Requirements

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
H1	$t_{su(HOLDH-COH)}$	Setup time, $\overline{\text{HOLD}}$ high before CLKOUT high†	7		ns

† $\overline{\text{HOLD}}$ is synchronized internally. If the setup time shown is not met, $\overline{\text{HOLD}}$ will be recognized on the next clock cycle.

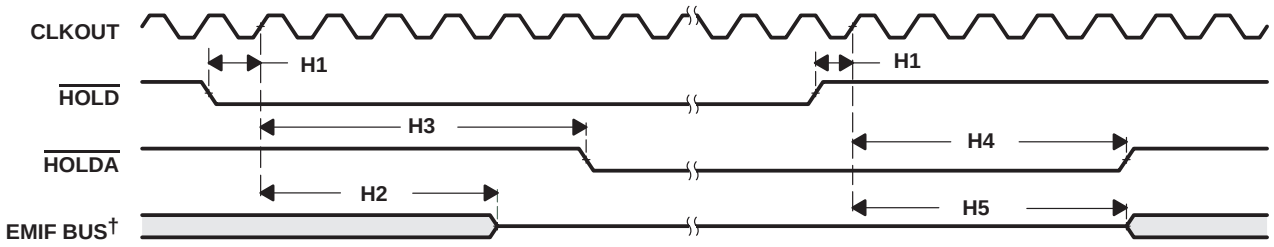
Table 5−12. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Switching Characteristics‡

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
H2	$t_{R(COH-BHZ)}$	Response time, CLKOUT high to EMIF Bus high impedance (HZ)¶	4P	§	ns
H3	$t_{R(COH-HOLDAL)}$	Response time, CLKOUT high to $\overline{\text{HOLDA}}$ low	5P−1		ns
H4	$t_{R(COH-HOLDAH)}$	Response time, CLKOUT high to $\overline{\text{HOLDA}}$ high	4P−1	4P+5	ns
H5	$t_{R(COH-BLZ)}$	Response time, CLKOUT high to EMIF Bus low impedance (LZ) (active)¶	4P−1	4P+5	ns

‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

§ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.

¶ EMIF Bus consists of $\overline{\text{CE}}$[3:0], $\overline{\text{BE}}$[3:0], D[31:0], A[21:0], $\overline{\text{ARE}}$, $\overline{\text{AOE}}$, $\overline{\text{AWE}}$, $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, $\overline{\text{SSWE}}$, CLKMEM, SDA10, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, and $\overline{\text{SDWE}}$.



† EMIF Bus consists of $\overline{\text{CE}}$[3:0], $\overline{\text{BE}}$[3:0], D[31:0], A[21:0], $\overline{\text{ARE}}$, $\overline{\text{AOE}}$, $\overline{\text{AWE}}$, $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, $\overline{\text{SSWE}}$, SDA10, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and CLKMEM.

Figure 5−14. $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ Timing

5.9 Reset Timings

Table 5−13 and Table 5−14 assume testing over recommended operating conditions (see Figure 5−15).

Table 5−13. Reset Timing Requirements†

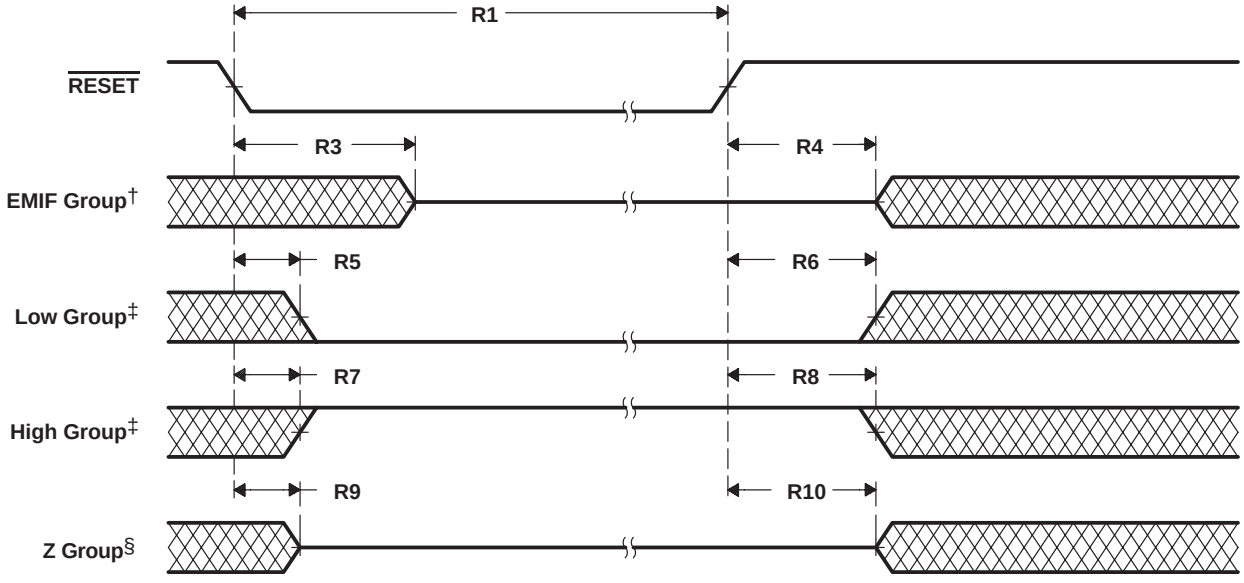
NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
R1	$t_{w(RSL)}$	Pulse width, reset low	2P + 5		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−14. Reset Switching Characteristics†

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
R3	$t_{d(RSL-EMIFHZ)}$	Delay time, reset low to EMIF group high impedance‡		19	ns
R4	$t_{d(RSL-EMIFV)}$	Delay time, reset low to EMIF group valid‡		38P + 19	ns
R5	$t_{d(RSL-LOWIV)}$	Delay time, reset low to low group invalid§		17	ns
R6	$t_{d(RSL-LOWV)}$	Delay time, reset low to low group valid§		38P + 17	ns
R7	$t_{d(RSL-HIGHIV)}$	Delay time, reset low to high group invalid§		9	ns
R8	$t_{d(RSL-HIGHV)}$	Delay time, reset low to high group valid§		38P + 9	ns
R9	$t_{d(RSL-ZHZ)}$	Delay time, reset low to Z group high impedance¶		18	ns
R10	$t_{d(RSL-ZV)}$	Delay time, reset low to Z group valid¶		39P + 18	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ EMIF group: $\overline{CE[0:3]}$, $\overline{BE[0:3]}$, CLKMEM, $\overline{ARE}$, $\overline{AOE}$, $\overline{AWE}$, $\overline{SSADS}$, $\overline{SSOE}$, $\overline{SSWE}$, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, and SDA10
§ High group: $\overline{HINT}$
Low group: $\overline{HOLDA}$
¶ Z group: A[21:0], D[31:0], CLKR[2:0], CLKX[2:0], FSR[2:0], FSX[2:0], DX[2:0], IO[7:0], XF, and TIN/TOUT[1:0]



† EMIF group: $\overline{CE[0:3]}$, $\overline{BE[0:3]}$, CLKMEM, $\overline{ARE}$, $\overline{AOE}$, $\overline{AWE}$, $\overline{SSADS}$, $\overline{SSOE}$, $\overline{SSWE}$, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, and SDA10
‡ High group: $\overline{HINT}$
Low group: $\overline{HOLDA}$
§ Z group: A[21:0], D[31:0], CLKR[2:0], CLKX[2:0], FSR[2:0], FSX[2:0], DX[2:0], IO[7:0], XF, and TIN/TOUT[1:0]

Figure 5−15. Reset Timing

5.10 External Interrupt Timings

Table 5−15 assumes testing over recommended operating conditions (see Figure 5−16).

Table 5−15. External Interrupt Timing Requirements†

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
I1	$t_{w(INTH)A}$	Pulse width, interrupt high, CPU active	2P		ns
I2	$t_{w(INTL)A}$	Pulse width, interrupt low, CPU active	3P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

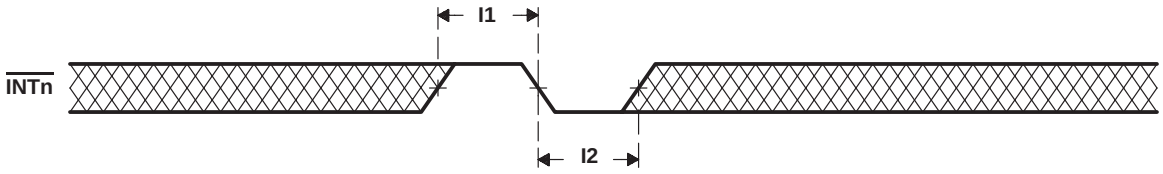


Figure 5−16. External Interrupt Timings

5.11 XF Timings

Table 5−16 assumes testing over recommended operating conditions (see Figure 5−17).

Table 5−16. XF Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
X1	$t_{d(XF)}$	Delay time, CLKOUT high to XF high	0	4	ns
		Delay time, CLKOUT high to XF low	0	4	

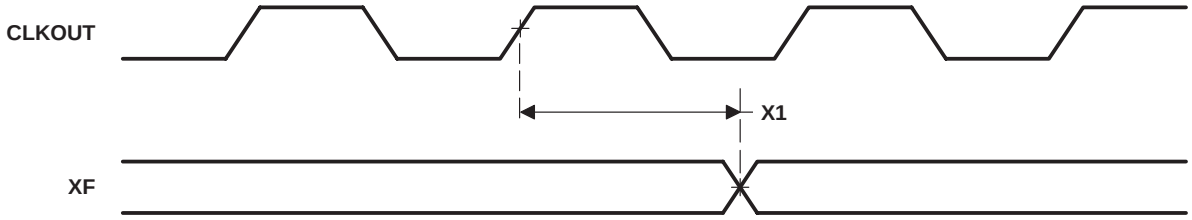


Figure 5−17. XF Timing

5.12 General-Purpose Input/Output (IOx) Timings

Table 5−17 and Table 5−18 assume testing over recommended operating conditions (see Figure 5−18).

Table 5−17. General-Purpose Input/Output (GPIO) Pins Configured as Inputs Timing Requirements

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
G2	$t_{su(GPIO-COH)}$	Setup time, IOx input valid before CLKOUT high	8		ns
G3	$t_{h(COH-GPIO)}$	Hold time, IOx input valid after CLKOUT high	0		ns

Table 5−18. General-Purpose Input/Output (GPIO) Pins Configured as Inputs Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
G1	$t_{d(COH-GPIO)}$	Delay time, CLKOUT high to IOx output change	0	6	ns

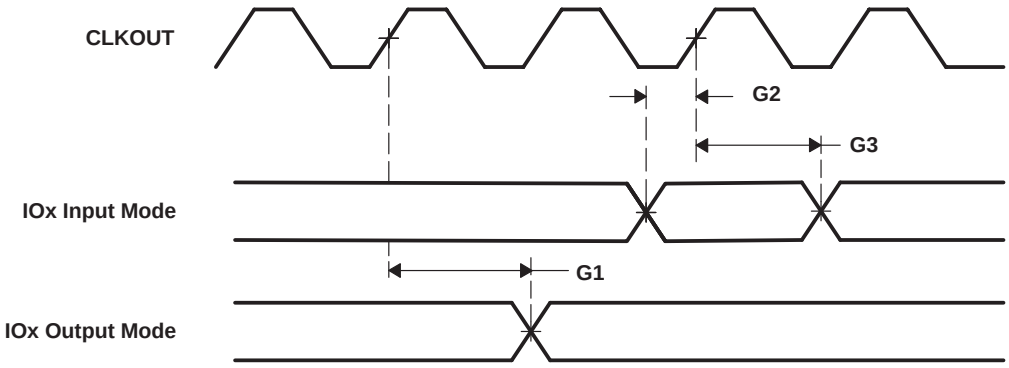


Figure 5−18. General-Purpose Input/Output (IOx) Signal Timings

5.13 TIN/TOUT Timings

Table 5−19 and Table 5−20 assume testing over recommended operating conditions (see Figure 5−19 and Figure 5−20).

Table 5−19. TIN/TOUT Pins Configured as Inputs Timing Requirements†

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
T4	$t_{w(TIN/TOUTL)}$	Pulse width, TIN/TOUT low	2P + 1		ns
T5	$t_{w(TIN/TOUTH)}$	Pulse width, TIN/TOUT high	2P + 1		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−20. TIN/TOUT Pins Configured as Outputs Switching Characteristics†‡

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
T1	$t_{d(COH-TIN/TOUTH)}$	Delay time, CLKOUT high to TIN/TOUT high	0	2	ns
T2	$t_{d(COH-TIN/TOUTL)}$	Delay time, CLKOUT high to TIN/TOUT low	0	2	ns
T3	$t_{w(TIN/TOUT)}$	Pulse duration, TIN/TOUT (output)	P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ For proper operation of the TIN/TOUT pin configured as an output, the timer period must be configured for at least 4 cycles.

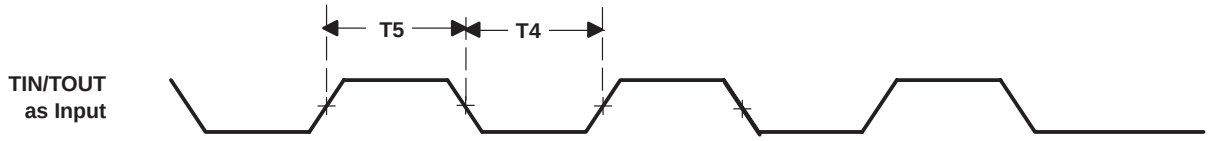


Figure 5−19. TIN/TOUT Timing When Configured as Inputs

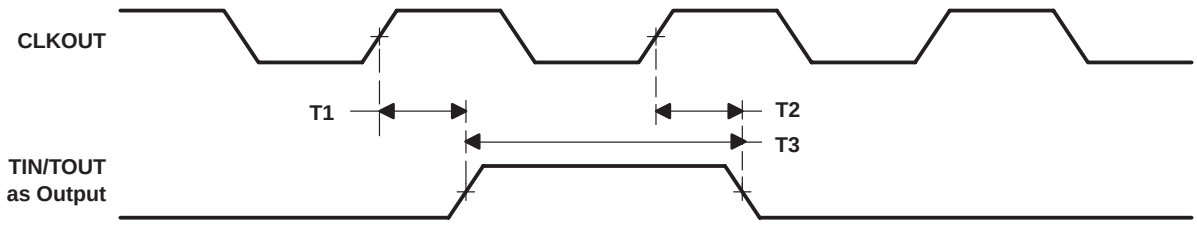


Figure 5−20. TIN/TOUT Timing When Configured as Outputs

5.14 Multichannel Buffered Serial Port (McBSP) Timings

5.14.1 McBSP Transmit and Receive Timings

Table 5−21 and Table 5−22 assume testing over recommended operating conditions (see Figure 5−21 and Figure 5−22).

Table 5−21. McBSP Timing Requirements†‡

NO.				VC5510/5510A-160 VC5510/5510A-200		UNIT
				MIN	MAX	
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P−1		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		5	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		5	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	5		ns
			CLKR ext	1		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	2		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	4		ns
			CLKR ext	1		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	2		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	5		ns
			CLKX ext	1		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	2		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−22. McBSP Switching Characteristics†‡

NO.	PARAMETER				VC5510/5510A-160 VC5510/5510A-200		UNIT
					MIN	MAX	
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D−1§	D+1§	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C−1§	C+1§	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	−2	2	ns
				CLKR ext	3	7	ns
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	−2	2	ns
				CLKX ext	3	7	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int	0	2	ns
				CLKX ext	1	11	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int		6	ns
				CLKX ext		9	
		Delay time, CLKX high to DX valid¶	DXENA = 0	CLKX int		6	
				CLKX ext		9	
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int		2P+6	
				CLKX ext		2P+9	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven¶	DXENA = 0	CLKX int	0		ns
				CLKX ext	6		
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P		
				CLKX ext	P+6		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid¶	DXENA = 0	FSX int		5	ns
				FSX ext		9	
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 1	FSX int		2P+5	
				FSX ext		2P+9	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven¶	DXENA = 0	FSX int	0		ns
				FSX ext	6		
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 1	FSX int	P		
				FSX ext	P+6		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

§ T=CLKRX period = (1 + CLKGDV) * P
C=CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D=CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even

¶ See the *TMS320VC5501/5502/5503/5507/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide* (literature number SPRU592) for a description of the DX enable (DXENA) and data delay features of the McBSP.

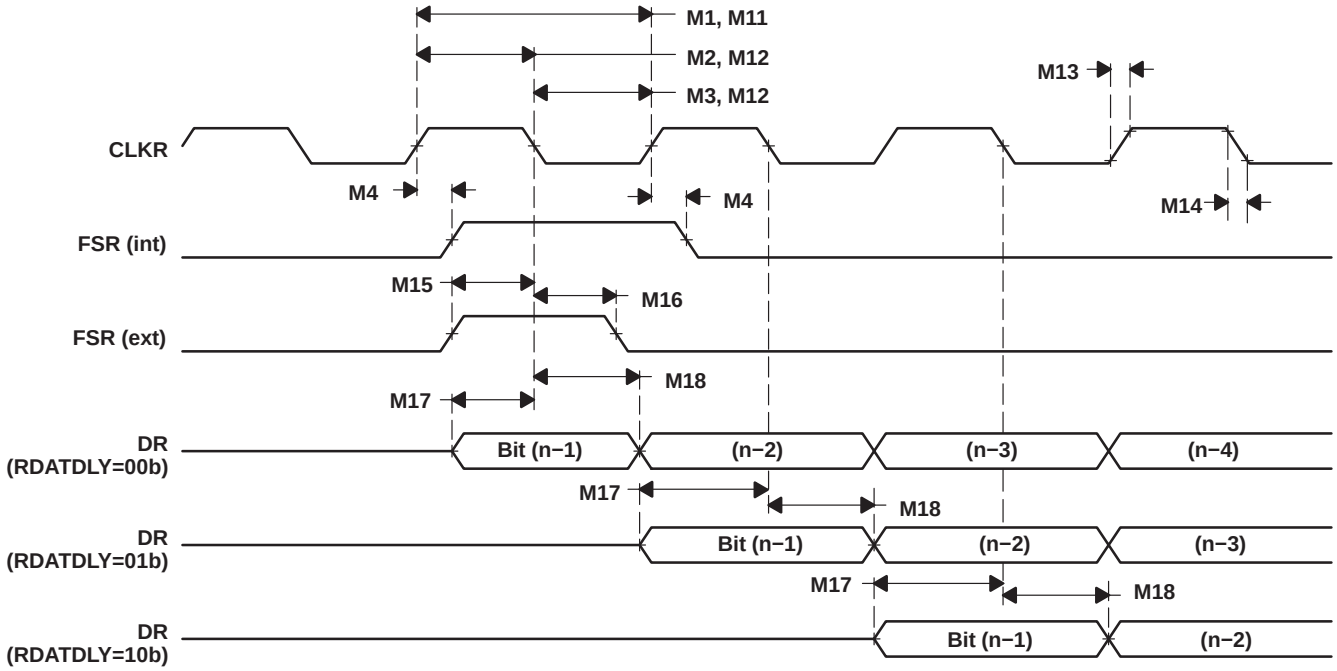


Figure 5−21. McBSP Receive Timings

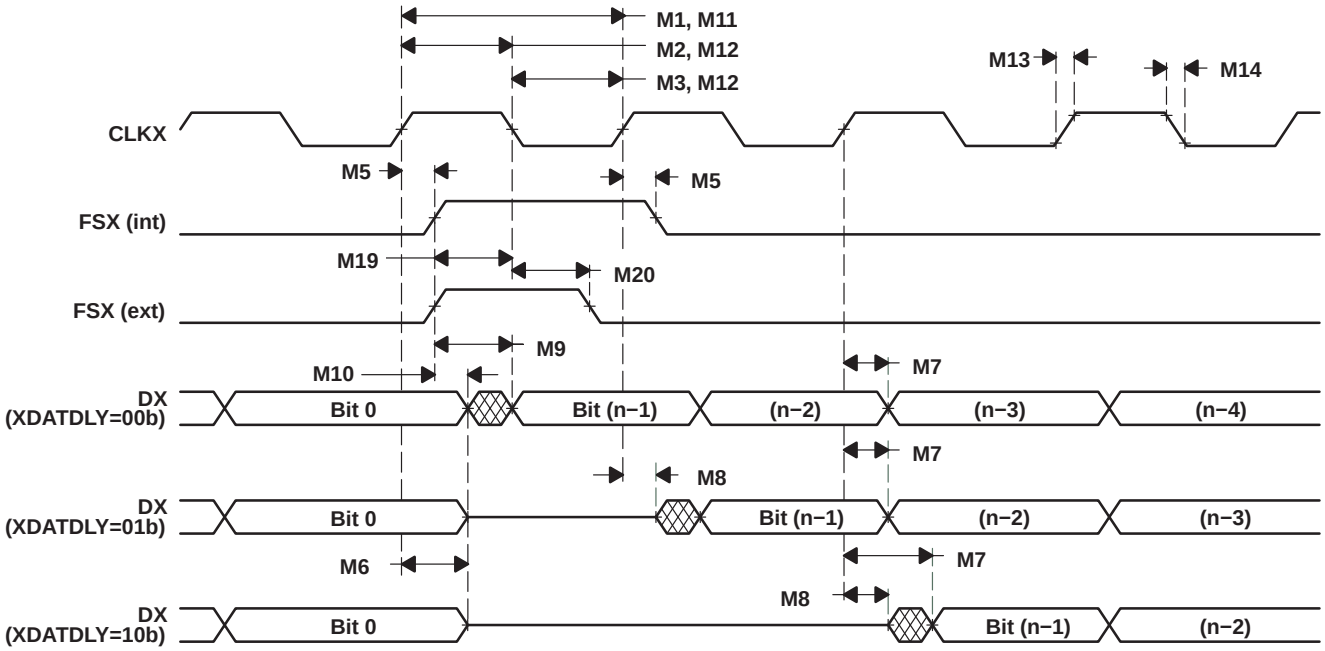


Figure 5−22. McBSP Transmit Timings

5.14.2 McBSP General-Purpose I/O Timing

Table 5−23 and Table 5−24 assume testing over recommended operating conditions (see Figure 5−23).

Table 5−23. McBSP General-Purpose I/O Timing Requirements

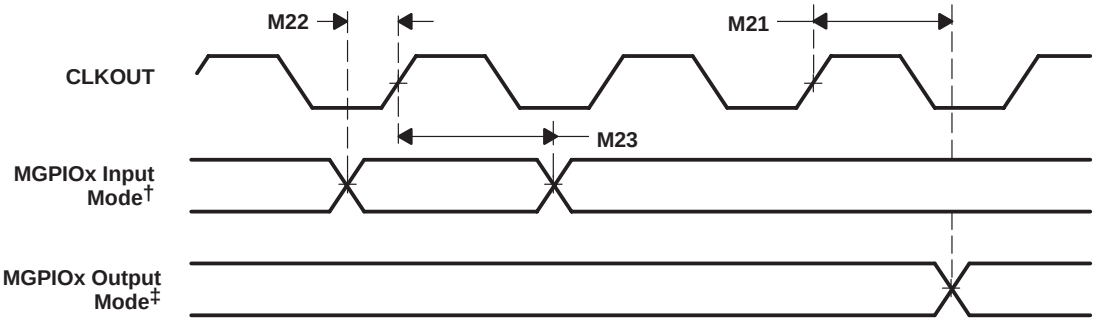
NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
M22	$t_{su(MGPIO-COH)}$	Setup time, MGPIOx input mode before CLKOUT high†	7		ns
M23	$t_{h(COH-MGPIO)}$	Hold time, MGPIOx input mode after CLKOUT high†	0		ns

† MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general-purpose input.

Table 5−24. McBSP General-Purpose I/O Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
M21	$t_{d(COH-MGPIO)}$	Delay time, CLKOUT high to MGPIOx output mode‡	0	3	ns

‡ MGPIOx refers to CLKRx, FSRx, CLKXx, FSXx, or DXx when configured as a general-purpose output.



† MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general-purpose input.
‡ MGPIOx refers to CLKRx, FSRx, CLKXx, FSXx, or DXx when configured as a general-purpose output.

Figure 5−23. McBSP General-Purpose I/O Timings

5.14.3 McBSP as SPI Master or Slave Timing

Table 5−25 to Table 5−32 assume testing over recommended operating conditions (see Figure 5−24 through Figure 5−27).

Table 5−25. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†‡

NO.			VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	4		3 − 6P		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		1 + 6P		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high			10		ns
M33	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−26. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†‡

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
M24	$t_{d(CKXL-FXL)}$	Delay time, FSX low to CLKX low¶	T − 1	T + 3			ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	C − 2	C + 2			ns
M26	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−2	4	3P + 2	5P+ 8	ns
M27	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	C − 2	C			ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			3P + 8	3P + 20	ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			3P − 3	3P + 20	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

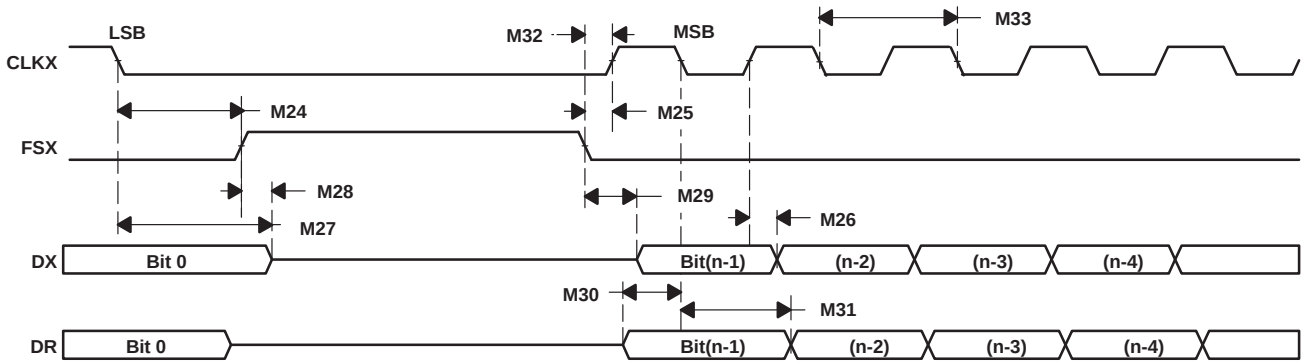


Figure 5−24. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5−27. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†‡

NO.			VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	4		3 − 6P		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		1 +6P		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high			10		ns
M42	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−28. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†‡

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
M34	$t_{d(CKXL-FXL)}$	Delay time, FSX low to CLKX low¶	C − 1	C + 3			ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	T − 2	T + 2			ns
M36	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	−2	4	3P + 2	5P + 8	ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	−2	0	3P + 8	3P + 21	ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	D − 2	D +10	3P − 3	3P + 21	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

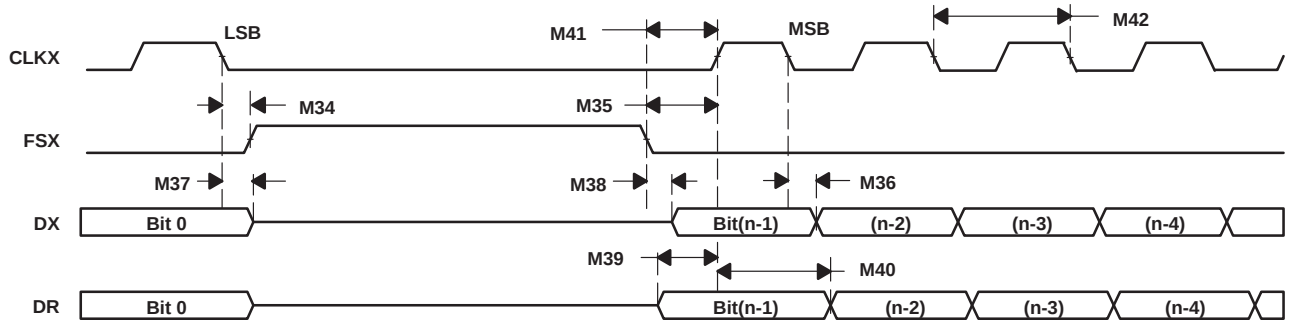


Figure 5−25. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5−29. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†‡

NO.			VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	4		3 − 6P		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		1 + 6P		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			10		ns
M52	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−30. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†‡

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
M43	$t_{d(CKXH-FXL)}$	Delay time, FSX low to CLKX high¶	T − 1	T + 3			ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	D − 2	D + 2			ns
M45	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	−2	4	3P + 2	5P + 8	ns
M46	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	D − 2	D			ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			3P + 8	3P + 20	ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			3P − 3	3P + 20	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ T = CLKX period = (1 + CLKGDV) * P
D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

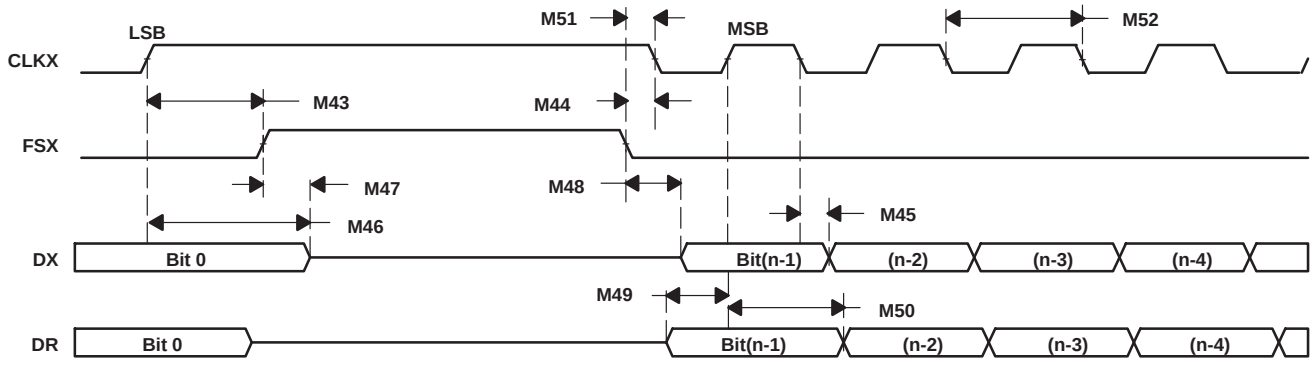


Figure 5−26. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5−31. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†‡

NO.			VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	4		3 − 6P		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		1 + 6P		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			10		ns
M61	$t_{c(CKX)}$	Cycle time, CLKX	2P		16P		ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−32. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†‡

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
M53	$t_{d(CKXH-FXL)}$	Delay time, FSX low to CLKX high¶	D − 1	D + 3			ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	T − 2	T + 2			ns
M55	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−2	4	3P + 2	5P + 8	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	−2	0	3P + 8	3P + 21	ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	C − 2	C +10	3P − 3	3P + 21	ns

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

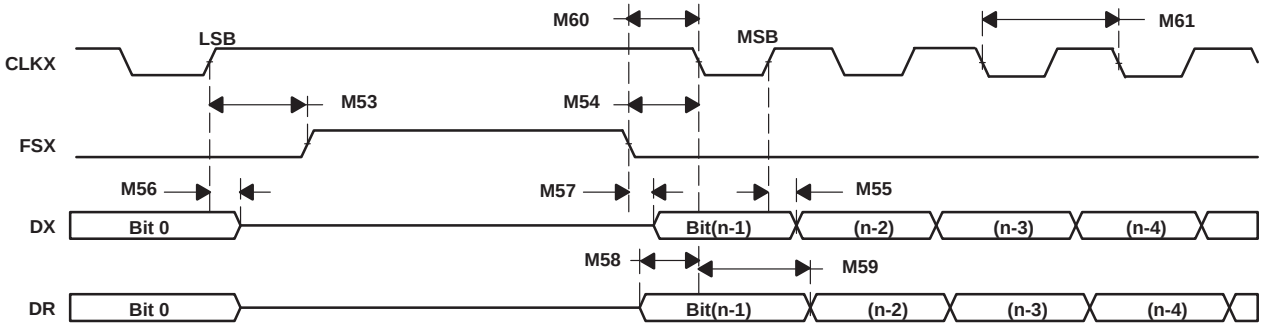


Figure 5−27. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.15 Enhanced Host-Port Interface (EHPI) Timing

Table 5−33 and Table 5−34 assume testing over recommended operating conditions (see Figure 5−28 through Figure 5−32).

Table 5−33. EHPI Timing Requirements

NO.			VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
E11	$t_{su(HASL-HDSL)}$	Setup time, $\overline{HAS}$ low before $\overline{HDS}$ low	4		ns
E12	$t_{h(HDSL-HASL)}$	Hold time, $\overline{HAS}$ low after $\overline{HDS}$ low	3		ns
E13	$t_{su(HCNTLV-HDSL)}$	Setup time, (HR/$\overline{W}$, HA[19:0], HCNTL[1:0]) valid before $\overline{HDS}$ low	4		ns
E14	$t_{h(HDSL-HCNTLIV)}$	Hold time, (HR/$\overline{W}$, HA[19:0], HCNTL[1:0]) invalid after $\overline{HDS}$ low	4		ns
E15	$t_{w(HDSL)}$	Pulse duration, $\overline{HDS}$ low	4P†		ns
E16	$t_{w(HDSH)}$	Pulse duration, $\overline{HDS}$ high	4P†		ns
E17	$t_{su(HDV-HDSH)}$	Setup time, HD bus write data valid before $\overline{HDS}$ high	5		ns
E18	$t_{h(HDSH-HDIV)}$	Hold time, HD bus write data invalid after $\overline{HDS}$ high	3		ns
E19	$t_{su(HCNTLV-HASL)}$	Setup time, (HR/$\overline{W}$, HCNTL[1:0]) valid before $\overline{HAS}$ low	5		ns
E20	$t_{h(HASL-HCNTLIV)}$	Hold time, (HR/$\overline{W}$, HCNTL[1:0]) valid after $\overline{HAS}$ low	3		ns

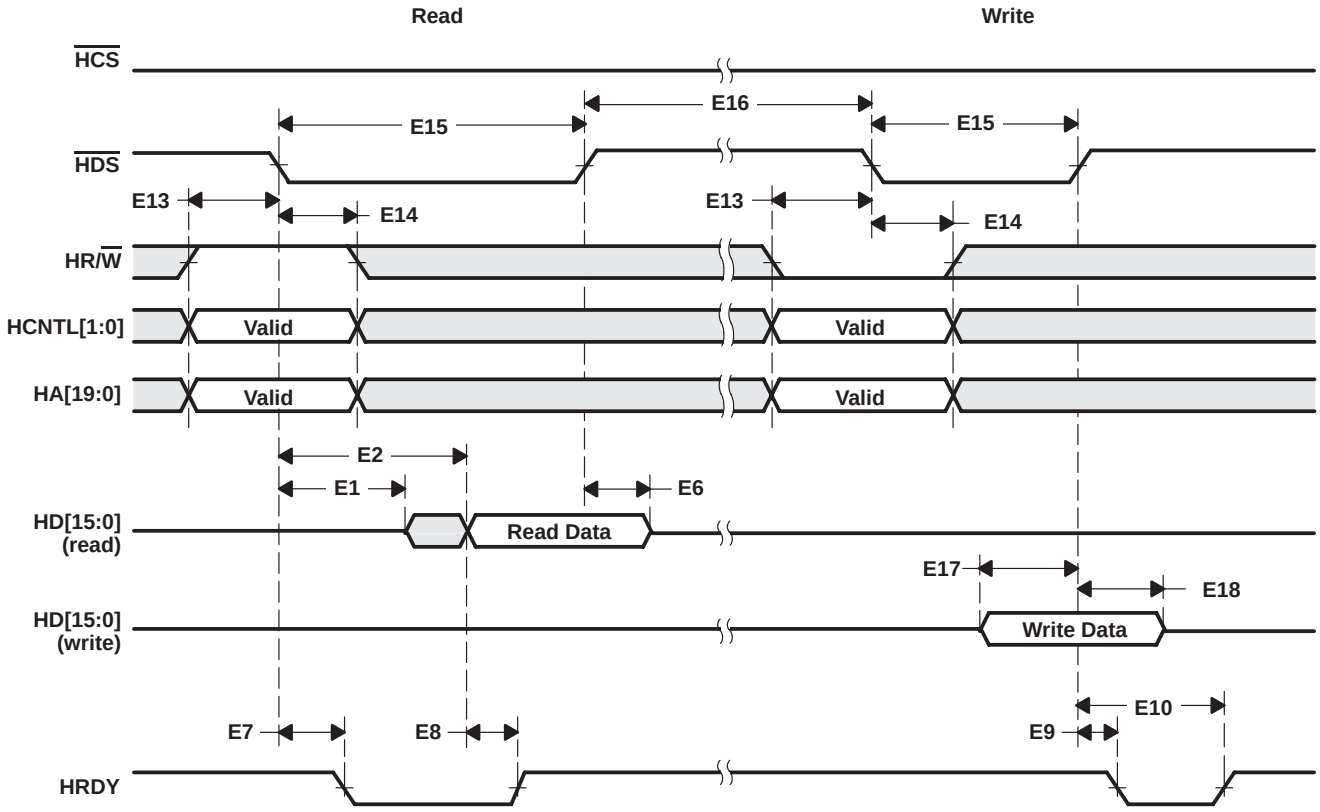
† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

Table 5−34. EHPI Switching Characteristics

NO.	PARAMETER		VC5510/5510A-160 VC5510/5510A-200		UNIT
			MIN	MAX	
E1	$t_{d(HDSL-HDD)M}$	Delay time, $\overline{HDS}$ low to HD bus read data driven (memory access)	6	16	ns
E2	$t_{d(HDSL-HDV1)M}$	Delay time, $\overline{HDS}$ low to HD bus read data valid (memory access)	14P+10†‡		ns
E4	$t_{d(HDSL-HDD)R}$	Delay time, $\overline{HDS}$ low to HD bus read data driven (register access)	6	16	ns
E5	$t_{d(HDSL-HDV)R}$	Delay time, $\overline{HDS}$ low to HD bus read data valid (register access)		16	ns
E6	$t_{dis(HDSH-HDIV)}$	Disable time, $\overline{HDS}$ high to HD bus read data invalid	6	16	ns
E7	$t_{d(HDSL-HRDYL)}$	Delay time, $\overline{HDS}$ low to HRDY low (during reads)		P+10†	ns
E8	$t_{d(HDV-HRDYH)}$	Delay time, HD bus valid to HRDY high (during reads)	2		ns
E9	$t_{d(HDSH-HRDYL)}$	Delay time, $\overline{HDS}$ high to HRDY low (during writes)		16	ns
E10	$t_{d(HDSH-HRDYH)}$	Delay time, $\overline{HDS}$ high to HRDY high (during writes)	14P+10†		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

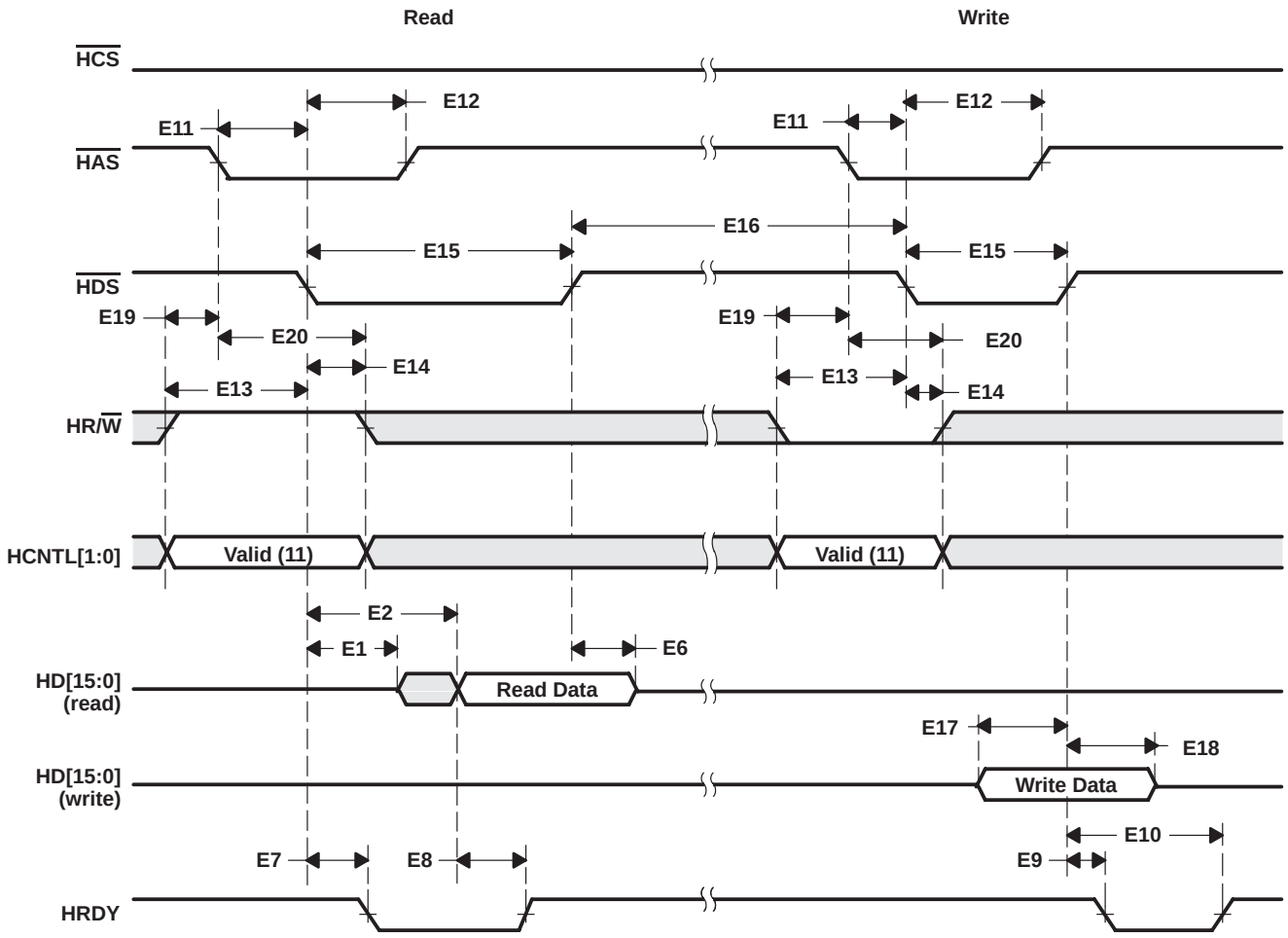
‡ EHPI latency is dependent on the number of DMA channels active, their priorities and their source/destination ports. The latency shown assumes no competing CPU or DMA activity to the memory resource being accessed by the EHPI.



NOTES: A. As of revision 2.1, the byte-enable function on the EHPI (as controlled by pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$) is no longer supported. These pins must always be driven low either by an external device, by external pulldown resistors or by using the on-chip pulldown circuitry controlled by the HPE bit in the System Register (SYSR).

B. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied low and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. Operation with $\overline{\text{HCS}}$ as a strobe is not recommended because $\overline{\text{HCS}}$ gates output of HRDY (when $\overline{\text{HCS}}$ is high HRDY is not driven).

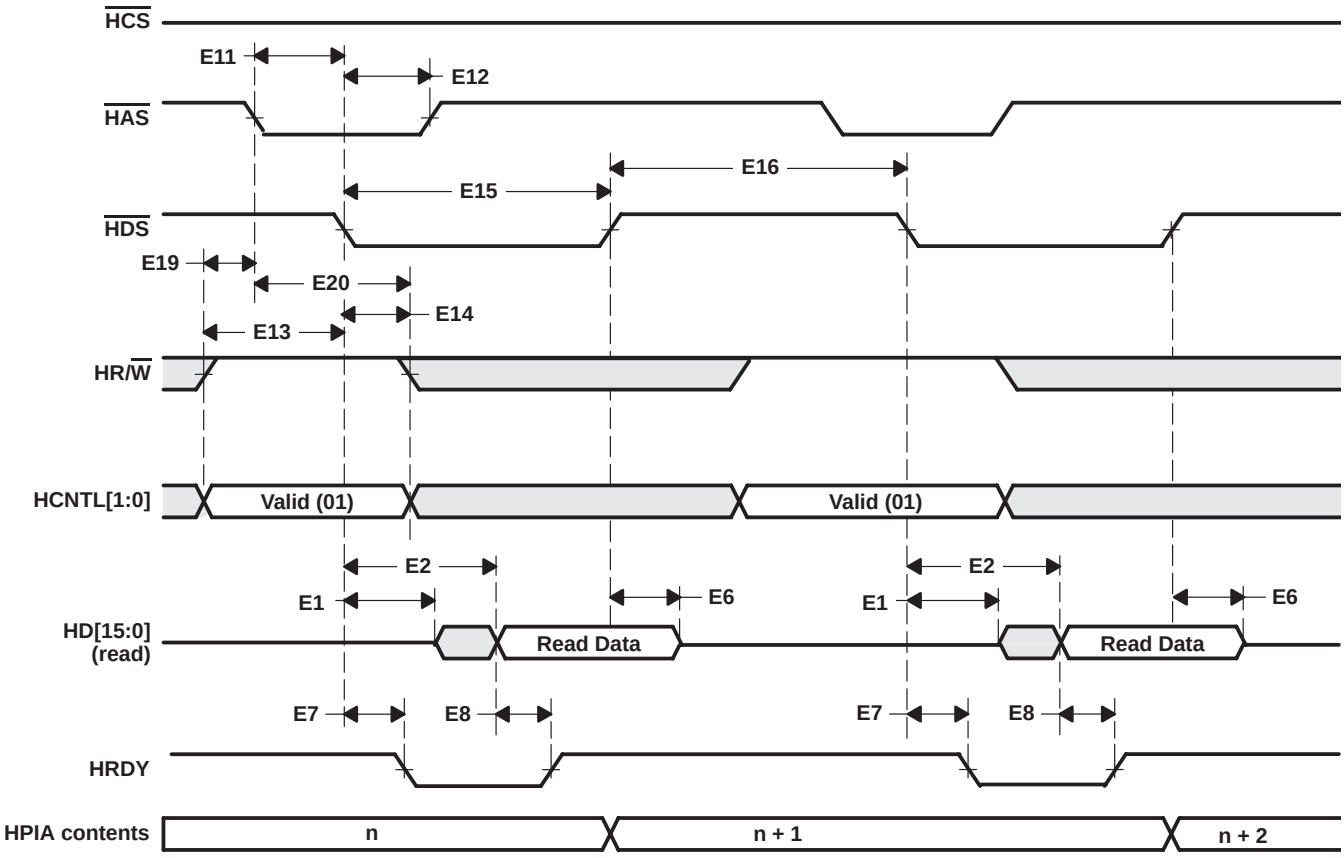
Figure 5−28. EHPI Nonmultiplexed Read/Write Timings



NOTES: A. As of revision 2.1, the byte-enable function on the EHPI (as controlled by pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$) is no longer supported. These pins must always be driven low either by an external device, by external pulldown resistors or by using the on-chip pulldown circuitry controlled by the HPE bit in the System Register (SYSR).

B. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied low and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. Operation with $\overline{\text{HCS}}$ as a strobe is not recommended because $\overline{\text{HCS}}$ gates output of HRDY (when $\overline{\text{HCS}}$ is high HRDY is not driven).

Figure 5−29. EHPI Multiplexed Memory (HPID) Access Read/Write Timings Without Autoincrement

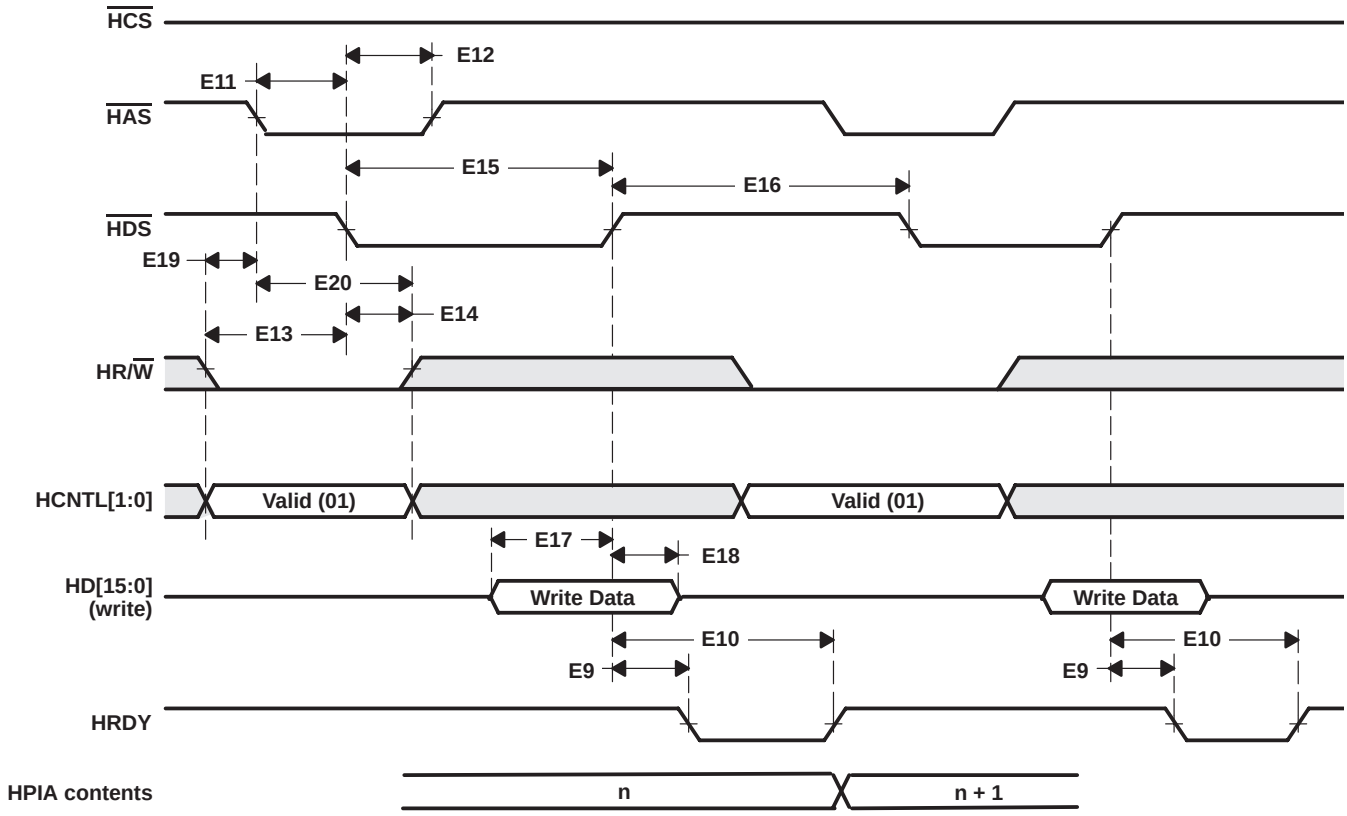


NOTES: A. As of revision 2.1, the byte-enable function on the EHPI (as controlled by pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$) is no longer supported. These pins must always be driven low either by an external device, by external pulldown resistors or by using the on-chip pulldown circuitry controlled by the HPE bit in the System Register (SYSR).

B. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.

C. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied low and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. Operation with $\overline{\text{HCS}}$ as a strobe is not recommended because $\overline{\text{HCS}}$ gates output of HRDY (when $\overline{\text{HCS}}$ is high HRDY is not driven).

Figure 5−30. EHPI Multiplexed Memory (HPID) Access Read Timings With Autoincrement

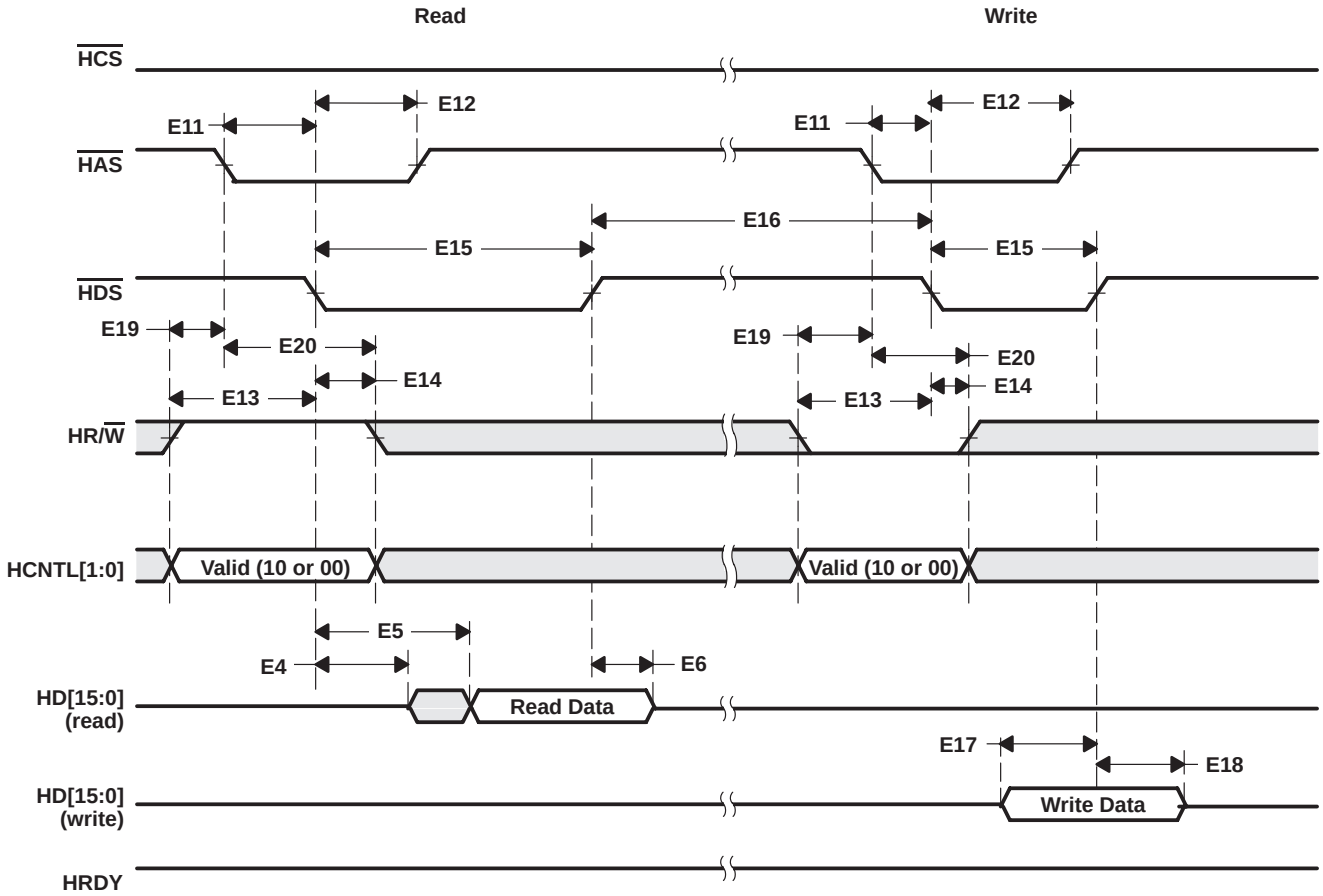


NOTES: A. As of revision 2.1, the byte-enable function on the EHPI (as controlled by pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$) is no longer supported. These pins must always be driven low either by an external device, by external pulldown resistors or by using the on-chip pulldown circuitry controlled by the HPE bit in the System Register (SYSR).

B. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.

C. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied low and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. Operation with $\overline{\text{HCS}}$ as a strobe is not recommended because $\overline{\text{HCS}}$ gates output of HRDY (when $\overline{\text{HCS}}$ is high HRDY is not driven).

Figure 5−31. EHPI Multiplexed Memory (HPID) Access Write Timings With Autoincrement



NOTES: A. As of revision 2.1, the byte-enable function on the EHPI (as controlled by pins $\overline{\text{HBE0}}$ and $\overline{\text{HBE1}}$) is no longer supported. These pins must always be driven low either by an external device, by external pulldown resistors or by using the on-chip pulldown circuitry controlled by the HPE bit in the System Register (SYSR).

B. During auto-increment mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.

C. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied low and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. Operation with $\overline{\text{HCS}}$ as a strobe is not recommended because $\overline{\text{HCS}}$ gates output of HRDY (when $\overline{\text{HCS}}$ is high HRDY is not driven).

Figure 5−32. EHPI Multiplexed Register Access Read/Write Timings

6 Mechanical Data

6.1 Package Thermal Resistance Characteristics

Table 6−1 and Table 6−2 provide the thermal resistance characteristics for the recommended package types used on the TMS320VC5510/5510A DSPs.

Table 6−1. Thermal Resistance Characteristics (Ambient)

$R_{\Theta JA}$ (°C/W)	BOARD TYPE†	AIRFLOW (LFM)
26	High-K	0
22	High-K	150
20	High-K	250
50	Low-K	0
35	Low-K	150
29	Low-K	250

† Board types are as defined by JEDEC. Reference JEDEC Standard JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements.

Table 6−2. Thermal Resistance Characteristics (Case)

$R_{\Theta JC}$ (°C/W)	BOARD TYPE†
6	2s JEDEC Test Card

† Board types are as defined by JEDEC. Reference JEDEC Standard JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements.

6.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320SP103AZGW2	NRND	BGA MICROSTAR	ZGW	240	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	VC5510AZGW2 TMS320	
TMS320VC5510AGGW1	NRND	BGA MICROSTAR	GGW	240	126	TBD	SNPB	Level-3-220C-168 HR	0 to 0	VC5510AGGW1 TMS320	
TMS320VC5510AGGW2	NRND	BGA MICROSTAR	GGW	240	126	TBD	SNPB	Level-3-220C-168 HR	0 to 0	VC5510AGGW2 TMS320	
TMS320VC5510AGGWA1	NRND	BGA MICROSTAR	GGW	240	126	TBD	SNPB	Level-3-220C-168 HR	0 to 0	VC5510AGGWA1 TMS320	
TMS320VC5510AGGWA2	NRND	BGA MICROSTAR	GGW	240	126	TBD	SNPB	Level-3-220C-168 HR	0 to 0	VC5510AGGWA2 TMS320	
TMS320VC5510AZGW1	NRND	BGA MICROSTAR	ZGW	240	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	VC5510AZGW1 TMS320	
TMS320VC5510AZGW2	NRND	BGA MICROSTAR	ZGW	240	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	VC5510AZGW2 TMS320	
TMS320VC5510AZGWA1	NRND	BGA MICROSTAR	ZGW	240	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	VC5510AZGWA1 TMS320	
TMS320VC5510AZGWA2	NRND	BGA MICROSTAR	ZGW	240	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	VC5510AZGWA2 TMS320	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

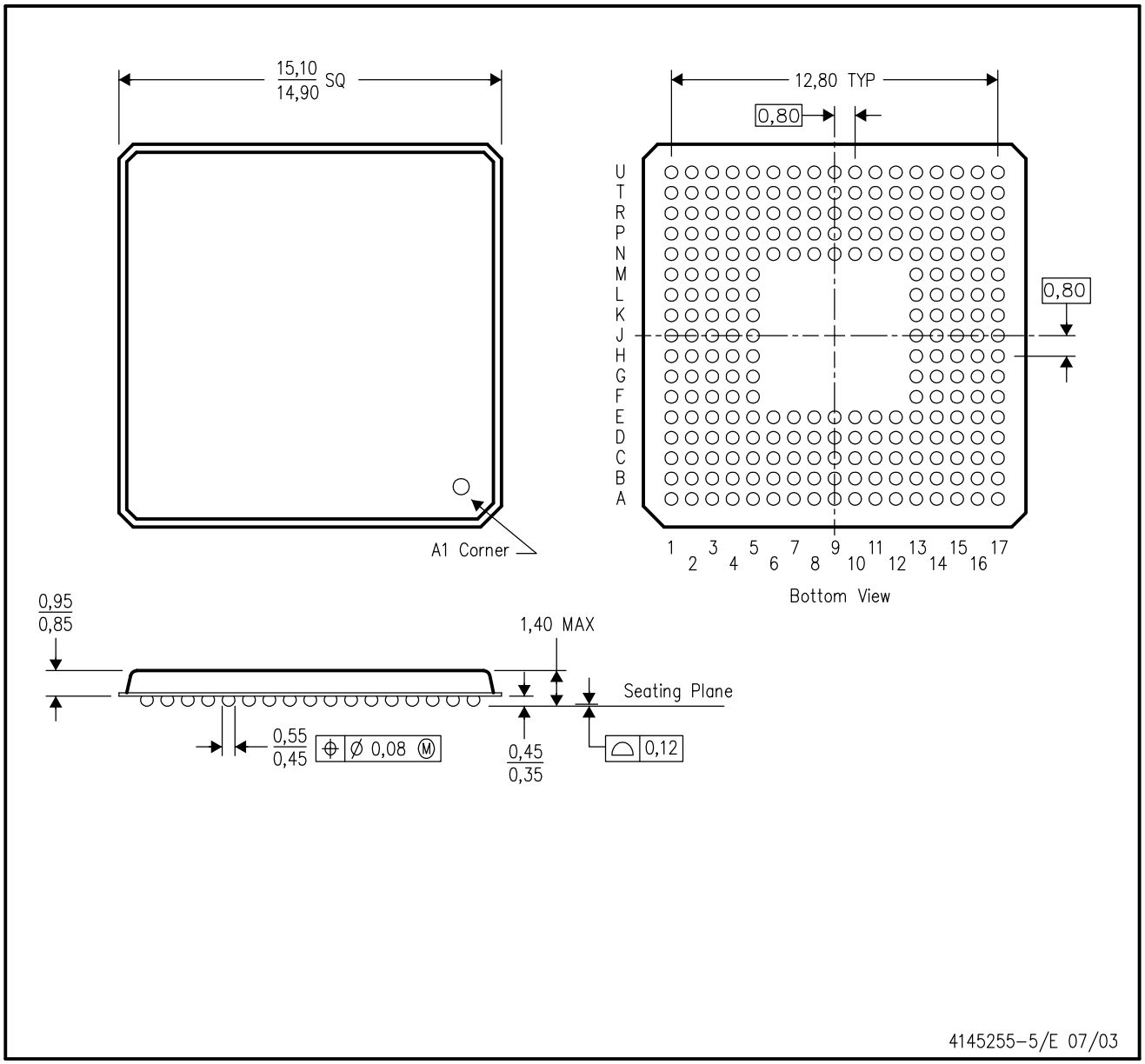
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

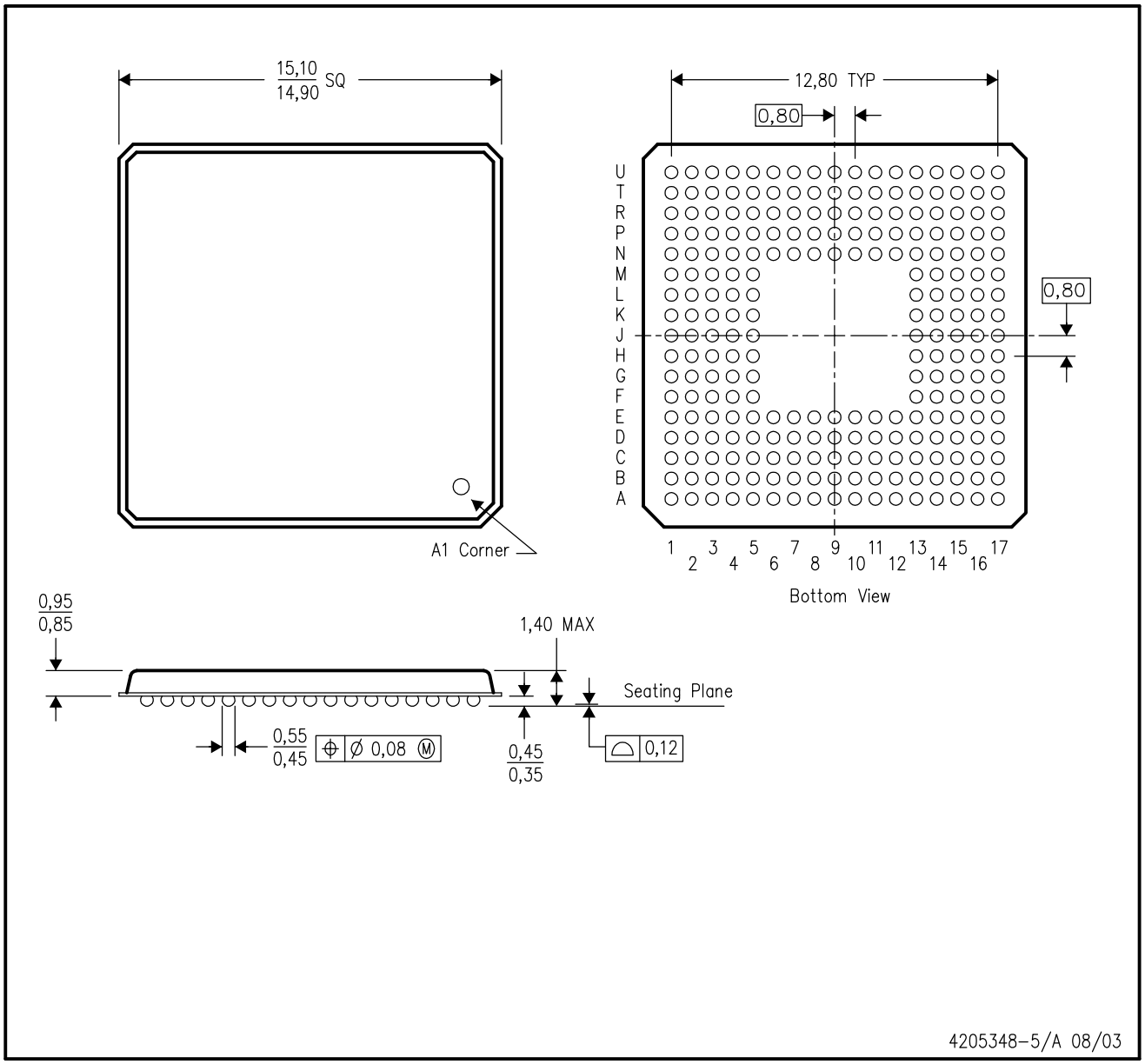
GGW (S–PBGA–N240) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments.

ZGW (S–PBGA–N240) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration
D. This package is lead–free.

MicroStar BGA is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265