

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

The **SENDA3** Series of non-isolated dc-dc converters deliver exceptional electrical and thermal performance in industry-standard footprints for Point-of-Load converters. Operating from a 6.0Vdc-14Vdc input, these are the converters of choice for Intermediate Bus Architecture (IBA) and Distributed Power Architecture applications that require high efficiency, tight regulation, and high reliability in elevated temperature environments with low airflow.

非絶縁型DC/DCコンバータの **SENDA3** シリーズは業界標準のPOLコンバータと同じ端子配列で極めて優れた電気的特性、及び温度特性を提供します。

入力電圧6V~14Vで動作しますので、このコンバータは、高効率、高い出力電圧精度、高温、及び風量の少ない環境での高信頼性が要求されるIBA、又はDPAでの使用に最適です。

The **FPLR12SR7525*A** converter of the **SENDA3** Series delivers 25A of output current at a tightly regulated programmable output voltage of 0.7525Vdc to 5.5Vdc. The thermal performance of the **FPLR12SR7525*A** is best-in-class: Little derating is needed up to 85°C, under natural convection.

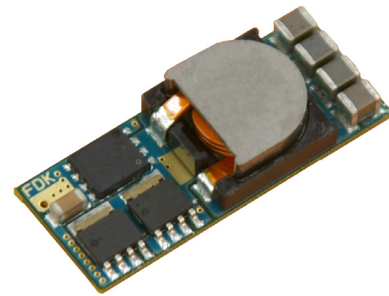
SENDA3 シリーズの **FPLR12SR7525*A** は高い電圧精度で0.7525V~5.5Vdcの可変を実現します。**FPLR12SR7525*A**の温度特性はクラス最高レベルです。自然対流、85°Cの条件で、わずかなデレーティングしか必要としません。

This leading edge thermal performance results from electrical, thermal and packaging design that is optimized for high density circuit card conditions. Extremely high quality and reliability are achieved through advanced circuit and thermal design techniques and FDK's state of the art in-house manufacturing processes and systems.

回路設計、放熱設計、及びパッケージング設計の結果である最先端の温度特性は、高密度実装回路用に最適化されています。非常に優れた品質と信頼性は高度な回路設計、温度設計技術、及びFDKの最先端の自社製造プロセスによりもたらされます。

Applications

- Intermediate Bus Architecture
中間バス構成システム
- Telecommunications
テレコムシステム
- Data/Voice processing
データ処理システム
- Distributed Power Architecture
分散型電源システム
- Computing (Servers, Workstations)
コンピュータ関係(サーバー、ワークステーション)



FPLR12SR7525*A

Features

- Delivers up to 25A (137.5W)
25A (137.5W)まで供給可能
- High efficiency, no heatsink required
高効率-放熱器が不要
- Negative and Positive ON/OFF logic
ON/OFFロジックはネガティブとポジティブ
- Industry-standard SMD footprint
業界標準のSMDフットプリント
- RoHS compliance
RoHS準拠
- Small size and low profile: 1.30" x 0.53" x 0.327" nominal
小型、低背 (33.0 x 13.4 x 8.3mm)
- Coplanarity less than 0.004"
平面度は0.1mm以下
- Tape and reel packaging
梱包はテーピング仕様
- Programmable output voltage via external resistor
外部接続の抵抗によりプログラム可能な出力電圧
- No minimum load required
最小負荷は不要
- Start up into pre-biased output
出力にプリバイアスがあっても起動可能
- Remote ON/OFF
リモートON/OFF機能
- Auto-reset output over-current protection
過電流保護機能: 自動復帰
- Auto-reset over-temperature protection
内部加熱保護機能: 自動復帰
- High reliability, MTBF = 1 Million Hours
高信頼性: MTBF = 1 Million Hours
- UL60950 recognition in U.S. & Canada, and CB Scheme certification per IEC/EN60950
UL60950、CB Scheme
- All materials meet UL94, V-0 flammability rating
全ての部品は UL94 V-0に適合

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6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Electrical Specifications 電氣的仕様

All specifications apply over specified input voltage, output load, and temperature range, unless otherwise noted.
 注記が無い場合、全ての仕様は指定された入力電圧、負荷、温度範囲で適用されます。

Conditions: $T_a=25\text{degC}$, Airflow=200LFM (1.0m/s), $V_{in}=12\text{Vdc}$, $V_{out}=0.7525\text{-}5.5\text{Vdc}$, unless otherwise specified.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS¹					
Input Voltage	Continuous	-0.3		15	Vdc
Operating Temperature	Ambient temperature	-40		85	°C
Storage Temperature		-55		125	°C
Output Voltage		0.7525		5.5	Vdc
FEATURE CHARACTERISTICS					
Switching Frequency			320		kHz
Output Voltage Programming Range	By external resistor. See trim table-1	0.7525		5.5	Vdc
Remote Sense Compensation				0.5	Vdc
Turn-On Delay Time	Full resistive load				
with V_{in} (module enabled, then V_{in} applied)	From $V_{in}=V_{in}(\text{min})$ to $0.1*V_{out}(\text{nom})$		5.0		ms
with Enable (V_{in} applied, then enabled)	From enable to $0.1*V_{out}(\text{nom})$		5.0		ms
Rise Time (Full resistive load)	From $0.1*V_{out}(\text{nom})$ to $0.9*V_{out}(\text{nom})$		5.0		ms
ON/OFF Control (Negative Logic)					
Module Off		2.4		V_{in}	Vdc
Module On		-5		0.8	Vdc
ON/OFF Control (Positive Logic)					
Module Off		-5		$V_{in}-2.7$	Vdc
Module On		$V_{in}-1.0$		V_{in}	Vdc

¹Absolute Maximum Ratings 絶対最大定格

Stresses in excess of the absolute maximum ratings may lead to degradation in performance and reliability of the converter and may result in permanent damage.

絶対最大定格を超えたストレスは、性能の低下、長期信頼性の低下、及びモジュールの破損を引き起こすことがあります。

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Electrical Specifications (Continued) 電氣的仕様 (続き)

Conditions: $T_a=25\text{degC}$, Airflow=200LFM (1.0m/s), $V_{in}=12\text{Vdc}$, $V_{out}=0.7525\text{-}5.5\text{Vdc}$, unless otherwise specified.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Operating Input Voltage Range	$V_{out} \leq 3.8\text{Vdc}$ (3.3Vdc+15%)	6	12	14	Vdc
	$V_{out} > 3.8\text{Vdc}$ (3.3Vdc+15%)	8	12	14	Vdc
Input Under Voltage Lockout					
Turn-on Threshold			5.5		Vdc
Turn-off Threshold			4.4		Vdc
Maximum Input Current	25Adc out at 6.0Vdc in				
	$V_{out}=5.0\text{Vdc}$ (25Adc at 8.0Vdc in)			16.5	Adc
	$V_{out}=3.3\text{Vdc}$			14.9	Adc
	$V_{out}=2.5\text{Vdc}$			11.5	Adc
	$V_{out}=2.0\text{Vdc}$			9.4	Adc
	$V_{out}=1.8\text{Vdc}$			8.5	Adc
	$V_{out}=1.5\text{Vdc}$			7.2	Adc
	$V_{out}=1.2\text{Vdc}$			6.0	Adc
	$V_{out}=1.0\text{Vdc}$			5.1	Adc
Input Stand-by Current (module disabled)			2.5		mA
Input No Load Current	$V_{out}=5.0\text{Vdc}$		85		mA
	$V_{out}=3.3\text{Vdc}$		67		mA
	$V_{out}=2.5\text{Vdc}$		55		mA
	$V_{out}=2.0\text{Vdc}$		47		mA
	$V_{out}=1.8\text{Vdc}$		45		mA
	$V_{out}=1.5\text{Vdc}$		40		mA
	$V_{out}=1.2\text{Vdc}$		37		mA
	$V_{out}=1.0\text{Vdc}$		35		mA
Input Reflected-Ripple Current	See Fig. F for setup (BW=20MHz)				
	$V_{out}=5.0\text{Vdc}$		140		mAp-p
	$V_{out}=3.3\text{Vdc}$		120		mAp-p
	$V_{out}=2.5\text{Vdc}$		100		mAp-p
	$V_{out}=2.0\text{Vdc}$		90		mAp-p
	$V_{out}=1.8\text{Vdc}$		85		mAp-p
	$V_{out}=1.5\text{Vdc}$		75		mAp-p
	$V_{out}=1.2\text{Vdc}$		65		mAp-p
	$V_{out}=1.0\text{Vdc}$		55		mAp-p

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Electrical Specifications (Continued) 電氣的仕様 (続き)

Conditions: $T_a=25\text{degC}$, Airflow=200LFM (1.05m/s), $V_{in}=12\text{Vdc}$, $V_{out}=0.7525\text{-}5.5\text{Vdc}$, unless otherwise specified.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS					
Output Voltage Set Point (no load)		-1.5	V_{out}	+1.5	% V_{out}
Output Regulation					
Over Line	Full resistive load		+/- 0.1		% V_{out}
Over Load	From no load to full load		+/- 0.4		% V_{out}
Output Voltage Range (Over all operating input voltage, resistive load and temperature conditions until end of life)		-3		+3	% V_{out}
Output Ripple and Noise BW=20MHz					
Peak to Peak	$V_{out}=1.0\text{Vdc}$		25	80	mVp-p
Peak to Peak	$V_{out}=5.0\text{Vdc}$		75	150	mVp-p
External Load Capacitance					
Min ESR > 1m Ω				1000	μF
Min ESR > 10m Ω				5000	μF
Output Current Range					
Output Current Limit Inception (I_{out})	$V_{out}=3.3\text{Vdc}$		33		A
Output Short-Circuit Current	Short=10m Ω , $V_{out}=3.3\text{Vdc}$ set		8.3		Arms
DYNAMIC RESPONSE					
I_{out} step from 12.5A to 25A with $di/dt=5\text{A}/\mu\text{S}$	$C_o=47\mu\text{F} \times 4$ ceramic + 1 μF ceramic		180		mV
Setting time ($V_{out} < 10\%$ peak deviation)			60		μS
I_{out} step from 25A to 12.5A with $di/dt=5\text{A}/\mu\text{S}$	$C_o=47\mu\text{F} \times 4$ ceramic + 1 μF ceramic		180		mV
Setting time ($V_{out} < 10\%$ peak deviation)			60		μS
EFFICIENCY					
Full load (25A)					
	$V_{out}=5.0\text{Vdc}$		94.5		%
	$V_{out}=3.3\text{Vdc}$		92.5		%
	$V_{out}=2.5\text{Vdc}$		90.0		%
	$V_{out}=2.0\text{Vdc}$		88.5		%
	$V_{out}=1.8\text{Vdc}$		87.5		%
	$V_{out}=1.5\text{Vdc}$		85.0		%
	$V_{out}=1.2\text{Vdc}$		83.0		%
	$V_{out}=1.0\text{Vdc}$		80.5		%

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Operation

Input and Output Impedance

The **FPLR12SR7525*A** converter should be connected to a DC power source using a low impedance input line. In order to counteract the possible effect of input line inductance on the stability of the converter, the use of decoupling capacitors placed in close proximity to the converter input pins is recommended. This will ensure stability of the converter and reduce input ripple voltage. Although low ESR Tantalum or other capacitors should typically be adequate, very low ESR capacitors (ceramic, over 200 μ F) are recommended to minimize input ripple voltage. The converter itself has on-board internal input capacitance of 20 μ F with very low ESR (ceramic).

FPLR12SR7525*Aと入力電源間は低インピーダンスで接続してください。コンバータの安定性に影響のある入力インダクタンスを抑えるため、コンバータの入力ピンの近傍にデカップリングコンデンサを付加することをお勧めします。これによりコンバータの安定動作を確実にし、入力リップル電圧を抑制します。低ESRタンタル、又はその他のコンデンサも一般的には問題ありませんが、入力リップルを最小にするためには、非常に低ESRコンデンサ(セラミックで200 μ F以上)を推奨します。コンバータ自身は入力回路に極低ESRの20 μ Fセラミック入力コンデンサを搭載しています。

The **FPLR12SR7525*A** is capable of stable operation with no external capacitance on the output. To minimize output ripple voltage, the use of very low ESR ceramic capacitors is recommended. These capacitors should be placed in close proximity to the load to improve transient performance and to decrease output voltage ripple.

FPLR12SR7525*Aは出力に外付けコンデンサが無い状態でも安定して動作します。出力リップルを最小にするため、極低ESRのセラミックコンデンサの接続を推奨します。過渡時の特性向上と出力リップル低減のために負荷の近傍に極低ESRセラミックコンデンサを実装することをお勧めします。

Note that the converter has a SENSE pin to counteract voltage drops between the output pins and the load. However, the impedance of the line from the converter output to the load should thus be kept as low as possible to maintain good load regulation.

このコンバータは出力端子と負荷間の電圧ドロップを補正するセンス端子を持っています。しかしながら、精度の高い負荷特性を保持するために、コンバータの出力から負荷までのラインインピーダンスは可能な限り低くしてください。

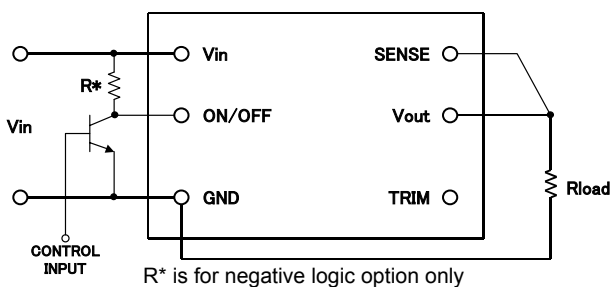


Fig. A: Circuit configuration for remote ON/OFF

ON/OFF (Pin 6)

The ON/OFF pin (pin 6) can be used to turn the converter on or off remotely using a signal that is referenced to GND (pin 2), as shown in Fig. A.

Two remote control options are available, corresponding to negative and positive logic. In the negative logic option, to turn the converter on Pin 6 should be at logic low or left open, and to turn the converter off Pin 6 should be at logic high or connected to Vin. In the positive logic option, to turn the converter on Pin 6 should be at logic high, connected to Vin or left open, and to turn the converter off Pin 6 should be at logic low.

ON/OFF端子(6番ピン)は図Aのように、グラウンド(2番ピン)を基準としたリモート信号によりコンバータをON/OFFするのに使われます。ネガティブとポジティブロジックに対応するため、2種類のリモートコントロールを選択可能です。ネガティブオプションの場合、コンバータをONするには6番ピンをLowレベル、又は未接続とし、コンバータをOFFするには6番ピンをHighレベル、又はVinと接続とします。ポジティブオプションの場合、コンバータをONするには6番ピンをHighレベル、Vinに接続、又は未接続とし、コンバータをOFFするには6番ピンをLowレベルにします。

For a positive logic option, the ON/OFF pin (pin6) is internally pulled-up to Vin. An open collector (open-drain) transistor can be used to drive Pin 6.

The device driving Pin 6 must be capable of:

- (a) Sinking up to 0.3mA at low logic level
- ポジティブオプションの場合、ON/OFFピンはモジュール内部でVinにプルアップされています。オープンコレクタ(オープンドレイン)のトランジスタがON/OFFピンの操作に使用可能です。
- ON/OFFピンを操作するデバイスには下記能力が必要です。
- (a) Lowレベルで0.3mA程度のシンク能力

For a negative logic option, the ON/OFF pin (pin6) is internally pulled-down. A TTL or CMOS logic gate, or an open collector (open-drain) transistor can be used to drive Pin 6. When using an open collector (open-drain) transistor, a pull-up resistor, $R^*=75k\Omega$, should be connected to Vin (See Fig.A).

The device driving Pin 6 must be capable of:

- (b) Sinking up to 0.2mA at low logic level ($\leq 0.8V$)
- (c) Sourcing up to 0.25mA at high logic level (2.3~5V)
- (d) Sourcing up to 0.75mA when connected to Vin

ネガティブオプションの場合、ON/OFFピンはモジュール内部でプルダウンされています。TTL、CMOSロジック、又はオープンコレクタ(オープンドレイン)のトランジスタもON/OFFピンの操作に使用可能です。オープンコレクタ(オープンドレイン)のトランジスタを使用する時は75k Ω のプルアップ抵抗をVinに接続してください。

(図A参照)

ON/OFFピンを操作するデバイスには下記能力が必要です。

- (b) 0.8V以下のLowレベルで0.2mAまでのシンク能力
- (c) 2.3V~5VのHighロジックレベルで0.25mAまでの供給能力
- (d) Vin接続時には0.75mAまでの供給能力

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Remote Sense (Pin 5)

The **FPLR12SR7525*A** converter incorporates a remote sense function to compensate for voltage drops between Vout (pin 3) and the load. SENSE (pin 5) should be connected via a separate trace to a point close to the load or to a point where regulation is required; see Fig. B. This trace should be located in proximity to a ground plane to minimize noise pick-up. Note that GND (pin 2) does not have a sense function: good connectivity to a ground plane is needed for low voltage drop.

In case the remote sense function is not required, SENSE (pin 5) must be connected to Vout (Pin 3). In the absence of this connection, the converter will provide a slightly higher output voltage than that specified.

FPLR12SR7525*AコンバータはVout(3番ピン)と負荷の間で起こる電圧低下を補正するために、リモートセンス機能を有しています。SENSE(5番ピン)は負荷端、又は補正が必要な箇所に個別の配線で接続してください。(図B参照) この配線はノイズの影響を最小にするため、グラウンドに近接して配線してください。GND(2番ピン)はセンス機能がありませんので、電圧低下を少なくするためにグラウンドに良好な接続が必要です。

リモートセンス機能が不要な場合は、SENSE(5番ピン)はVout(3番ピン)に接続してください。接続が無い場合、コンバータは出力電圧規格より若干高い電圧を出力します。

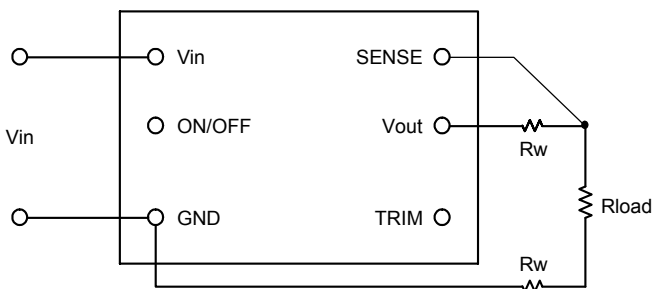


Fig. B: Remote Sense Circuit Configuration

Note that the remote sense function will allow the output voltage at Vout to be up to 0.5V above the nominal rated voltage in order to maintain regulation at the sense point. The system design should take this into account to ensure that the maximum power drawn from the converter under a given set of conditions does not exceed that allowed by the derating curves.

リモートセンス機能は、センス箇所の電圧を規格内にするため、Vout端の電圧を基準出力電圧より最大0.5V高くします。システムをデザインする際、この機能に留意し、テイルテイングカーブで許容される最大電力以下で使用するように、注意してください。

Output Voltage Programming (Pin 4)

The output voltage of the **FPLR12SR7525*A** converter can be programmed from 0.7525V to 5.5V by using an external resistor or a voltage source

FPLR12SR7525*Aの出力電圧は外部抵抗を接続するか、又は外部電源を印加することで 0.7525V~5.5Vまで可変可能です。

External Resistor

An external trim resistor, R_{TRIM} , should be connected between TRIM (pin 4) and GND (pin 2); see Fig. C. The value of R_{TRIM} , in $k\Omega$, for a desired output voltage, V_{O-REQ} , in V, is given by:

外部抵抗 R_{TRIM} はTRIM端子(4番ピン)とGND端子(2番ピン)の間に接続してください。図Cを参照。 R_{TRIM} の定数、及び必要な出力電圧は次の式により求めます。

$$R_{TRIM} = \frac{10.5}{(V_{O-REQ} - 0.7525)} - 1 \text{ [k}\Omega\text{]}$$

Note that the tolerance of a trim resistor will affect the tolerance of the output voltage. Standard 1% or 0.5% resistors may suffice for most applications; however, a tighter tolerance can be obtained by using two resistors in series instead of one standard value resistor.

Table 1 lists calculated values of R_{TRIM} for common output voltages. For each value of R_{TRIM} , Table 1 also shows the closest available standard resistor value.

R_{TRIM} の公差は出力電圧の公差に影響します。ほとんどの使用状況においては、標準的な1%又は0.5%品の抵抗で十分です。しかしながら、より厳しい出力精度のためには、抵抗1本よりも2本を直列に使用します。Table 1に一般的な出力電圧を設定する際の抵抗値を表示します。またTable 1に標準的な抵抗を使用した場合の近似値も表示しています。

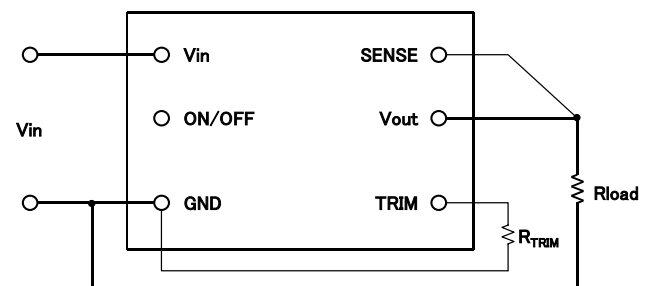


Fig. C: Configuration for programming output voltage

FPLR12SR7525*A

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Table 1: Trim Resistor Value

V _{O-REG} [V]	R _{TRIM} [kΩ]	The Closest Standard Value [kΩ]
0.7525	Open	
1.0	41.42	41.2
1.2	22.46	22.6
1.5	13.05	13.0
1.8	9.02	9.09
2.0	7.42	7.50
2.5	5.01	4.99
3.3	3.12	3.09
5.0	1.47	1.47
5.5	1.21	1.21

External Voltage Source

To program the output voltage using an external voltage source, a voltage, V_{CTRL}, should be applied to the TRIM pin. Use of a series resistor, R_{EXT}, between the TRIM pin and the programming voltage source is recommended to make trimming less sensitive.

外部電源を使って出力電圧を可変するには、TRIM端子にV_{CTRL}の電圧を印加します。電圧設定が敏感すぎるのを避けるため、TRIM端子と外部電源間に抵抗を直列に接続することをお勧めします。

The voltage of the control voltage V_{CTRL}, in V, for a given value of R_{EXT}, in kΩ, is given by:

V_{CTRL}電圧は下記の式により算出が可能です。

$$V_{CTRL} = 0.7 - \frac{(1 + R_{EXT})(V_{O-REQ} - 0.7525)}{15} \quad [V]$$

Table 2 lists values of V_{CTRL} for R_{EXT}=0 and R_{EXT}=15kΩ.

Table 2はR_{EXT}=0の時とR_{EXT}=15kの時とR_{EXT}電圧を表しています。

Table 2: Control Voltage [Vdc]

V _{O-REG} [V]	V _{CTRL} (R _{EXT} =0)	V _{CTRL} (R _{EXT} =15k)
0.7525	0.700	0.700
1.0	0.684	0.436
1.2	0.670	0.223
1.5	0.650	-0.097
1.8	0.630	-0.417
2.0	0.617	-0.631
2.5	0.584	-1.164
3.3	0.530	-2.017
5.0	0.417	-3.831
5.5	0.384	-4.364

Protection Features

Input Under-Voltage Lockout

From a turned-on state, the converter will turn off automatically when the input voltage drops below typically 4.4V. It will then turn on automatically when the input voltage reaches typically 5.5V.

動作している状態で入力電圧がTYPで4.4V未満になると、このコンバータは自動的に停止します。また、入力電圧がTYPで5.5V以上になると、このコンバータは自動的に動作を開始します。

Output Over-Current Protection (OCP)

The converter is self-protected against over-current and short circuit conditions. On the occurrence of an over-current condition, the converter will enter a pulse-by-pulse hiccup mode. On the removal of the over-current or short circuit condition, V_{out} will return to the original value (auto-reset).

このコンバータは過電流と短絡に対し自己保護します。過電流状態になると、このコンバータはパルス・ハイ・パルス HICCUPモードになり、過電流状態が解除されるとV_{out}は通常の値に戻ります。(自動リセット)

Over-Temperature Protection (OTP)

The converter is self-protected against over-temperature conditions. In case of overheating due to abnormal operation conditions, the converter will turn off automatically. It will turn back on automatically once it has cooled down to a safe temperature (auto-reset).

このコンバータは加熱保護機能を有しています。異常な動作条件によって加熱状態になると、このコンバータは自動的に停止します。安全な温度にまで下がると自動的に復帰します。(自動リセット)

Safety Requirements

The converter meets North American and International safety regulatory requirements per UL60950 and EN60950. The converter meets SELV (safety extra-low voltage) requirements under normal operating conditions in that the output voltages are ELV (extra-low voltage) when all the input voltages are ELV. Note that the converter is not internally fused: to meet safety requirements, a fast acting in-line fuse with a maximum rating of TBD A must be used in the positive input line.

このコンバータはUL60950とEN60950による北米、及び国際的な安全基準を満たしています。このコンバータは通常の動作条件下においてSELVの条件を満たしており、入力電圧がELVであれば出力電圧もELVとなります。但し、このコンバータは内部にヒューズを持っていませんので、安全規格に適合させるためには、入力ラインのプラス側に即断型で最大定格TBDAのヒューズを接続してください。

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Characterization

Overview

The converter has been characterized for several operational features, including thermal derating (maximum available load current as a function of ambient temperature and airflow), efficiency, power dissipation, start-up and shutdown characteristics, ripple and noise, and transient response to load step-changes.

このコンバータは温度デレティング、効率、電力損失、スタートアップ時、及びシャットダウン時の動作、リップル・ノイズ、動的負荷変動などを含む、さまざまな動作状態で特徴付けられます。

Figures showing data plots and waveforms for different output voltages are presented in the following pages. The figures are numbered as Fig.*V-#, where *V indicates the output voltage, and # indicates a particular plot type for that voltage. For example, Fig *V-2 is a plot of efficiency vs. load current for any output voltage *V.

各出力電圧時のデータ、及び波形の図は以後のページに掲載されています。図はFig *V-#のように番号付けされており、*Vは出力電圧を表し、#は特定のプロットを表します。例えば Fig *V-2とあれば、*V出力での効率特性を表します。

Test Conditions

To ensure measurement accuracy and reproducibility, all thermal and efficiency data were taken with the converter soldered to a standardized thermal test board. The thermal test board was mounted inside FDK's custom wind tunnel to enable precise control of ambient temperature and airflow conditions.

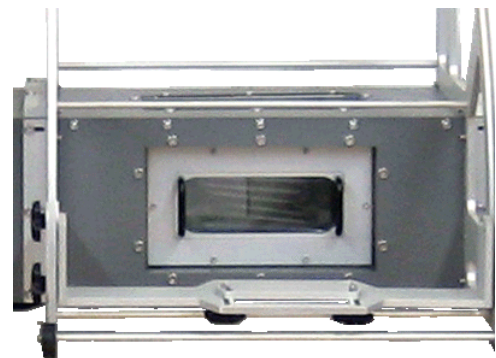
測定精度、及び再現性を確実にするために、全ての温度、及び効率データは標準化された温度評価ボードにコンバータを半田付けして取得しています。温度評価ボードをFDK特製の風洞実験設備内に設置することで、環境温度、及び風量を精密に管理しています。

The thermal test board comprised a four layer printed circuit board (PCB) with a total thickness of 0.060". Copper metallization on the two outer layers was limited to pads and traces needed for soldering the converter and peripheral components to the board. The two inner layers comprised power and ground planes of 2 oz. copper. This thermal test board, with the paucity of copper on the outer surfaces, limits heat transfer from the converter to the PCB, thereby providing a worst-case but consistent set of conditions for thermal measurements.

温度評価ボードは厚さ0.060"(1.6mm)厚の4層PCBで作成しています。表面2層の銅箔はコンバータを実装するためのパッドと周辺部品へのパターンのみに限られています。内側2層は70 μ mの銅箔で電力、及びグラウンドラインを形成しています。このように表層の銅箔を限りなく少なくした温度評価ボードは、コンバータからPCBへの熱の逃げを制限し、ワーストケースでありながら矛盾の無い温度評価条件を実現しています。



FDK Original Wind Tunnel



Test Chamber

FDK's custom wind tunnel was used to provide precise horizontal laminar airflow in the range of 50 LFM (equivalent to natural convection, NC) to 600LFM, at ambient temperatures between 30°C and 85°C. Infrared (IR) thermography and thermocouples were used for temperature measurements.

FDK特製の風洞実験装置は水平方向の層流を50LFM(自然対流と同等、NC)から600LFMまで精密に制御でき、環境温度は30°Cから85°Cを制御できます。温度測定には赤外線(IR)サーモグラフィと熱電対を使用しています。

It is advisable to check the converter temperature in the actual application, particularly if the application calls for loads close to the maximums specified by the derating curves. IR thermography or thermocouples may be used for this purpose. In the latter case, AWG#40 gauge thermocouples are recommended to minimize interference and measurement error. An optimum location for placement of a thermocouple is indicated in Fig. D.

コンバータの温度を実際の使用環境で測定することをお勧めします。特に実用上の負荷が温度デレティングの最大値に近い場合は測定が必要です。温度測定には赤外線サーモグラフィ、又は熱電対をお使いいただけます。熱電対を使用する場合、風の妨げになることを防ぐためと、測定誤差を少なくするため、AWG40の熱電対を推奨します。熱電対での測定に最適な箇所は図Dに示します。

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Thermal Derating

Figs *V-1 show the maximum available load current vs. ambient temperature and airflow rates. Ambient temperature was varied between 30°C and 85°C, with airflow rates from NC(50LFM) to 400LFM (0.25m/s to 2.0m/s). The converter was mounted horizontally, and the airflow was parallel to the short axis of the converter, going from pin 1 to pin 2.

図 *V-1はある環境温度と風量の条件下における最大出力電流を表します。環境温度は風量NC(50LFM)~400LFMの条件で30°C~85°Cの間を変動させています。コンバータは水平に設置し、風向きはコンバータの短手方向に平行で1番ピンから2番ピンに向けて吹いています。

The maximum available load current, for any given set of conditions, is defined as the lower of:

- (i) The output current at which the temperature of any component reaches 120°C, or
- (ii) The current rating of the converter (25A)

A maximum component temperature of 120°C should not be exceeded in order to operate within the derating curves. Thus, the temperature at the thermocouple location shown in Fig. D should not exceed 120°C in normal operation.

各々の測定条件で最大出力電流の値は下記のとおり定義します。

- (i) いずれかの部品の温度が120°Cに到達した時点の出力電流値又は
- (ii) コンバータの公称定格電流 (25A)

温度デレーティングの範囲内で動作させるために、部品温度は120°Cを超えないようにご注意ください。従って、通常動作時に図Dに示す位置の熱電対の温度が120°Cを超えないようにしてください。

Note that continuous operation beyond the derated current as specified by the derating curves may lead to degradation in performance and reliability of the converter and may result in permanent damage.

出力電流デレーティングカーブで指定された定格電流を超えた連続した操作は、性能の低下、信頼性の低下、及びモジュールの破損を引き起こすことがあります。

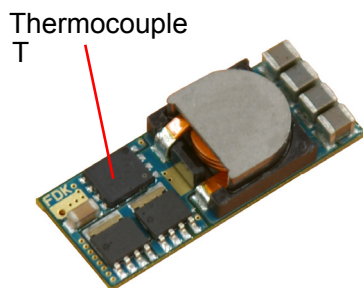


Fig. D: Location of the thermo couples for thermal testing

Ripple and Noise

The test circuit setup shown in Fig. E was used to obtain the output voltage ripple. And Fig. F was used to obtain the input reflected ripple current waveforms. The output voltage ripple waveform was measured across a 1µF ceramic capacitor at full load current.

図Eに示す試験回路は出力リップルの測定に使用しており、入力リップルの測定には図Fの試験回路を使用しています。全ての出力リップル波形は1µFのセラミックコンデンサを通して測定しています。

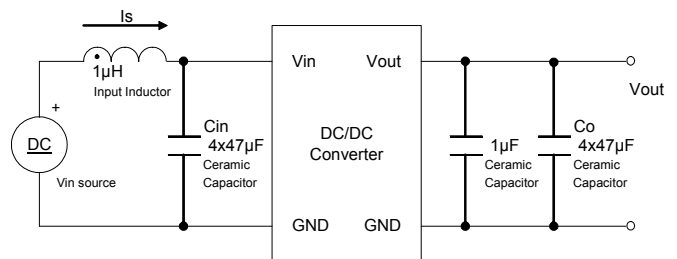


Fig. E: Test setup for measuring output voltage ripple

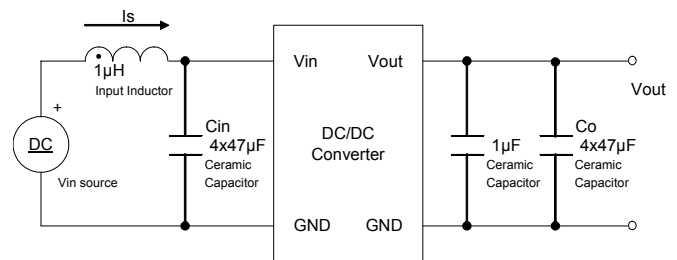


Fig. F: Test setup for measuring input reflected ripple current

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

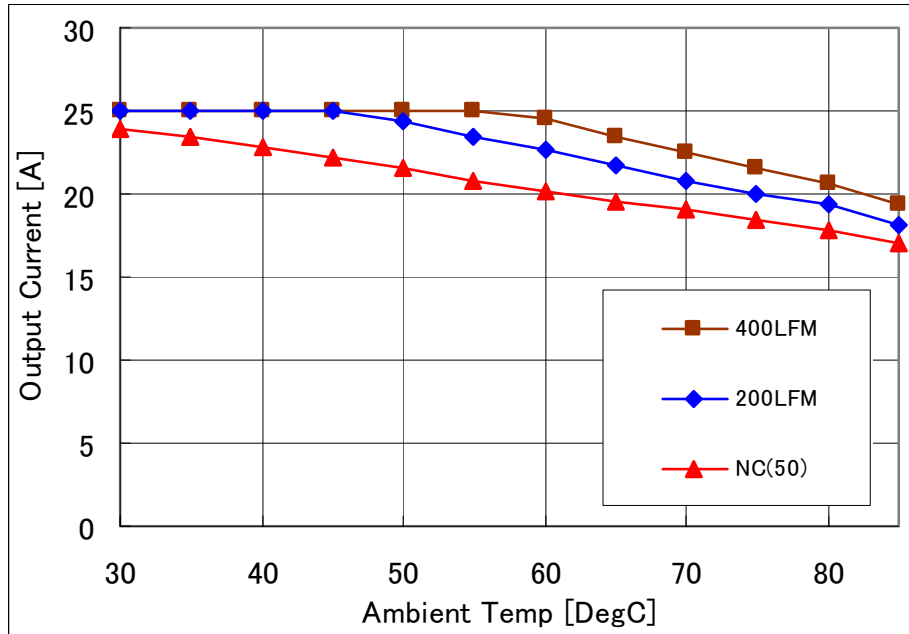


Fig-5.0V-1: Available load current vs. ambient temperature and airflow rates for Vout=5.0V with Vin=12V. Maximum component temperature $\leq 120^{\circ}\text{C}$

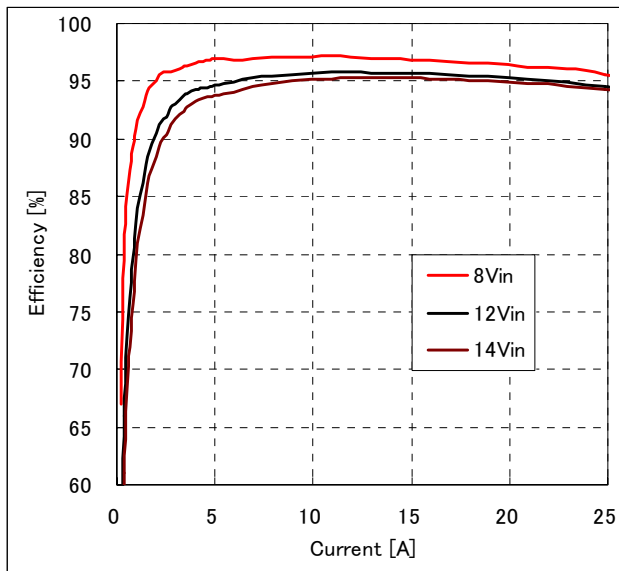


Fig-5.0V-2: Efficiency vs. load current and input voltage for Vout=5.0V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

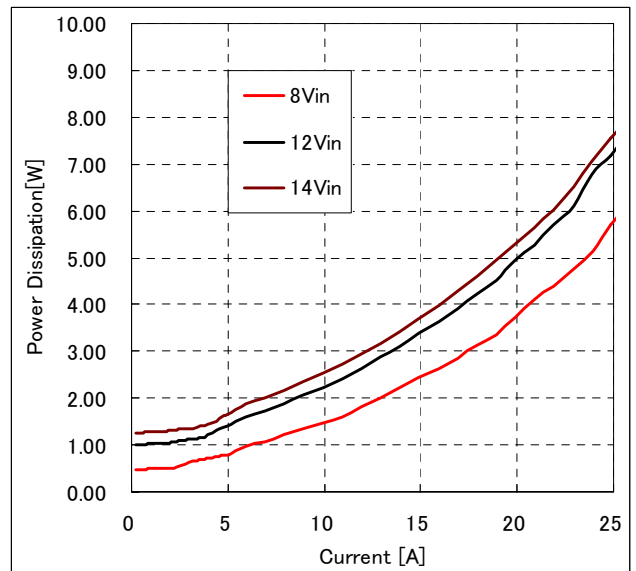


Fig-5.0V-3: Power Loss vs. load current and input voltage for Vout=5.0V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

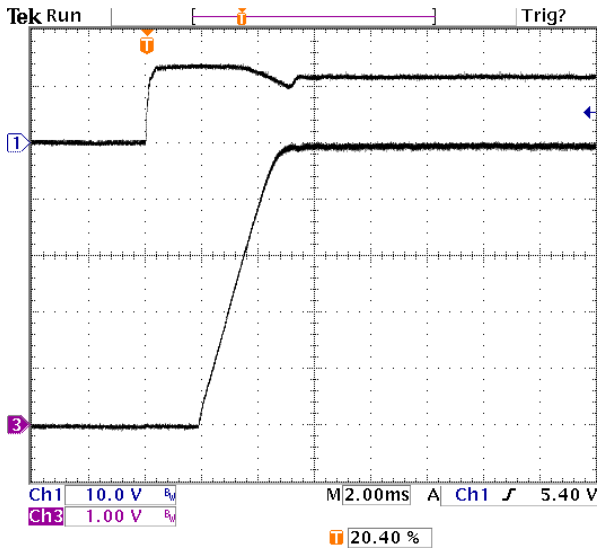


Fig-5.0V-4: Turn-on transient for $V_{out}=5.0V$ with application of V_{in} at full rated load current (resistive) and 47uF \times 4 external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)
 Time scale: 2 ms/div.

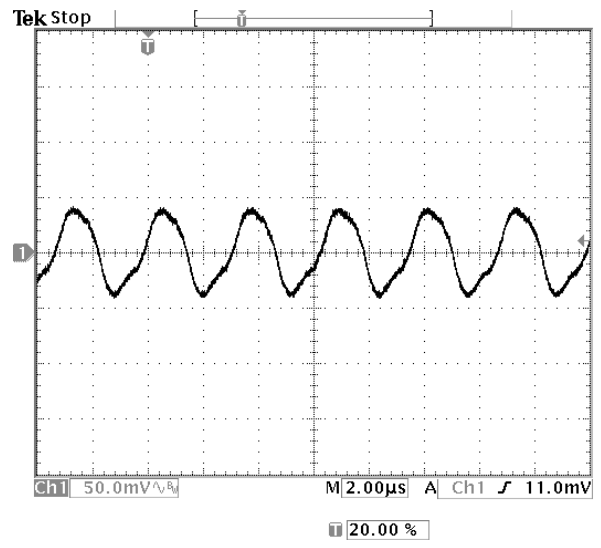


Fig-5.0V-5: Output voltage ripple (50mV/div.) for $V_{out}=5.0V$ at full rated load current into a resistive load with external capacitance 47uF \times 4 ceramic + 1uF ceramic at $V_{in}=12V$.
 Time scale: 2 us/div

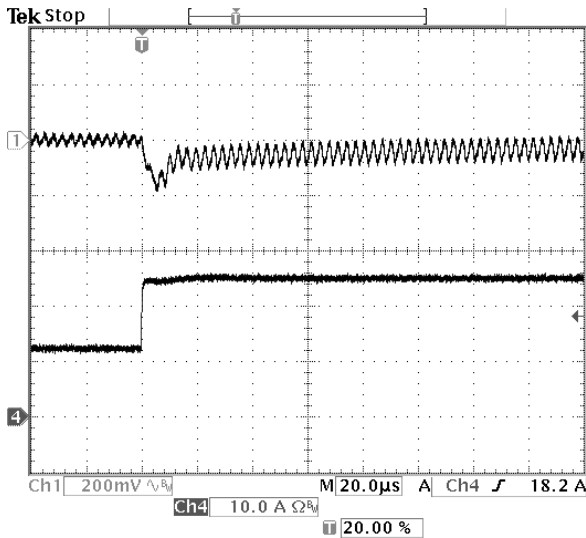


Fig-5.0V-6: Output voltage response for $V_{out}=5.0V$ to positive load current step change from 12.5A to 25A with slew rate of 5A/us at $V_{in}=12V$.
 $C_o=47uF \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

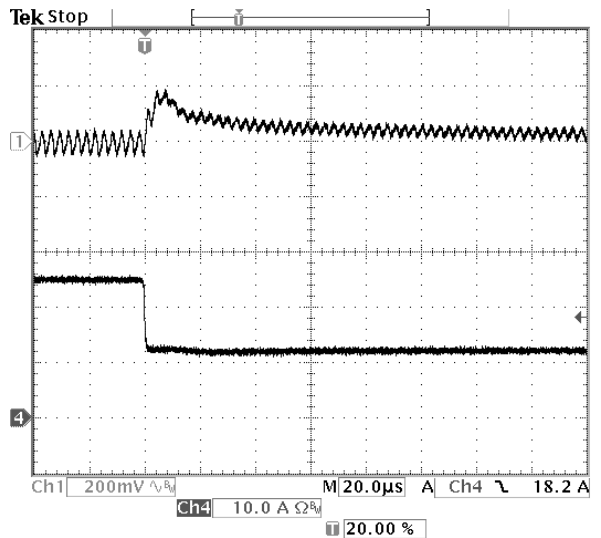


Fig-5.0V-7: Output voltage response for $V_{out}=5.0V$ to negative load current step change from 25A to 12.5A with slew rate of -5A/us at $V_{in}=12V$.
 $C_o=47uF \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

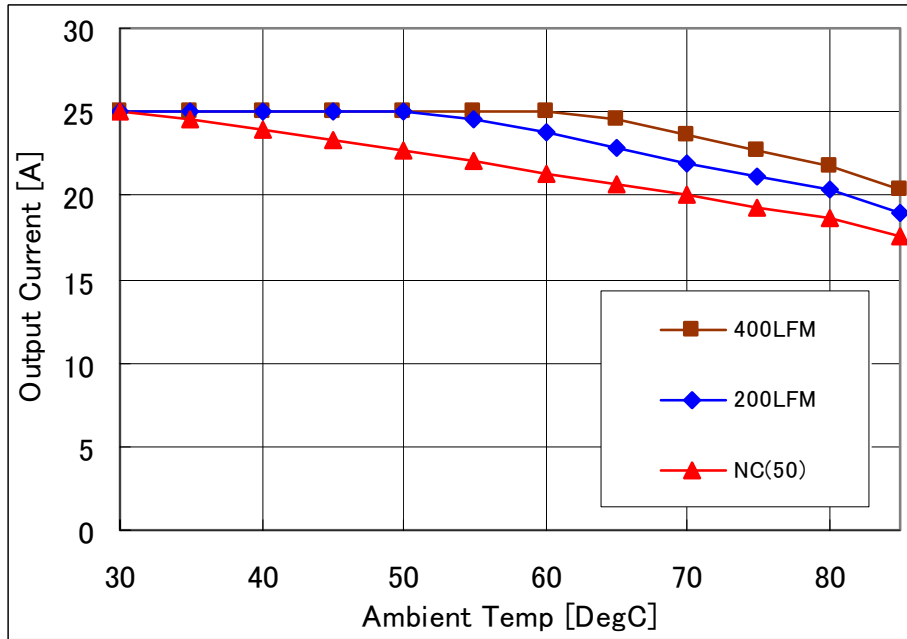


Fig-3.3V-1: Available load current vs. ambient temperature and airflow rates for Vout=3.3V with Vin=12V. Maximum component temperature $\leq 120^{\circ}\text{C}$.

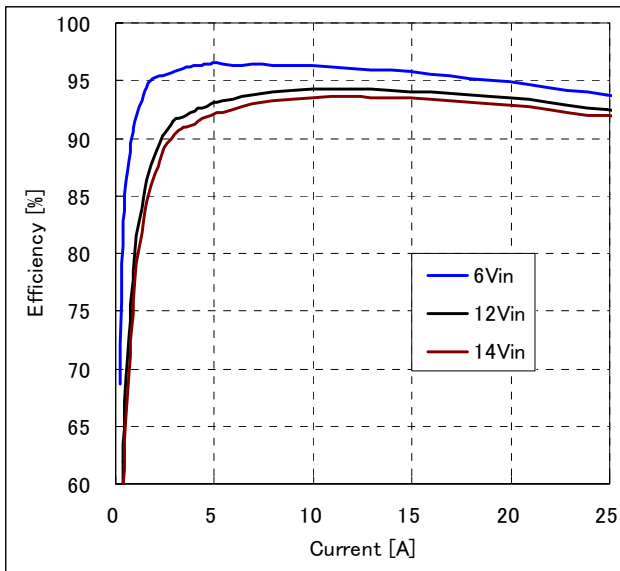


Fig-3.3V-2: Efficiency vs. load current and input voltage for Vout=3.3V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

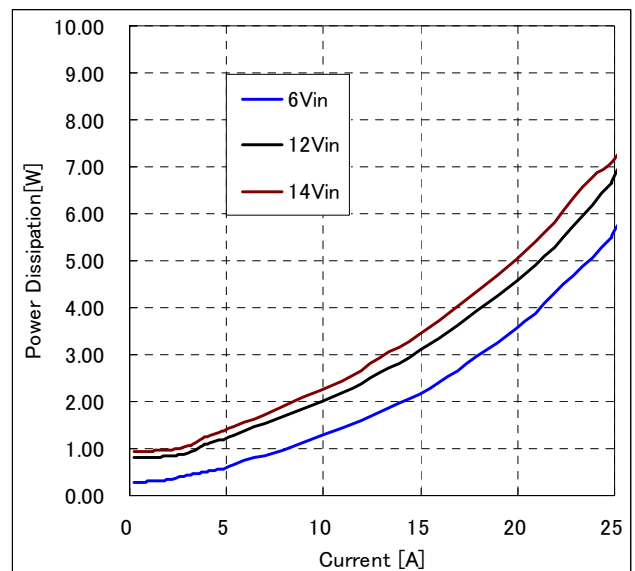


Fig-3.3V-3: Power Loss vs. load current and input voltage for Vout=3.3V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

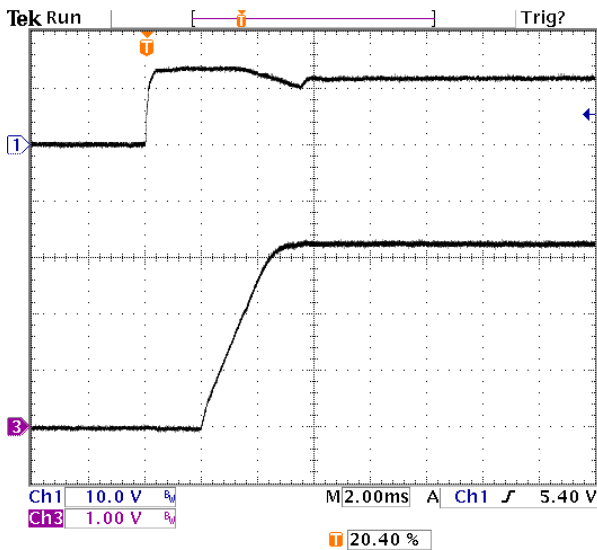


Fig-3.3V-4: Turn-on transient for $V_{out}=3.3V$ with application of V_{in} at full rated load current (resistive) and $47\mu F \times 4$ external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)

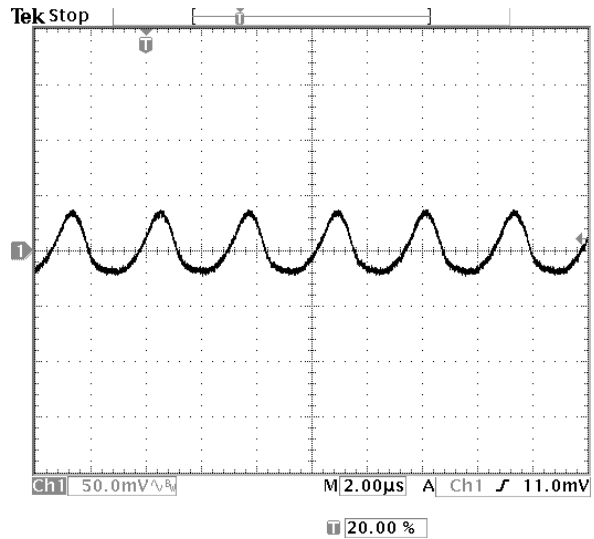


Fig-3.3V-5: Output voltage ripple (50mV/div.) for $V_{out}=3.3V$ at full rated load current into a resistive load with external capacitance $47\mu F \times 4$ ceramic + $1\mu F$ ceramic at $V_{in}=12V$.
 Time scale: 2 μs /div

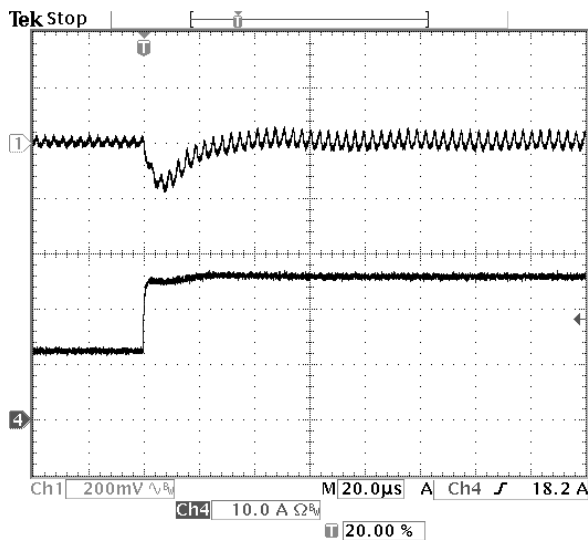


Fig-3.3V-6: Output voltage response for $V_{out}=3.3V$ to positive load current step change from 12.5A to 25A with slew rate of $5A/\mu s$ at $V_{in}=12V$. $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20 μs /div.

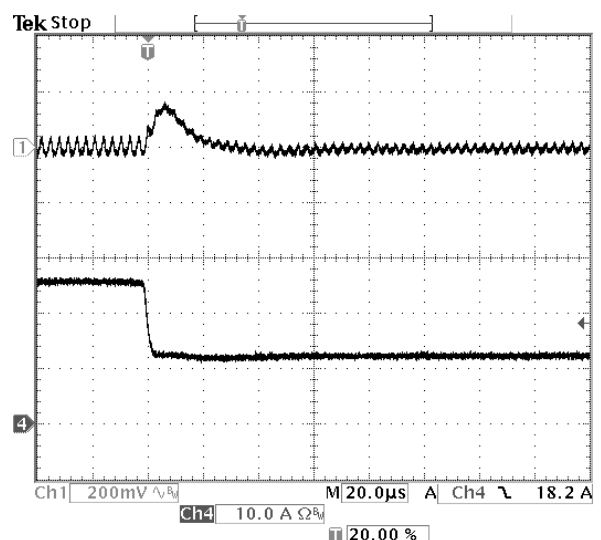


Fig-3.3V-7: Output voltage response for $V_{out}=3.3V$ to negative load current step change from 25A to 12.5A with slew rate of $-5A/\mu s$ at $V_{in}=12V$. $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

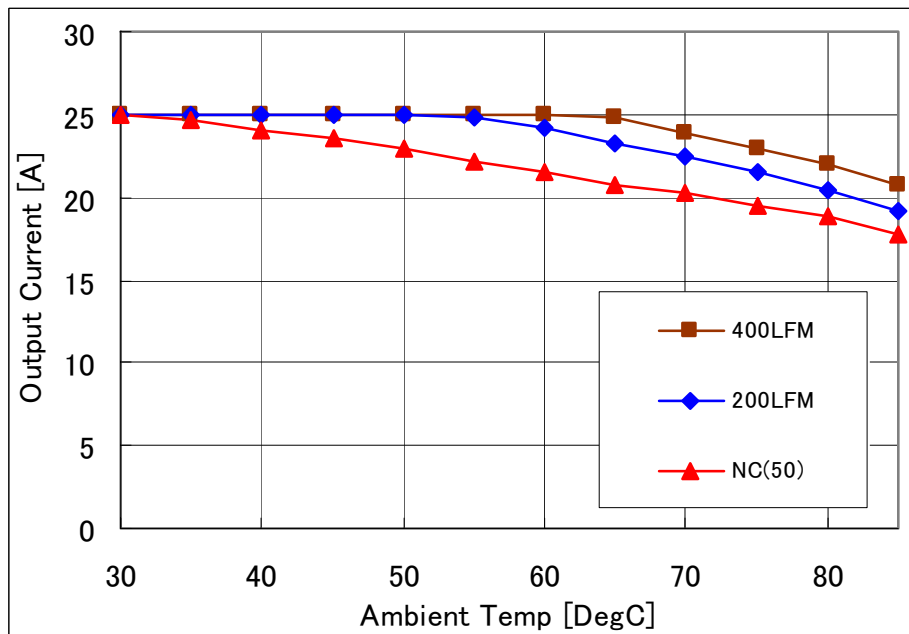


Fig-2.5V-1: Available load current vs. ambient temperature and airflow rates for Vout=2.5V with Vin=12V. Maximum component temperature $\leq 120^{\circ}\text{C}$

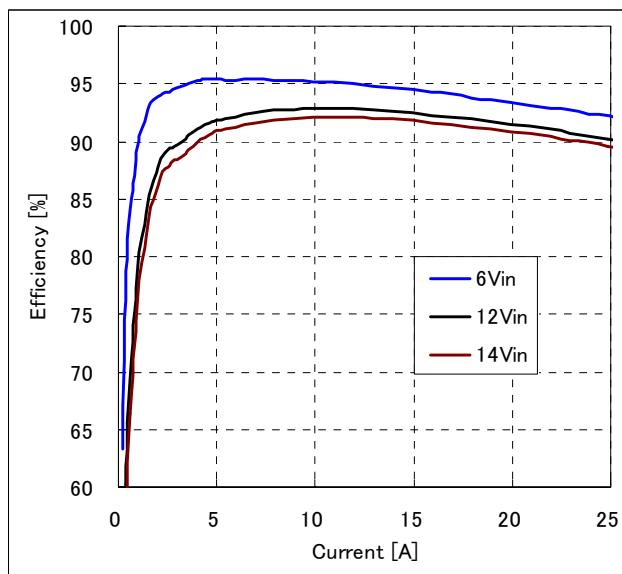


Fig-2.5V-2: Efficiency vs. load current and input voltage for Vout=2.5V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

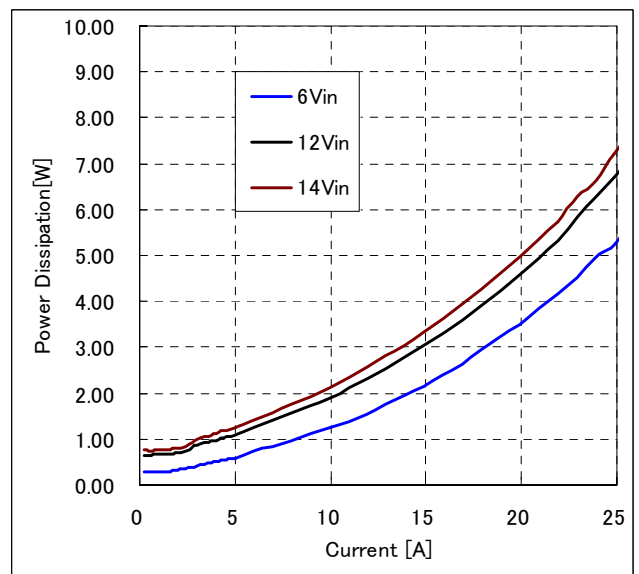


Fig-2.5V-3: Power Loss vs. load current and input voltage for Vout=2.5V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

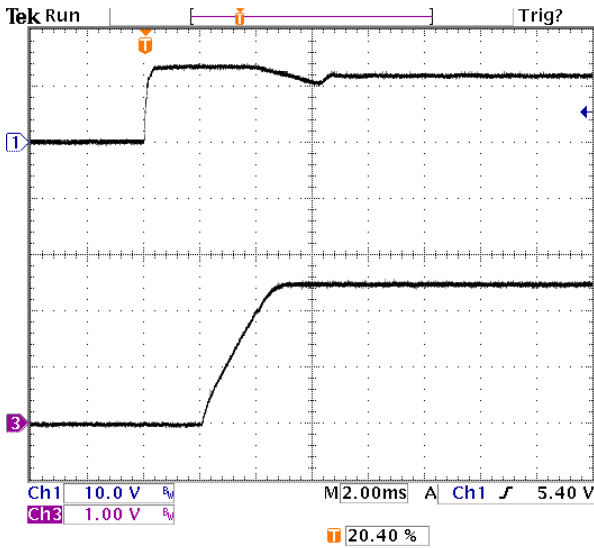


Fig-2.5V-4: Turn-on transient for $V_{out}=2.5V$ with application of V_{in} at full rated load current (resistive) and 47uFx4 external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)
 Time scale: 2 ms/div.

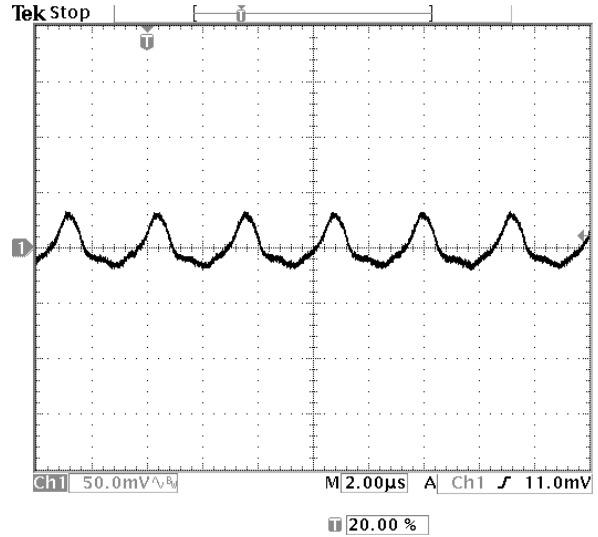


Fig-2.5V-5: Output voltage ripple (50mV/div.) for $V_{out}=2.5V$ at full rated load current into a resistive load with external capacitance 47uFx4 ceramic + 1uF ceramic at $V_{in}=12V$.
 Time scale: 2 us/div

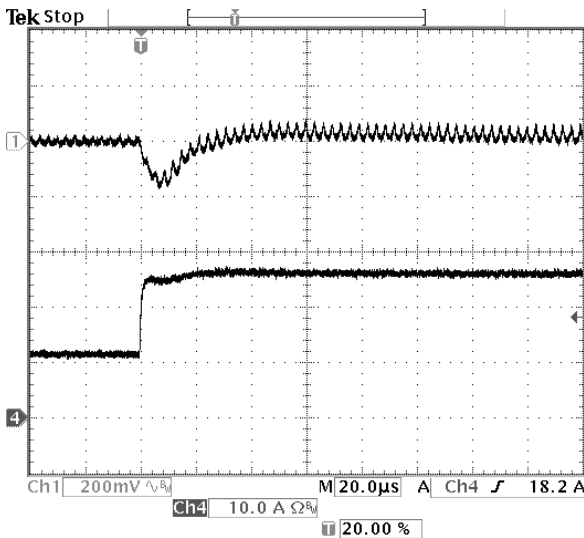


Fig-2.5V-6: Output voltage response for $V_{out}=2.5V$ to positive load current step change from 12.5A to 25A with slew rate of 5A/us at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

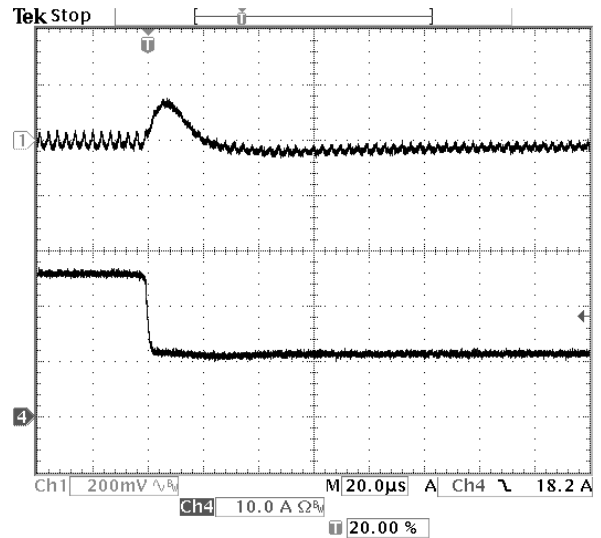


Fig-2.5V-7: Output voltage response for $V_{out}=2.5V$ to negative load current step change from 25A to 12.5A with slew rate of -5A/us at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

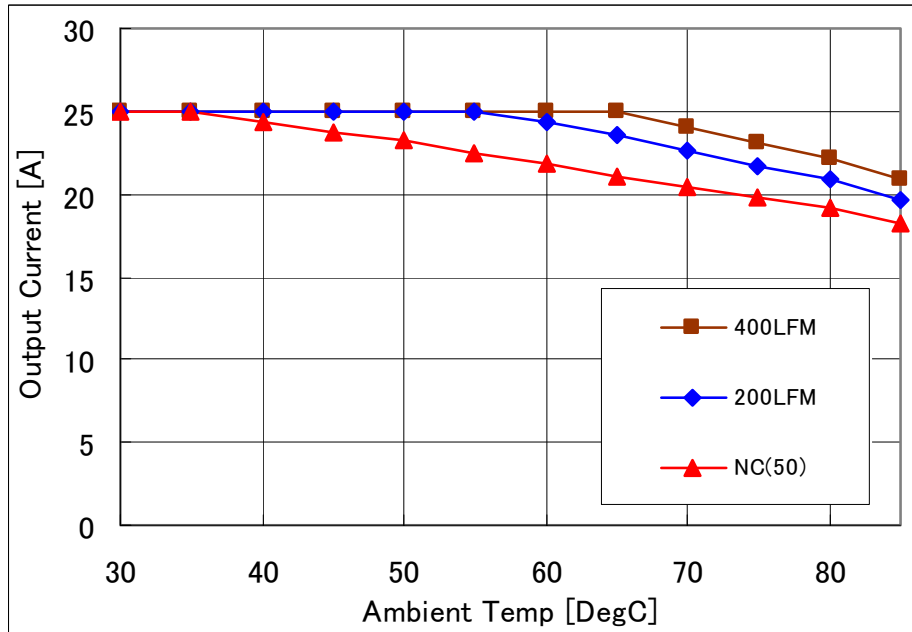


Fig-2.0V-1: Available load current vs. ambient temperature and airflow rates for Vout=2.0V with Vin=12V. Maximum component temperature ≤ 120°C

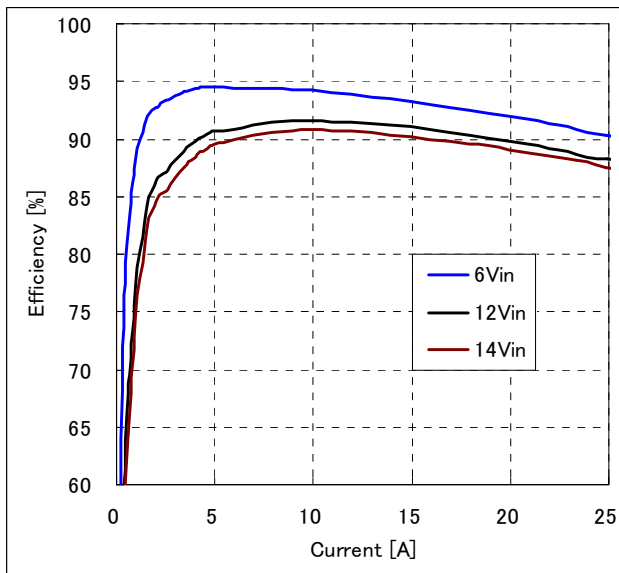


Fig-2.0V-2: Efficiency vs. load current and input voltage for Vout=2.0V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

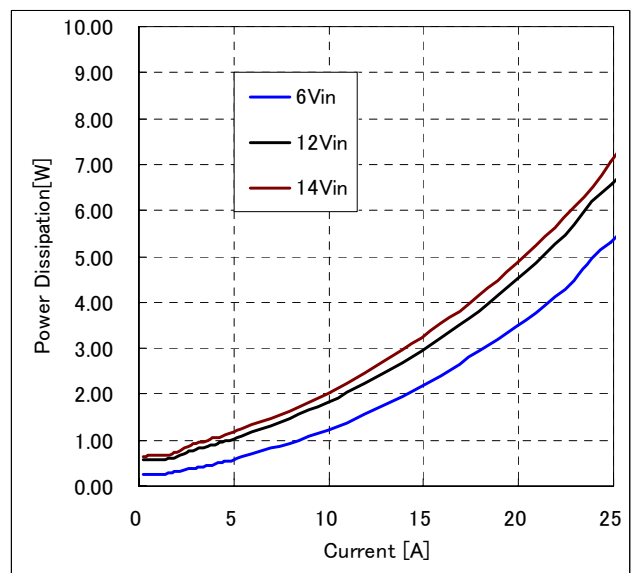


Fig-2.0V-3: Power Loss vs. load current and input voltage for Vout=2.0V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

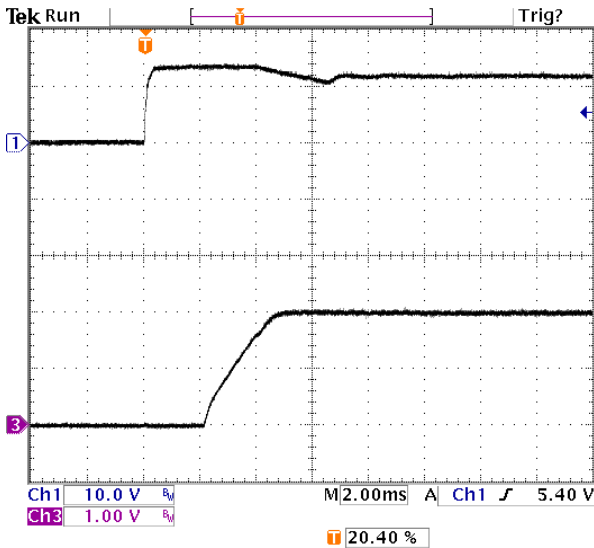


Fig-2.0V-4: Turn-on transient for $V_{out}=2.0V$ with application of V_{in} at full rated load current (resistive) and $47\mu F \times 4$ external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)
 Time scale: 2 ms/div.

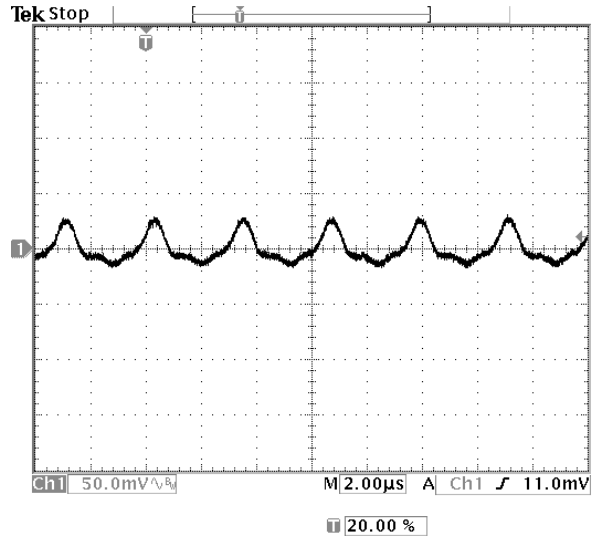


Fig-2.0V-5: Output voltage ripple (50mV/div.) for $V_{out}=2.0V$ at full rated load current into a resistive load with external capacitance $47\mu F \times 4$ ceramic + $1\mu F$ ceramic at $V_{in}=12V$.
 Time scale: 2 us/div

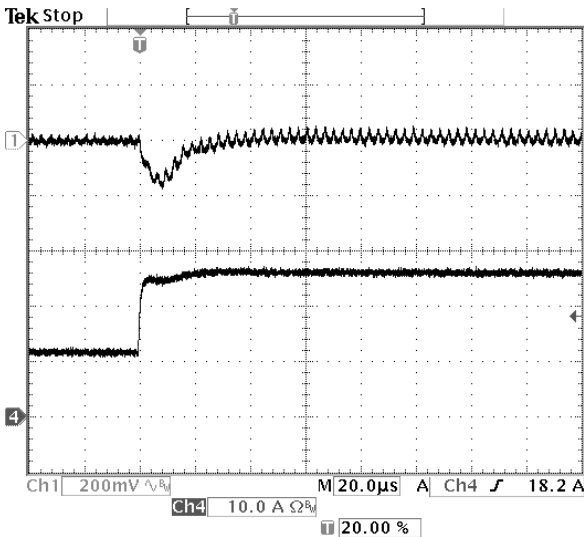


Fig-2.0V-6: Output voltage response for $V_{out}=2.0V$ to positive load current step change from 12.5A to 25A with slew rate of 5A/us at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

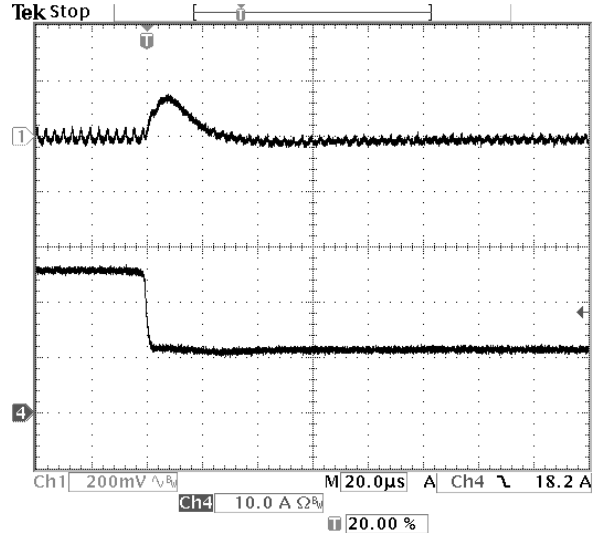


Fig-2.0V-7: Output voltage response for $V_{out}=2.0V$ to negative load current step change from 25A to 12.5A with slew rate of -5A/us at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

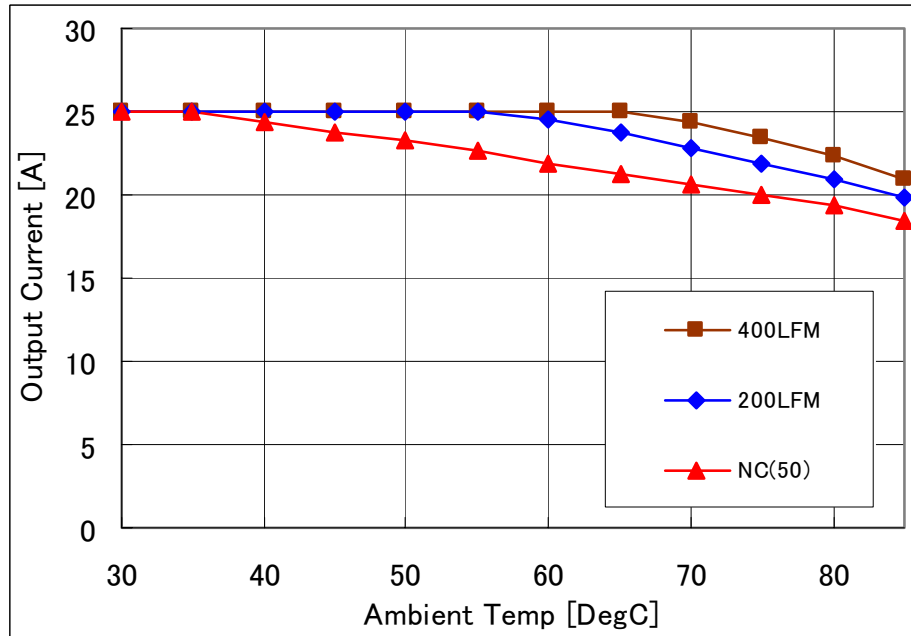


Fig-1.8V-1: Available load current vs. ambient temperature and airflow rates for $V_{out}=1.8V$ with $V_{in}=12V$. Maximum component temperature $\leq 120^{\circ}C$

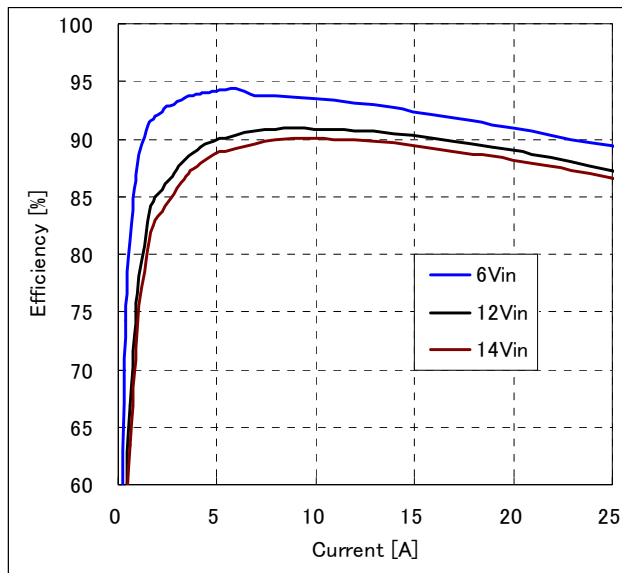


Fig-1.8V-2: Efficiency vs. load current and input voltage for $V_{out}=1.8V$. Airflow rate=200 LFM (1m/s) and $T_a=25^{\circ}C$.

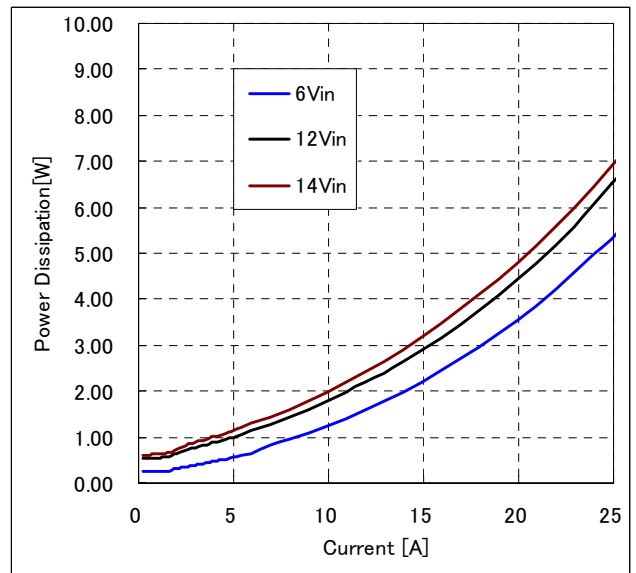


Fig-1.8V-3: Power Loss vs. load current and input voltage for $V_{out}=1.8V$. Airflow rate=200 LFM (1.0 m/s) and $T_a=25^{\circ}C$.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

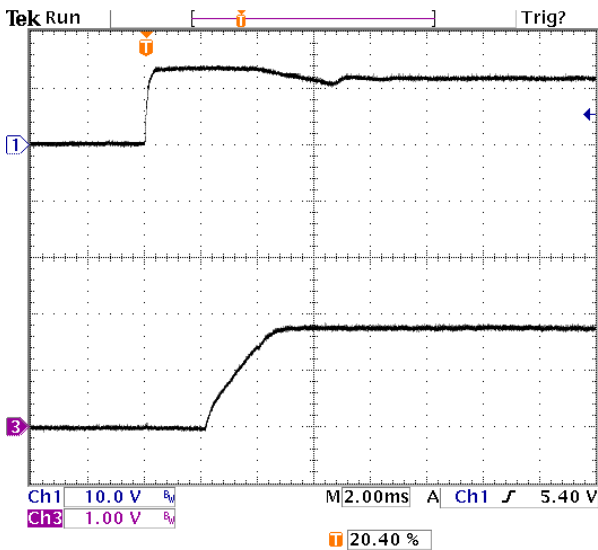


Fig-1.8V-4: Turn-on transient for $V_{out}=1.8V$ with application of V_{in} at full rated load current (resistive) and $47\mu F \times 4$ external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)
 Time scale: 2 ms/div.

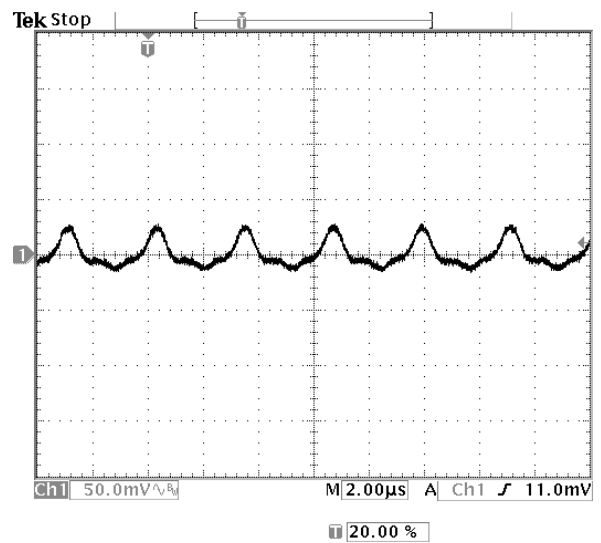


Fig-1.8V-5: Output voltage ripple (50mV/div.) for $V_{out}=1.8V$ at full rated load current into a resistive load with external capacitance $47\mu F \times 4$ ceramic + $1\mu F$ ceramic at $V_{in}=12V$.
 Time scale: 2 us/div

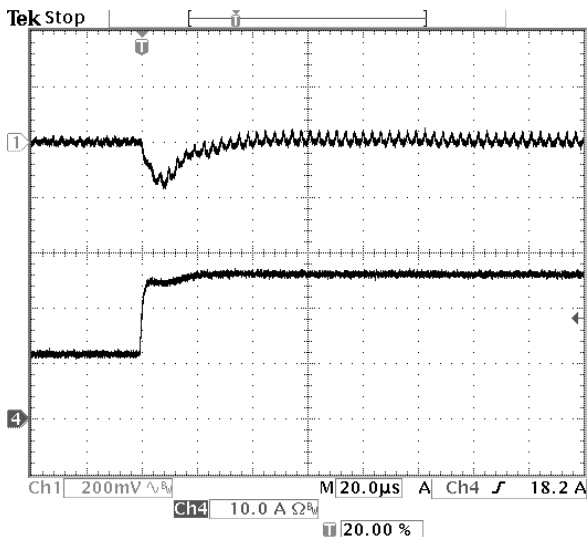


Fig-1.8V-6: Output voltage response for $V_{out}=1.8V$ to positive load current step change from 12.5A to 25A with slew rate of $5A/\mu s$ at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

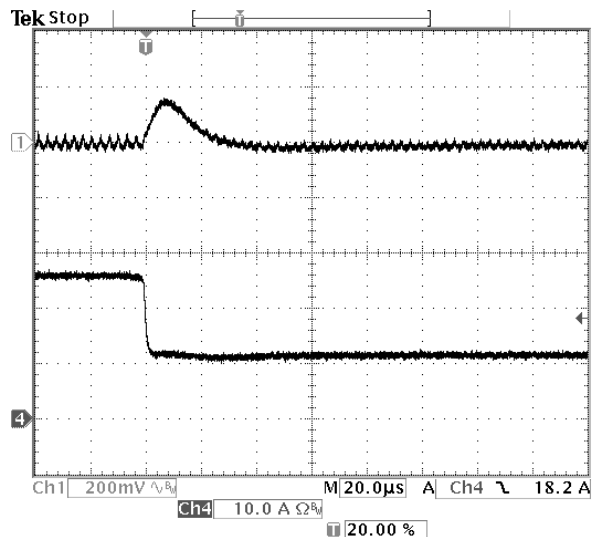


Fig-1.8V-7: Output voltage response for $V_{out}=1.8V$ to negative load current step change from 25A to 12.5A with slew rate of $-5A/\mu s$ at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

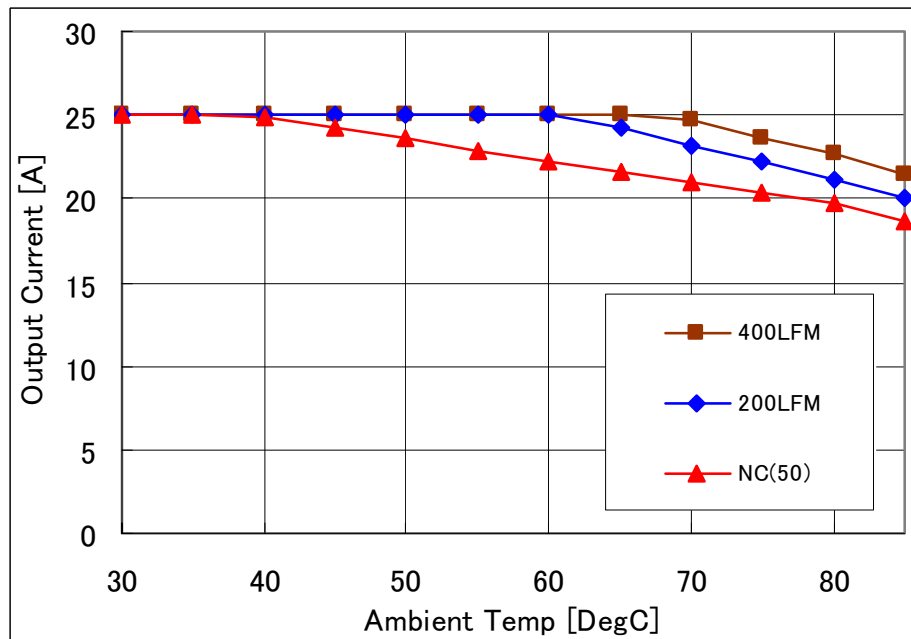


Fig-1.5V-1: Available load current vs. ambient temperature and airflow rates for Vout=1.5V with Vin=12V. Maximum component temperature ≤ 120°C

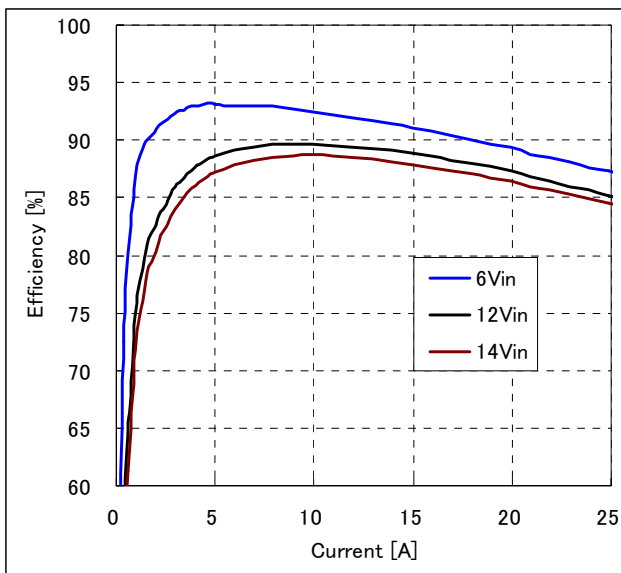


Fig-1.5V-2: Efficiency vs. load current and input voltage for Vout=1.5V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

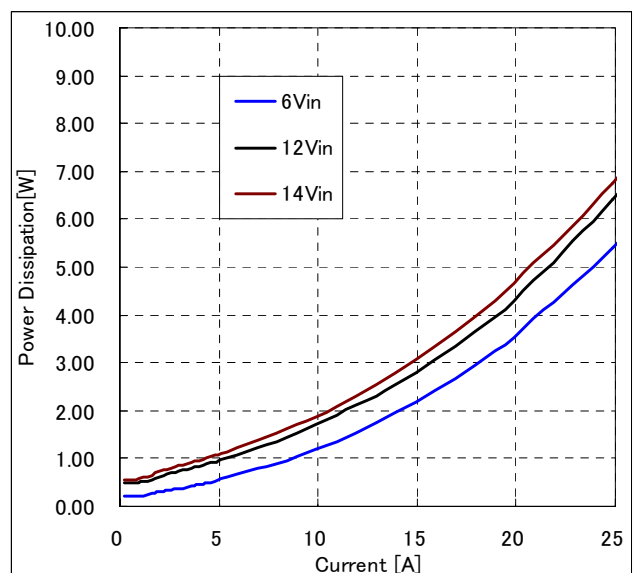


Fig-1.5V-3: Power Loss vs. load current and input voltage for Vout=1.5V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

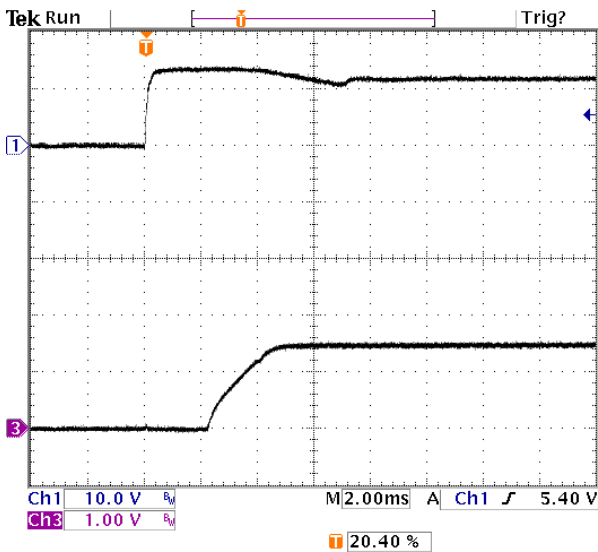


Fig-1.5V-4: Turn-on transient for $V_{out}=1.5V$ with application of V_{in} at full rated load current (resistive) and $47\mu F \times 4$ external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)
 Time scale: 2 ms/div.

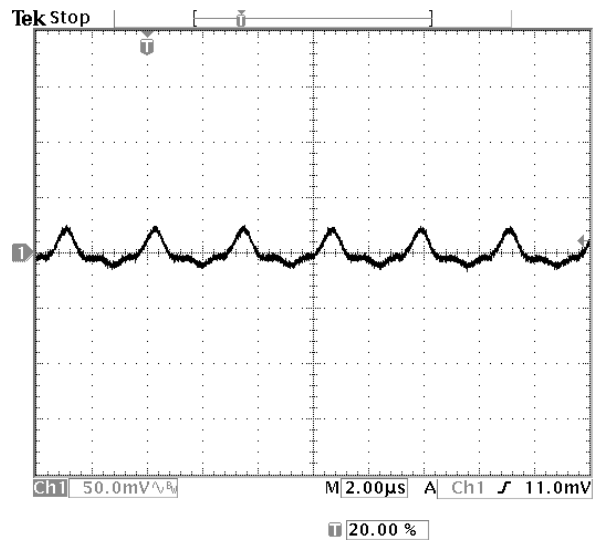


Fig-1.5V-5: Output voltage ripple (50mV/div.) for $V_{out}=1.5V$ at full rated load current into a resistive load with external capacitance $47\mu F \times 4$ ceramic + $1\mu F$ ceramic at $V_{in}=12.0V$.
 Time scale: 2us/div

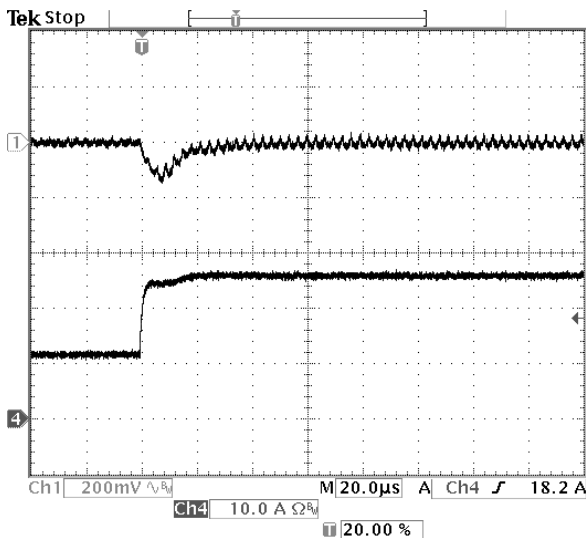


Fig-1.5V-6: Output voltage response for $V_{out}=1.5V$ to positive load current step change from 12.5A to 25A with slew rate of $5A/\mu s$ at $V_{in}=12V$. $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

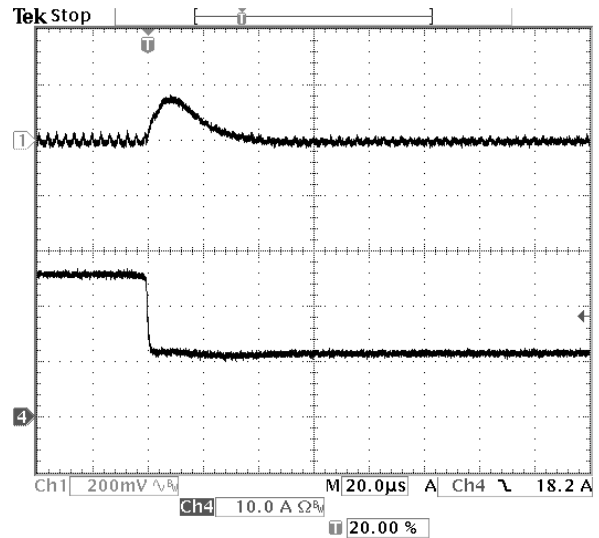


Fig-1.5V-7: Output voltage response for $V_{out}=1.5V$ to negative load current step change from 25A to 12.5A with slew rate of $-5A/\mu s$ at $V_{in}=12V$. $C_o=47\mu F \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

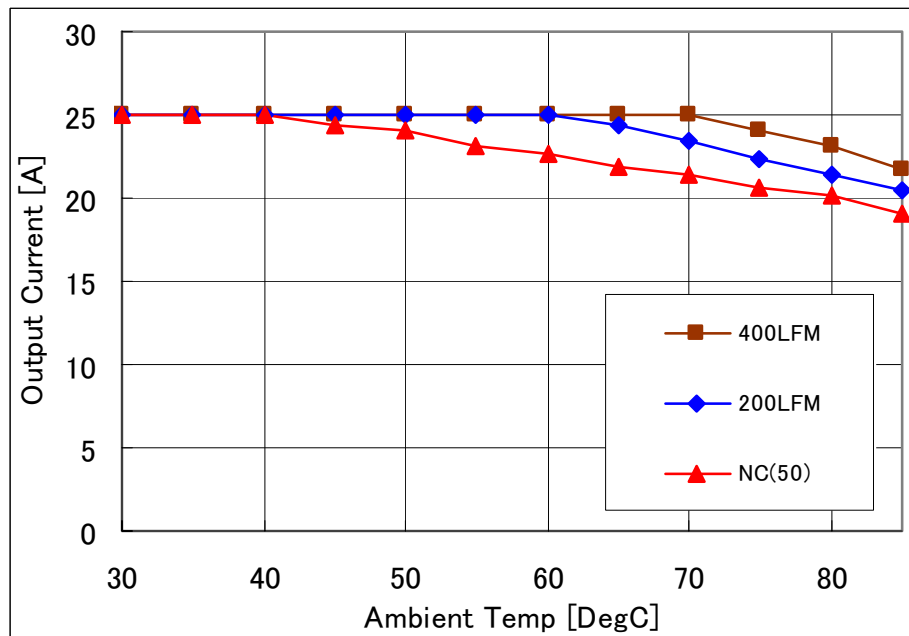


Fig-1.2V-1: Available load current vs. ambient temperature and airflow rates for Vout=1.2V with Vin=12V. Maximum component temperature $\leq 120^{\circ}\text{C}$

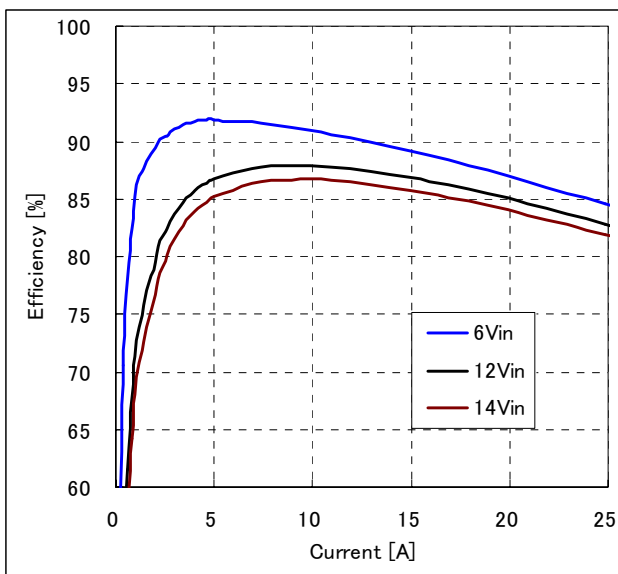


Fig-1.2V-2: Efficiency vs. load current and input voltage for Vout=1.2V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

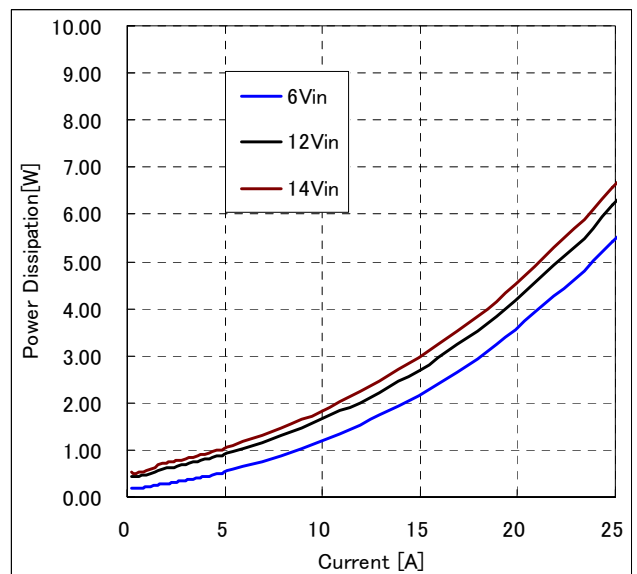


Fig-1.2V-3: Power Loss vs. load current and input voltage for Vout=1.2V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

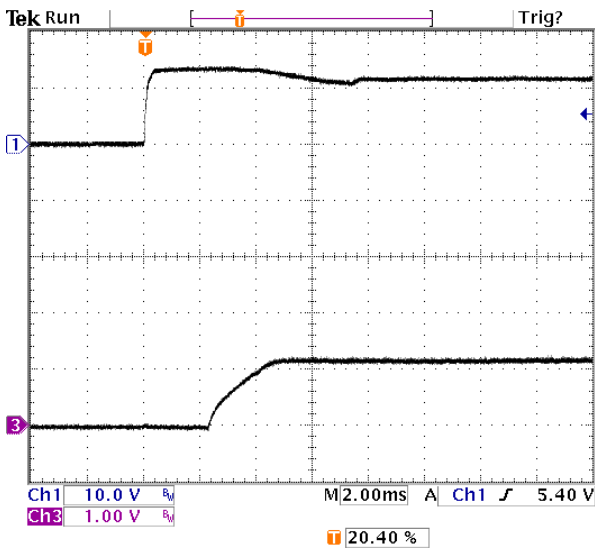


Fig-1.2V-4: Turn-on transient for $V_{out}=1.2V$ with application of V_{in} at full rated load current (resistive) and $47\mu F \times 4$ external capacitance at $V_{in}=12V$.
Top trace: V_{in} (10V/div.)
Bottom trace: output voltage (1V/div.)
Time scale: 2ms/div.

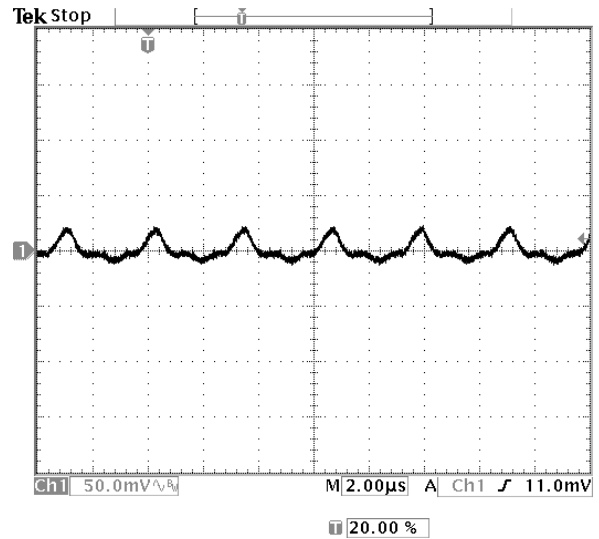


Fig-1.2V-5: Output voltage ripple (50mV/div.) for $V_{out}=1.2V$ at full rated load current into a resistive load with external capacitance $47\mu F \times 4$ ceramic + $1\mu F$ ceramic at $V_{in}=12V$.
Time scale: 2us/div

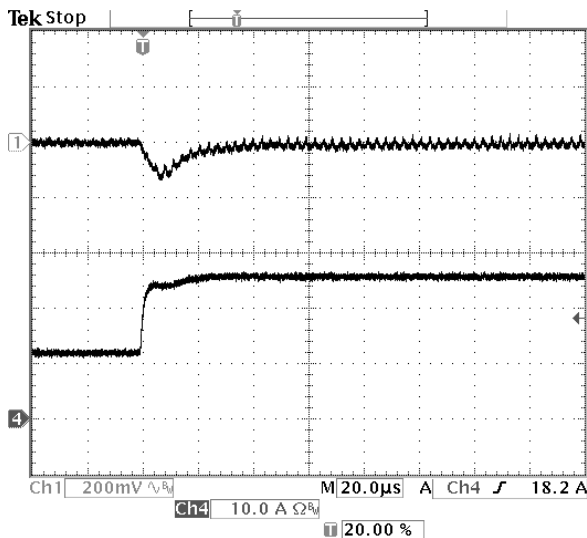


Fig-1.2V-6: Output voltage response for $V_{out}=1.2V$ to positive load current step change from 12.5A to 25A with slew rate of 5A/us at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
Top trace: output voltage (200mV/div.)
Bottom trace: load current (10A/div.)
Time scale: 20us/div.

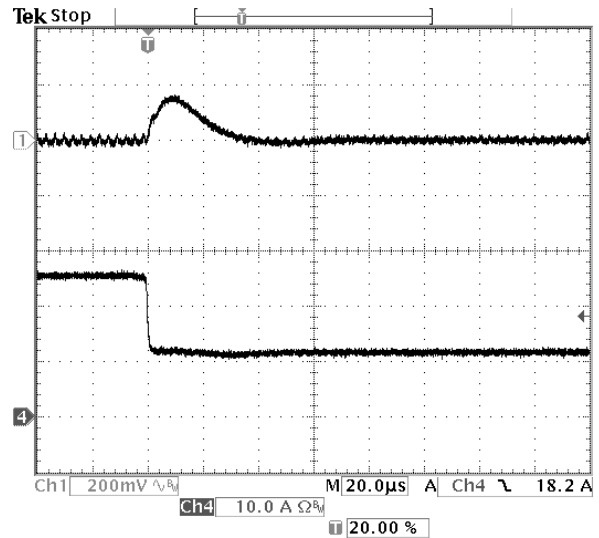


Fig-1.2V-7: Output voltage response for $V_{out}=1.2V$ to negative load current step change from 25A to 12.5A with slew rate of -5A/us at $V_{in}=12V$.
 $C_o=47\mu F \times 4$ ceramic.
Top trace: output voltage (200mV/div.)
Bottom trace: load current (10A/div.)
Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

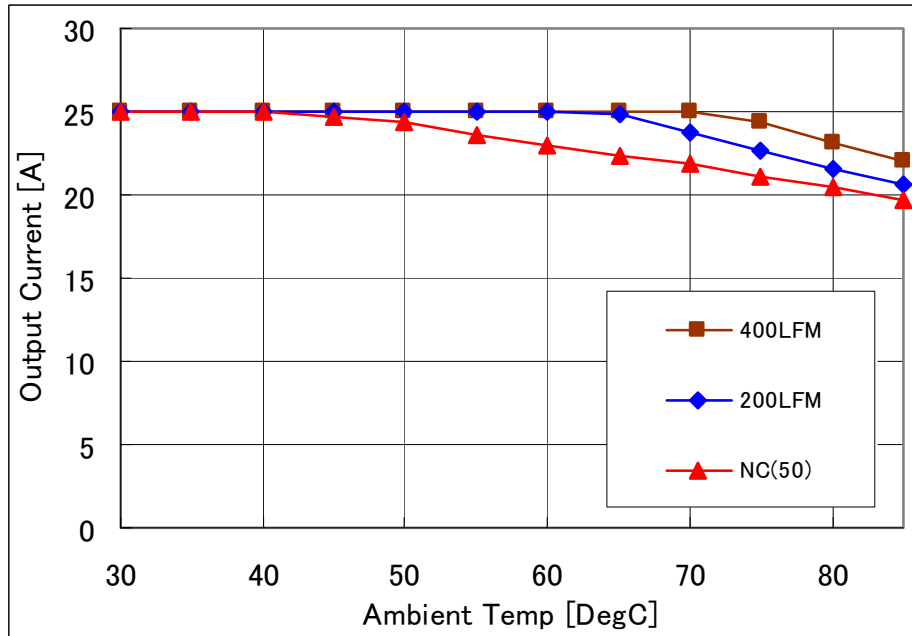


Fig-1.0V-1: Available load current vs. ambient temperature and airflow rates for Vout=1.0V with Vin=12V. Maximum component temperature $\leq 120^{\circ}\text{C}$

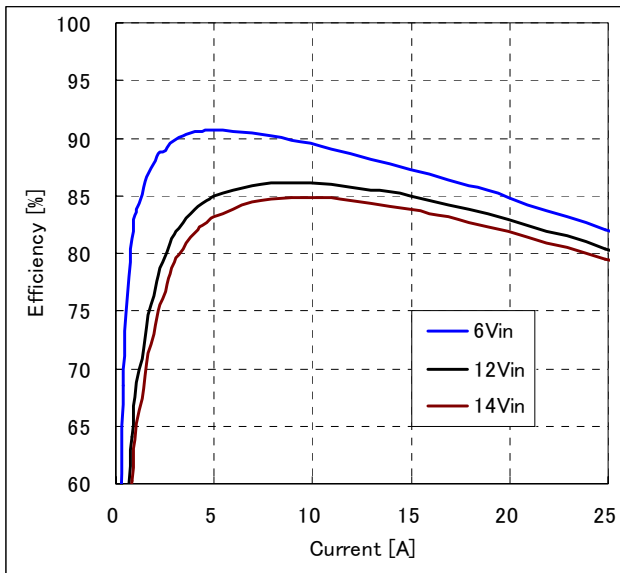


Fig-1.0V-2: Efficiency vs. load current and input voltage for Vout=1.0V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

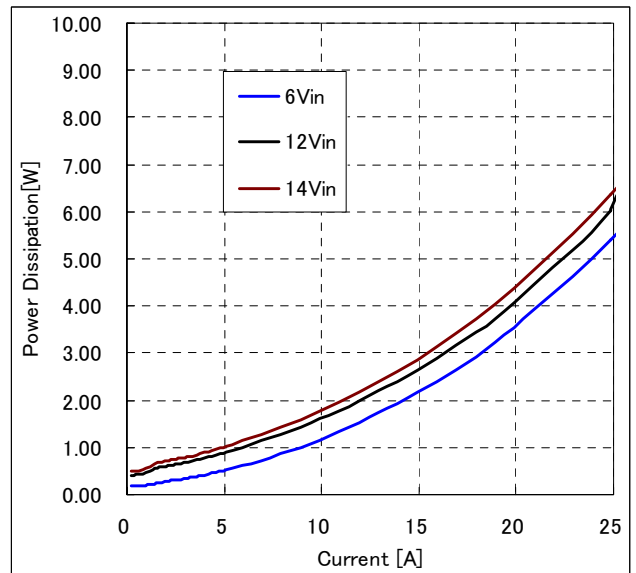


Fig-1.0V-3: Power Loss vs. load current and input voltage for Vout=1.0V. Airflow rate=200 LFM (1m/s) and Ta=25°C.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

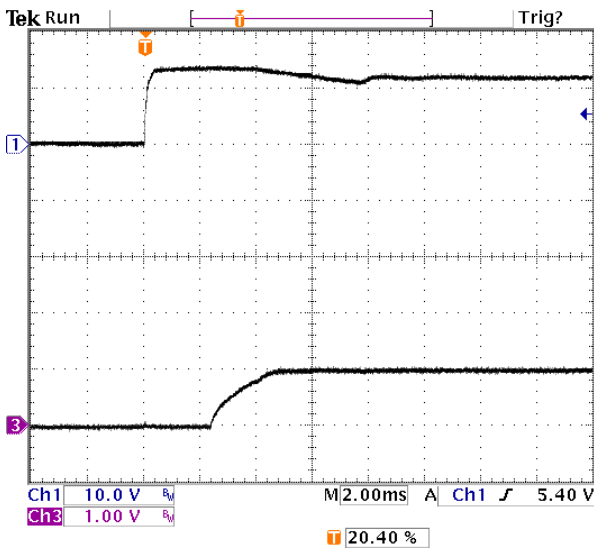


Fig-1.0V-4: Turn-on transient for $V_{out}=1.0V$ with application of V_{in} at full rated load current (resistive) and 47uF \times 4 external capacitance at $V_{in}=12V$.
 Top trace: V_{in} (10V/div.)
 Bottom trace: output voltage (1V/div.)
 Time scale: 2 ms/div.

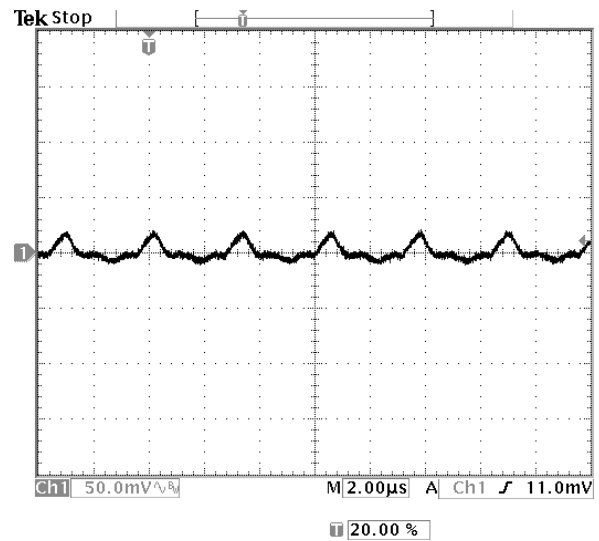


Fig-1.0V-5: Output voltage ripple (50mV/div.) for $V_{out}=1.0V$ at full rated load current into a resistive load with external capacitance 47uF \times 4 ceramic + 1uF ceramic at $V_{in}=12V$.
 Time scale: 2 us/div

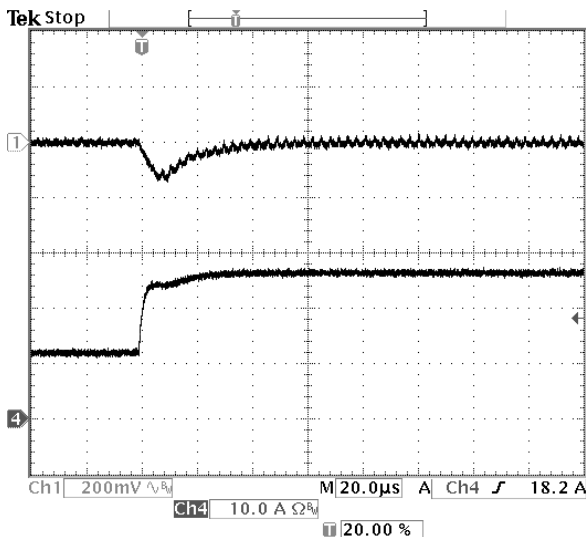


Fig-1.0V-6: Output voltage response for $V_{out}=1.0V$ to positive load current step change from 12.5A to 25A with slew rate of 5A/us at $V_{in}=12V$.
 $C_o=47uF \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

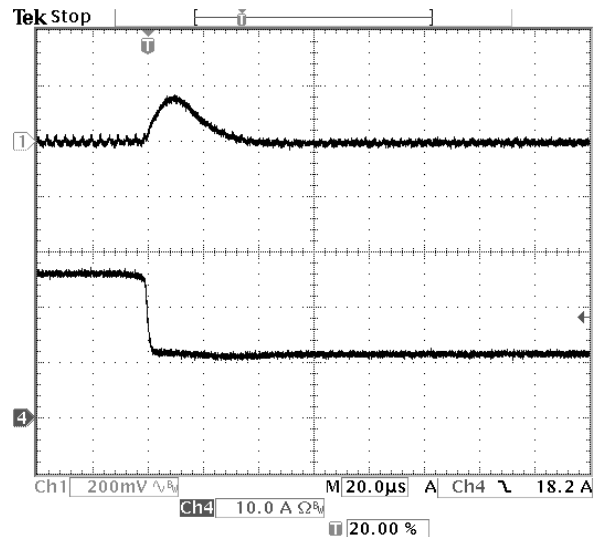
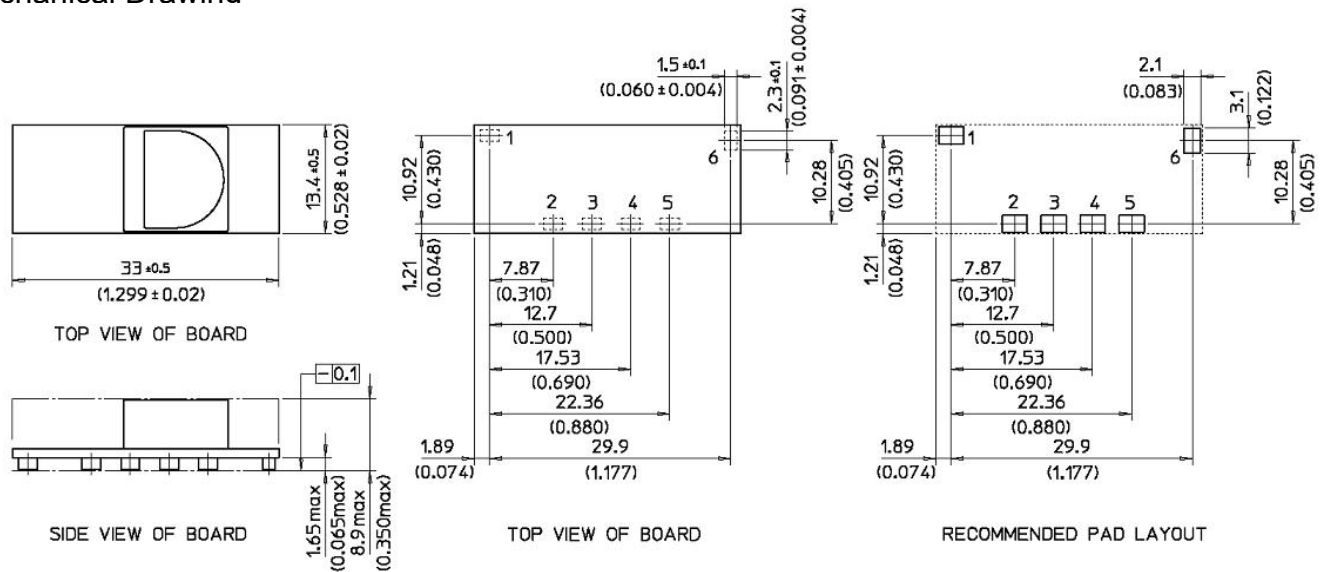


Fig-1.0V-7: Output voltage response for $V_{out}=1.0V$ to negative load current step change from 25A to 12.5A with slew rate of -5A/us at $V_{in}=12V$.
 $C_o=47uF \times 4$ ceramic.
 Top trace: output voltage (200mV/div.)
 Bottom trace: load current (10A/div.)
 Time scale: 20us/div.

FPLR12SR7525*A

6-14Vdc Input, 25A, 0.7525-5.5Vdc Output

Mechanical Drawing



Pin Connections	
Pin #	Function
1	Vin
2	GND
3	Vout
4	TRIM
5	SENSE
6	ON/OFF

Notes

- All dimensions are in millimeters (inches)
- Unless otherwise specified, tolerances are +/- 0.25mm
- Connector material: Copper
- Connector finish: Gold over Nickel
- Converter weight: 0.247oz (7.0g)
- Converter height: 8.90mm Max
- Recommended surface-mount pads: 2.1 x 3.1mm

Part Numbering Scheme

Product Series	Shape	Regulated/ Non	Input Voltage	Mounting Scheme	Output Voltage	Rated Current	ON/OFF Logic	Pin Shape
FP	L	R	12	S	R75	25	*	A
Series Name	Large	R: Regulated	Typ=12V	Surface Mount	0.75V (Programmable: See page 6)	25A	N: Negative P: Positive	Standard

Cautions

NUCLEAR AND MEDICAL APPLICATIONS: FDK Corporation products are not authorized for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems without the written consent of FDK Corporation.

SPECIFICATION CHANGES AND REVISIONS: Specifications are version-controlled, but are subject to change without notice.