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Overview of Xilinx JTAG Programming Cables and Reference Schematics for Legacy Parallel Cable III (PC3)

Summary

This technical publication provides an overview of Xilinx JTAG Cables and a reference schematic for the legacy Xilinx Parallel Cable III product (PC3) for educational use.

Description

Xilinx offers the Hi-Speed Platform Cable USB (PCUSB) and the Parallel Cable IV (PC4) cables. The PC4 cable supports both the IEEE 1284 parallel port interface and IEEE STD 1149.1 (JTAG) standards for in-system programming or embedded debug. These cables are more thoroughly described in the "Overview of Xilinx JTAG Solutions."

For reference purposes, the PC3 product schematic is also provided in this document.

Note: The PC3 cable product has been discontinued and replaced by PCUSB and PC4. Both the PCUSB and PC4 cables have expanded capabilities, superior download performance, and robust immunity to system interface sensitivities when compared to the legacy PC3 cable.

The PC3 product was first introduced in 1998 and then discontinued in 2002. Software support for PC3 was removed starting in March 2008 with the 10.1 release of Xilinx iMPACT software. Versions of iMPACT software after 10.1 release do *not* support the PC3 cable. See "Notice of Disclaimer" regarding warranty and support of the PC3 schematic information.

Overview of Xilinx JTAG Solutions

Xilinx recommends the Platform Cable USB (PCUSB) or Parallel Cable IV (PC4) for new designs. The PCUSB and PC4 offer reliable operation, higher speed download, voltage support down to 1.5V, keyed ribbon cable connector for error-free insertion, and improved ground/signal integrity. The PC4 operates, by default, in a PC3-compatibility mode for use with applications designed for the PC3. The PCUSB and PC4 can be used with ISE™ Foundation™ software, Platform Studio EDK, and ChipScope™ Pro analyzer.

- **Platform Cable USB:**

  Platform Cable USB is a high-performance, RoHS-compliant, download cable attaching to user hardware for the purpose of programming or configuring any of the following Xilinx devices:

  • ISP Configuration PROMs

  • CPLDs

  • FPGAs

  Platform Cable USB attaches to the USB port on a desktop or laptop PC with an off-the-shelf Hi-Speed USB A-B cable. It derives all operating power from the hub port controller. No external power supply is required.

  Device configuration and programming operations using Platform Cable USB are supported by iMPACT download software using Boundary-Scan (IEEE 1149.1 / IEEE 1532), slave-serial mode, or serial peripheral interface (SPI). Target clock speeds are selectable from 750 kHz to 24 MHz.

  Platform Cable USB attaches to target systems using a 14-conductor ribbon cable designed for high-bandwidth data transfers. An optional adapter that allows attachment of a flying lead set is included for backward compatibility with target systems that do not use the ribbon cable connector.

Note: Xilinx download cables are for prototyping only and should not be used as a production programming solution.

For more details, refer to:

http://www.xilinx.com/products/devkits/HW-USB-G.htm

- **Parallel Cable IV:**

  The Xilinx Parallel Cable IV (PC4) is a high-speed download cable that configures or programs all Xilinx FPGAs, CPLDs, and ISP PROMs. The cable takes advantage of the IEEE 1284 ECP protocol and Xilinx iMPACT software to achieve download speeds that are over 10 times faster than the PC3. The cable automatically senses and adapts to target I/O voltages and is able to accommodate a wide range of I/O standards from 1.5V to 5V.

  PC4 supports the widely used industry standard IEEE 1149.1 Boundary Scan (JTAG) specification using a four-wire interface. It also supports the Xilinx Slave Serial mode for Xilinx FPGA devices. It interfaces to target systems using a ribbon cable that features integral alternating ground leads to reduce noise and increase signal integrity.

  The cable is externally powered from either a power brick or by interfacing to a standard PC mouse or keyboard connection. A bi-color status LED indicates the presence of operating and target reference voltages.

  Note: The PC4 is not available in a RoHS-compliant version. Moreover, Xilinx download cables are for prototyping only and should not be used as a production programming solution.

  For more details, refer to:

  http://www.xilinx.com/products/devkits/HW-PC4.htm

PC3-Based Reference Schematic

The Parallel Cable III (also known as the PC3) schematic provides an example cable design for educational use only. The PC3 schematic is not recommended for new designs and customers are instead encouraged to use the complete Platform Cable USB (PCUSB) and Parallel Cable IV (PC4) products as outline in "Overview of Xilinx JTAG Solutions."

Note: Xilinx does not provide schematics for the PCUSB or PC4 products.

While the PC3 cable is no longer a supported product, Xilinx is continuing to provide schematics for the PC3 cable via this technical publication for reference use by the Xilinx development and education communities. The schematic has been used in the past for development of embedded systems and application specific solutions to create custom solutions outside of the iMPACT environment. The PC3-based schematic in this technical publication provides a simple model of connectivity between a Microsoft Windows based personal computer and an in-system programmable (ISP) device.

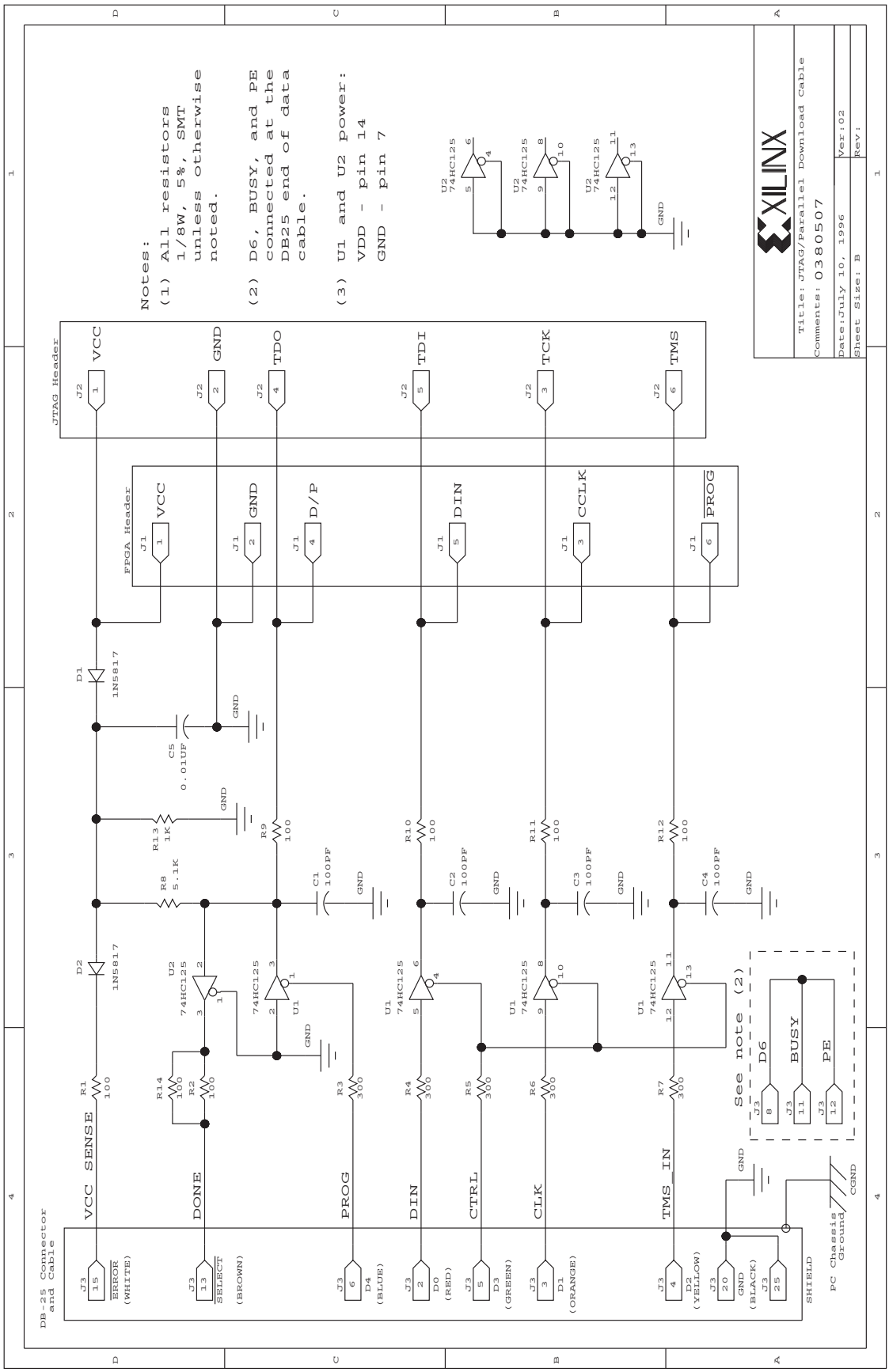
The PC3 schematic demonstrates support for two interfaces to target devices. The first interface is an IEEE STD 1149.1 (JTAG) interface which can connect to the JTAG port of a CPLD, ISP PROM, or FPGA. The second interface is a connection to the slave-serial port of an FPGA.

Note: IMPACT software no longer supports this PC3 Cable schematic after release 10.1.

The original PC3 cable (using the schematic provided in "Schematic") consisted of a cable assembly containing logic to protect the host PC's parallel port and a set of headers to connect to the target system. Also, the PC3 schematic typically requires a PC equipped with an AT compatible parallel port interface with a DB25 standard printer connector. When combined with appropriate software, the PC3 schematic enables development of systems that can download to a single device or several devices connected in either a Boundary-Scan chain or a slave-serial daisy chain (FPGA only). The PC3 schematic could also be used to develop systems that provide read back configuration and Boundary-Scan data.

Note: The transmission speed of systems developed using the PC3 schematic is determined solely by the speed at which the host PC can transmit data through its parallel port interface. Based upon typical experience, the resulting average JTAG TCK frequency is typically 100 to 300 kHz.

Schematic


Notes:
(1) All resistors 1/8W, 5%, SMT unless otherwise noted.
(2) D6, BUSY, and PE connected at the DB25 end of data cable.
(3) U1 and U2 power: VDD - pin 14 GND - pin 7
XILINX
Title: JTAG/Parallel Download Cable
Comments: 0380507
Date: July 10, 1996
Ver: 02
Sheet Size: B
Rev:
JTAG Header
FPGA Header
VCC
GND
TDO
TDI
TCK
TMS
D/P
DIN
CCLK
PROG
See note (2)
D6
BUSY
PE
DB-25 Connector and Cable
VCC SENSE
DONE
PROG
DIN
CTRL
CLK
TMS_IN
SHIELD
PC Chassis Ground
CGND
SELECT
ERROR
D0
D1
D2
D3
D4

Cable Connections to JTAG Chain

Table 1: **Parallel Cable Connections and Definitions for JTAG**

Name	Function	Connections
VCC	**Power**. Supplies V_{CC} (5V, or 3.3V; 10 mA, typically) to the cable. The V_{CC} supply level must match the I/O voltage level for all devices in the JTAG chain for best signal integrity.	To target system V_{CC}.
GND	**Ground.** Supplies ground reference to the cable.	To target system ground.
TCK	**Test Clock.** This clock drives the test logic for all devices on boundary-scan chain.	Connect to system TCK pin (the TCK pins of all devices in the JTAG chain).
TDO	**Test Data Out.** Read back data from the target system is read at this pin.	Connect to system TDO pin (the TDO pin of the last device in the JTAG chain).
TDI	**Test Data In.** This signal is used to transmit serial test instructions and data.	Connect to system TDI pin (the TDI pin of the first device in the JTAG chain).
TMS	**Test Mode Select**.This signal is decoded by the JTAG test access port (TAP) controller to control test operations.	Connect to system TMS pin (the TMS pins of all devices in the JTAG chain).

Cable Connections to Slave Serial Port

Table 2: **Parallel Cable Connections and Definitions for Slave Serial Mode**

Name	Function	Connections
VCC	**Power**. Supplies V_{CC} (5V, or 3.3V; 10 mA, typically) to the cable. The V_{CC} supply level must match the I/O voltage level of the FPGA slave-serial configuration pins for best signal integrity.	To target system V_{CC}.
GND	**Ground.** Supplies ground reference to the cable.	To target system ground.
CCLK	**Configuration Clock**. This signal supplies the clock for the slave-serial configuration sequence.	Connect to FPGA CCLK pin.
DONE (D/P)	**Done/Program**. Enables the host application to detect when configuration loading is complete, and that the start-up sequence is in progress.	Connect to FPGA DONE pin.
DIN	**Data In**. Provides configuration data to target system during configuration and is 3-stated at all other times.	Connect to FPGA DIN, or equivalent, pin.
PROG	**Program**. A Low indicates the device is clearing its configuration memory. This active-Low signal is used to initiate the configuration process.	Connect to FPGA PROG_B pin.

Additional Resources

For a complete listing of all current documentation covering configuration hardware, refer to:

http://www.xilinx.com/support/documentation/configuration_hardware.htm

For a listing of Xilinx documentation covering Boundary-Scan and JTAG, refer to:

http://www.xilinx.com/support/documentation/boundary_scan_and_jtag.htm

For an extensive collection of Xilinx and third-party Automatic Test Equipment (ATE) and Boundary-Scan (JTAG) resources, refer to:

http://www.xilinx.com/products/design_resources/config_sol/resource/isp_ate.htm

For details on JTAG probing tools, refer to:

http://www.xilinx.com/products/design_resources/design_tool/grouping/jtag_probes.htm

For a quick JTAG checklist, refer to:

XAPP104, *A Quick JTAG ISP Checklist*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/28/08	1.0	Initial Xilinx release.

Notice of Disclaimer