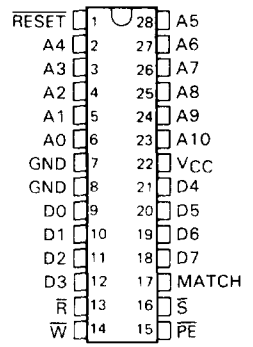
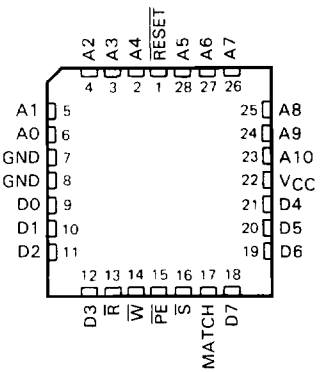
D3156, DECEMBER 1988—REVISED MARCH 1990

- **Fast Address to Match Delay 20 or 25 ns Max**
- **Common I/O with Read Feature**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generator and Checking**
- **Parity Error Output, Force Parity Error Input**
- **Easily Expandable**
- **Choice of Open-Drain or Totem-Pole MATCH Output**
- **EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process**
- **Fully TTL-Compatible**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2152A and 'ACT2154A cache address comparators consist of a high-speed 2K × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2152A has a totem-pole MATCH output while the 'ACT2154A has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the data D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

EPIC is a trademark of Texas Instruments Incorporated.
These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

A read mode is provided with the 'ACT2152A and 'ACT2154A, which allows the contents of RAM to be read at the D0-D7 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low, and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

These cache address comparators operate from a single +5-V supply and are offered in 28-pin plastic 600-mil ceramic side brazed, dual-in-line and PLCC packages.

The 'ACT2152A and 'ACT2154A are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A10] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}
or: $\overline{R}$ = V_{IL}

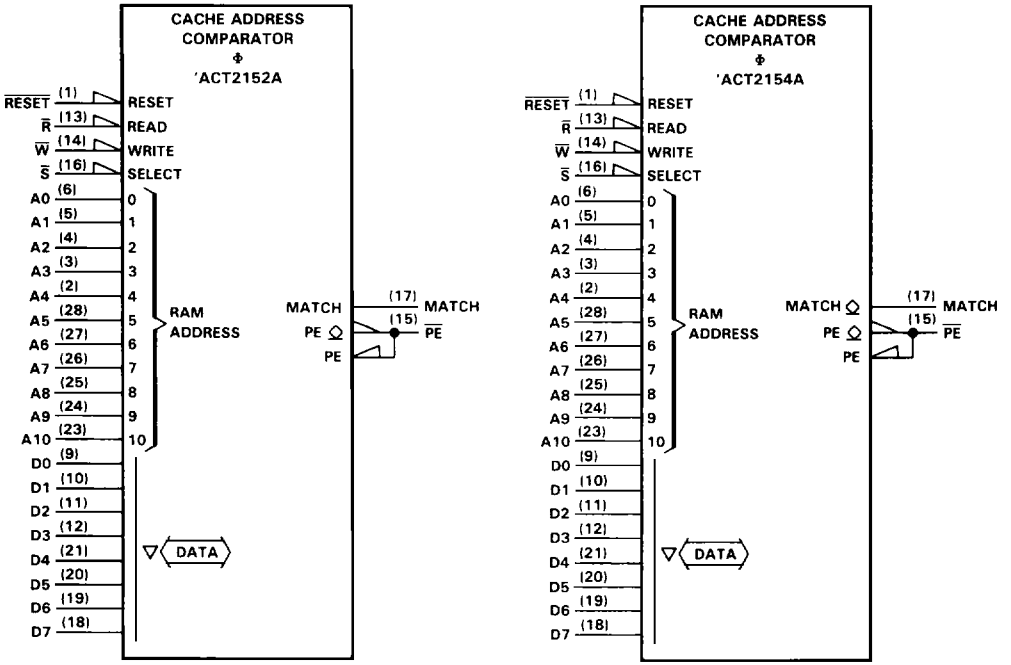
MATCH = V_{OL} if: [A0-A10] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS				OUTPUTS		I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	D0-D7	
H	L	L	H	H	H	Output	Read
H	H	L	H	L	L	Input	Parity error
				L	H		Not equal
				H	L		Undefined error
				H	H		Equal
L	X	L	H	H	IN	Input	Write
X	X	H	H	H	H	Hi-Z	Device disabled
X	X	X	L	H	†	†	Memory reset

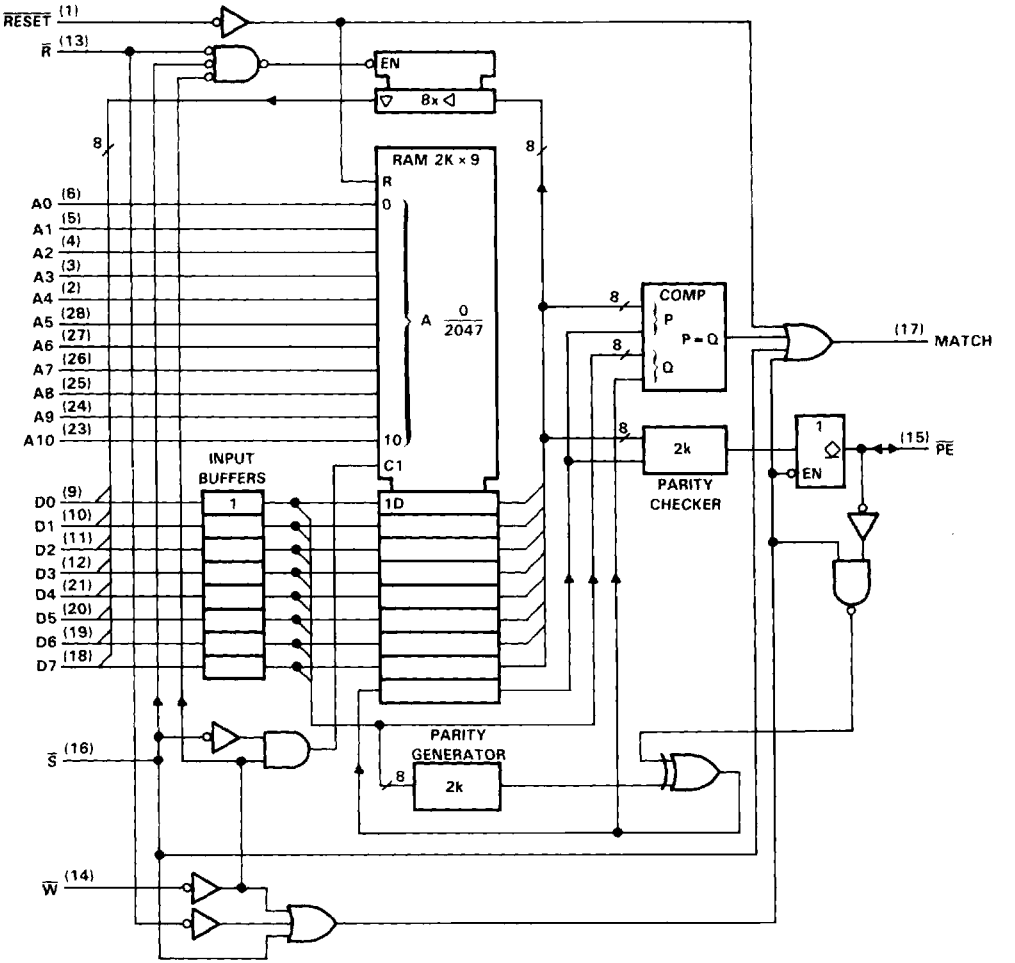
†The state of these pins is dependent on inputs $\overline{W}$, $\overline{R}$, and $\overline{S}$.

logic symbol†



†These symbols are in accordance with ANSI/IEEE Std 91-1984.

functional block diagram (positive logic)



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TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	6	Address inputs. Addresses 1 of 2048 random access memory locations. Must be stable for the duration of the write cycle.
A1	5	
A2	4	
A3	3	
A4	2	
A5	28	
A6	27	
A7	26	
A8	25	
A9	24	
A10	23	
D0	9	Data inputs/outputs. D0-D7 are data inputs during the compare and write modes. D0-D7 are data outputs during the read mode.
D1	10	
D2	11	
D3	12	
D4	21	
D5	20	
D6	19	
D7	18	
GND	7,8	Ground
MATCH	17	When MATCH output is at V_{OH} during a compare cycle, D0-D7 plus generated parity equals the contents of the 9-bit memory location addressed by A0-A10. MATCH is also driven high during deselect, reset, and read. Since the 'ACT2154A features an open-drain MATCH output, an external pull-up resistor of 220 Ω minimum is required.
$\overline{PE}$	15	Parity error input/output. During compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. During write cycles, $\overline{PE}$ can force a parity error into the 9th-bit location specified by A0-A10 when $\overline{PE}$ is taken to V_{IL}. $\overline{PE}$ is an open-drain output so an external pull-up resistor of 220 Ω minimum is required.
$\overline{R}$	13	Read input. When $\overline{R}$ and $\overline{S}$ are at V_{IL} and $\overline{W}$ is at V_{IH}, addressed data is output to the D0-D7 pins and the MATCH and $\overline{PE}$ outputs are forced high.
$\overline{RESET}$	1	Reset input. Asynchronously clears entire RAM array to zero and forces MATCH high when $\overline{RESET}$ is at V_{IL}.
$\overline{S}$	16	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH and $\overline{PE}$ high when $\overline{S}$ is at V_{IH}.
V_{CC}	22	Supply voltage
$\overline{W}$	14	Write control input. Writes D0-D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ and $\overline{S}$ are at V_{IL}. Places selected device in compare mode when $\overline{W}$ and $\overline{R}$ are at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage, any input . . . . . −1.5 to 7 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±25 mA
Output diode current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}): D0–D8 . . . . . ±25 mA
MATCH, $\overline{PE}$ . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage, write or compare cycles		2.2		V_{CC}+0.5	V
V_{IH}	High-level input voltage, read cycle		2.6		V_{CC}+0.5	
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2154A) and $\overline{PE}$ outputs only				5.5	V
I_{OH}	High-level output current, MATCH ('ACT2152A) and D0-D7				−8	mA
I_{OL}	Low-level output current	MATCH – 'ACT2152A			8	mA
		MATCH – 'ACT2154A			24	mA
		$\overline{PE}$			24	mA
		D0-D7			8	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, in which the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with −1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{OH}	High-level output current	MATCH ('ACT2154A) and $\overline{PE}$	V_{OH} = 5.5 V, V_{CC} = 5.5 V			10			10	μA
V_{OH}	High-level output voltage	MATCH ('ACT2152A) and D0-D7	I_{OH} = −8 mA, V_{CC} = 4.5 V	3.7			3.7			V
V_{OL}	Low-level output voltage	MATCH - 'ACT2154A	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	V
		MATCH - 'ACT2152A	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
		$\overline{PE}$	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	
		D0-D7	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
I_I	Input current		V_I = 0 − V_{CC}, V_{CC} = 5.5 V			±5			±5	μA
I_{OZ}	Off-state output current		V_O = 0 − V_{CC}, V_{CC} = 5.5 V, $\overline{S}$ at V_{IH}			±10			±10	μA
I_{CC1}	Supply current (operative)		$\overline{RESET}$ at 3 V, V_{CC} = 5.5 V, $\overline{S}$ at 0 V		85	125		85	125	mA
I_{CC2}	Supply current (reset)		$\overline{RESET}$ at 0 V, V_{CC} = 5.5 V, $\overline{S}$ at 0 V		5	25		5	25	mA
I_{CC3}	Supply current (deselected)		$\overline{RESET}$ at 3 V, V_{CC} = 5.5 V, $\overline{S}$ at 3 V		75	105		75	105	mA
C_i	Input capacitance		f = 1 MHz			5			5	pF
C_o	Output capacitance		f = 1 MHz			6			6	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), see Figures 1 and 2

compare cycle

PARAMETER			SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-M)}$	Access time from address to MATCH			14	20		18	25	ns
$t_{a(A-P)}$	Access time from address to $\overline{PE}$ high or low			17	25		22	28	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH	ACT2152A		9	15		11	15	ns
		ACT2154A		8	12		11	15	
$t_{p(D-M)}$	Propagation time, data inputs to MATCH			7	12		10	16	ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high			6	12		10	18	ns
$t_{p(RSTH-M)}$	Propagation delay, $\overline{RESET}$ high to MATCH‡			20	30		20	30	ns
$t_{p(RST-PE)}$	Propagation delay, $\overline{RESET}$ high to $\overline{PE}$‡			20	30		20	30	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high			6	10		9	12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high			6	10		9	14	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high			8	11		9	11	ns
$t_{p(WH-M)}$	Propagation delay, $\overline{W}$ high to MATCH‡			14	20		14	20	ns
$t_{p(WH-PE)}$	Propagation delay, $\overline{W}$ high to $\overline{PE}$‡			14	20		14	20	ns
$t_{v(A-M)}$	MATCH valid time after change of address		2	6		2	8		ns
$t_{v(D-M)}$	MATCH valid time after change of data		0	3		0	5		ns
$t_{v(S-M)}$	MATCH valid time (low) after $\overline{S}$ high		0	3		0	5		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address		0	3		0	5		ns

read cycle

PARAMETER		SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-D)}$	Read Access time from address to D0-D7		20	27		24	30	ns
$t_{en(S-D)}$	Enable time, $\overline{S}$ low to D0-D7		12	20		15	20	ns
$t_{en(R-D)}$	Enable time, $\overline{R}$ low to valid D0-D7 output		10	18		12	20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{R}$ low to MATCH high		6	10		9	12	ns
$t_{p(R-PH)}$	Propagation time, $\overline{R}$ low to $\overline{PE}$ high		6	10		9	15	ns
$t_{dis(R-D)}$	Disable time, $\overline{R}$ to D0-D7 (from high or low level)		10	18		12	20	ns
$t_{dis(S-D)}$	Disable time, $\overline{S}$ to D0-D7 (from high or low level)		10	18		12	20	ns
$t_{dis(W-D)}$	Disable time, $\overline{W}$ to D0-D7 (from high or low level)		10	18		12	20	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The MATCH and PE outputs will glitch at the end of a write or reset cycle after $\overline{W}$ or $\overline{RESET}$ returns high. These specifications indicate when the MATCH and $\overline{PE}$ outputs are stable after $\overline{W}$ or $\overline{RESET}$ returns high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	25			30			ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	12			15			ns
$t_{w(WL)PE}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	18			18			ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0			0			ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	10			10			ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	7			7			ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	10			10			ns
$t_{su(RST)}$	$\overline{RESET}$ inactive setup time before $\overline{W}$ low	15			15			ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0			0			ns
$t_{h(WH-D)}$	Data hold time after $\overline{W}$ high	2			5			ns
$t_{h(WL-D)}$	Data hold time after $\overline{W}$ low with MATCH high, (see Note 4)	10			10			ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	2			5			ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0			0			ns
t_{AVWH}	Address valid to write enable high	12			15			ns

NOTES: 3. The pulse-duration requirement specified by $t_{w(WL)PE}$ is only necessary when a parity error exists, (i.e., PE output is low) prior to writing data with correct parity (i.e., PE input is high during write). Parameter $t_{su(P)}$ applies only during the write cycle timing when writing a parity error.

4. $t_{h(WL-D)}$ guarantees that when $\overline{W}$ is taken low during a compare cycle with MATCH high, match will remain high without a low glitch. (As shown in the function table, $\overline{W}$ low forces MATCH high). $t_{h(WL-D)}$ is guaranteed indirectly by $t_{v(D-M)}$ and $t_{p(W-MH)}$.

PARAMETER MEASUREMENT INFORMATION

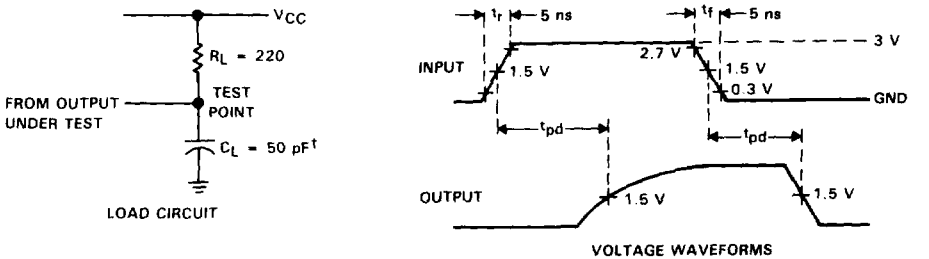


FIGURE 1. OPEN-DRAIN OUTPUTS

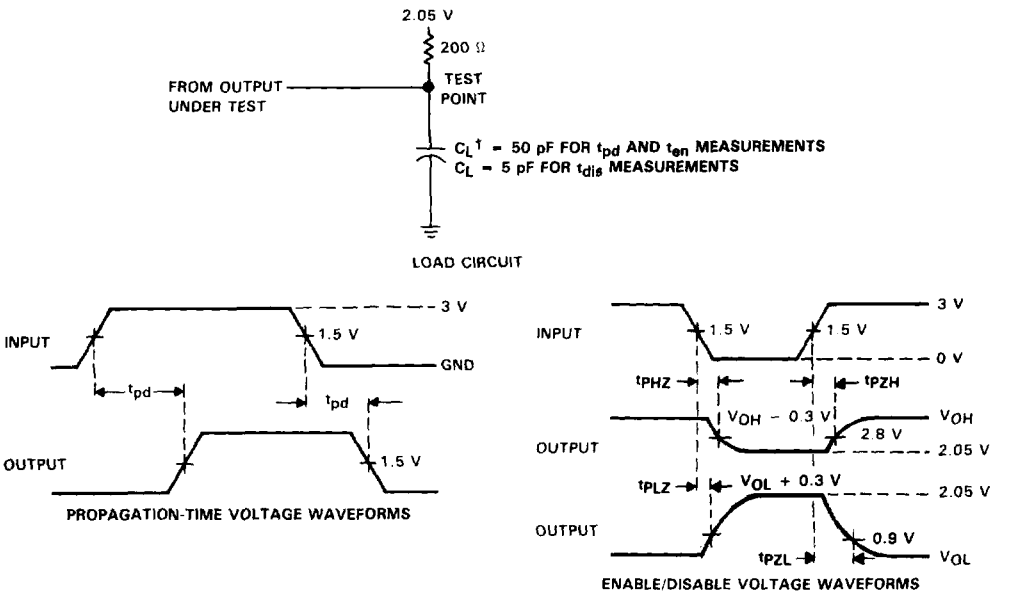
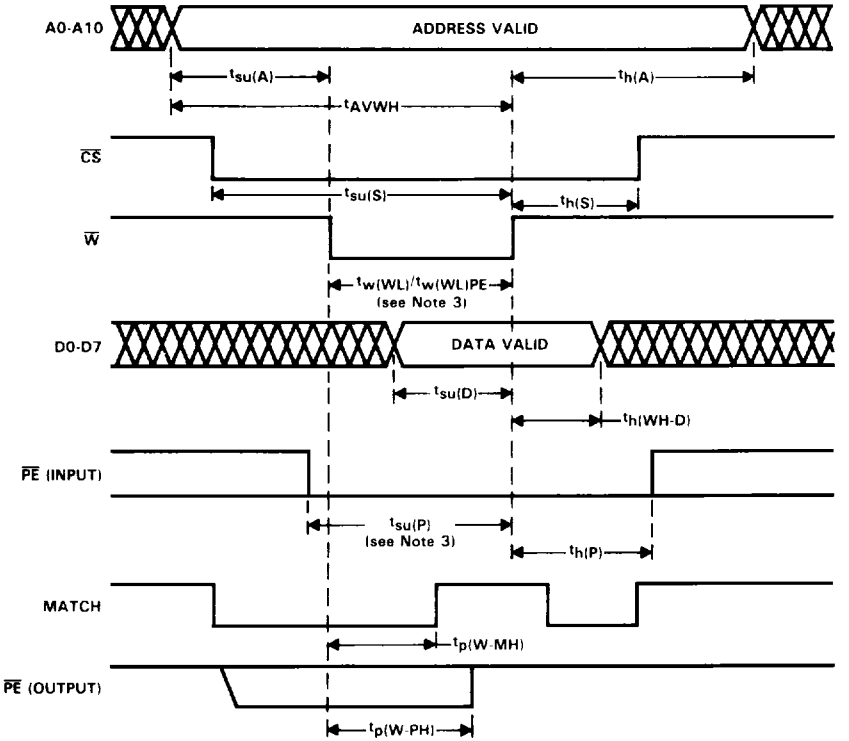


FIGURE 2. ALL OTHER OUTPUTS

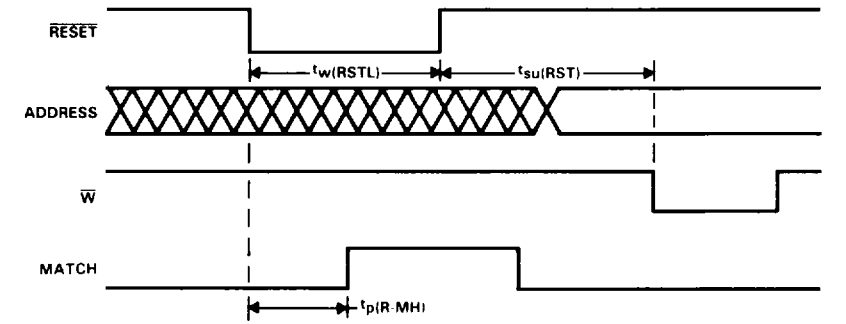
†C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

write cycle timing



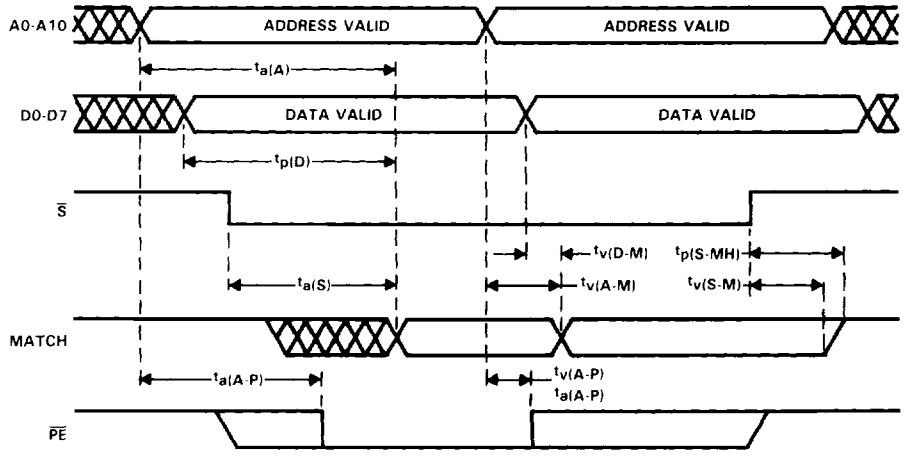
reset cycle timing



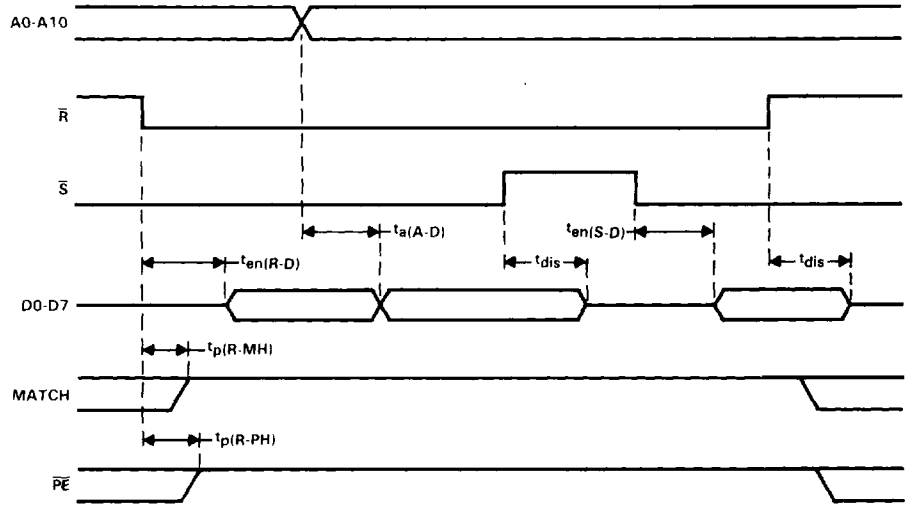
NOTE 3. Parameters $t_{w(WL)PE}$ and $t_{su(P)}$ apply only during the write cycle when writing a parity error

PARAMETER MEASUREMENT INFORMATION

compare cycle timing



read cycle timing



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APPLICATION INFORMATION

cascading the 'ACT2152A and 'ACT2154A

The 'ACT2152A and 'ACT2154A are easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A10 inputs of each device with the same index and applying the additional address bits to the D0-D7 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the MATCH output is driven high. It should be noted that a decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH on the 'ACT2154A is an open-drain output for easy AND-tying. Figure 3 shows the 'ACT2154A cascaded.

cache coherency through bus watching

When cache designs are implemented, the problem of cache coherency is always a concern. One solution to this problem is to implement bus-watching using the 'ACT2152A or 'ACT2154A. By storing the same tags in the bus-watcher RAM as are stored in the cache tag RAM, the bus-watcher will indicate a hit every time a cache address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 4 shows a possible bus-watcher implementation.

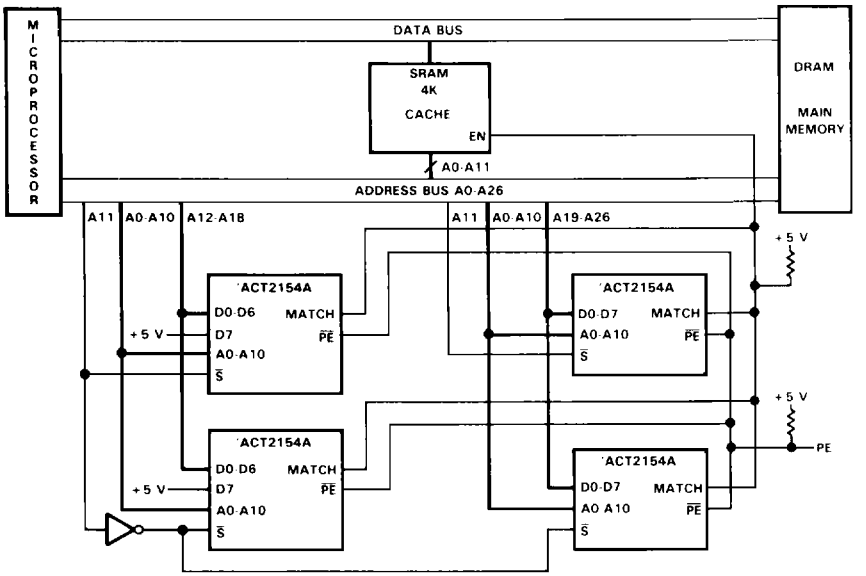

FIGURE 3. CASCADING THE 'ACT2154A

TYPICAL APPLICATION INFORMATION

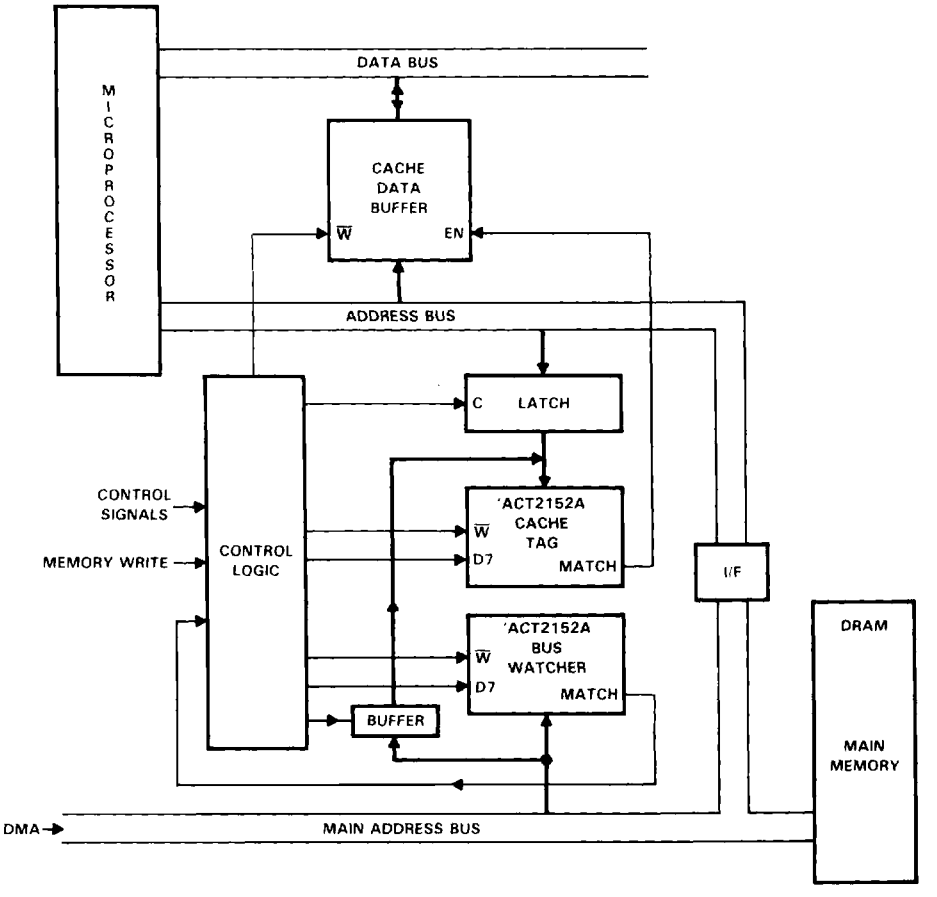

FIGURE 4. BUS WATCHING USING THE 'ACT2152A