

Fine Tune Sensitivity 2-wired Monaural Microphone Amplifier with Regulator for Microphone Capsule

■ FEATURES

- Operating Voltage Range V_{DD} = 2.7V to 16V
- 2-wired connections
- Built-in Regulator for Microphone Capsule 1.6V typ.
- Voltage Gain Range

24dB to 40dB (Set by external resistors.)

-112dBV typ.

- Adjust and memorize the gain by Single-wire serial interface
- Gain Adjustment
 9dB ±3dB/0.2dB step
- Maximum Output Voltage 1.5Vrms min.
- Equivalent Input Noise Voltage
- CMOS Technology
- Package MSOP10 (TVSP10)

DESCRIPTION

The NJU72097 is a monaural microphone amplifier IC including regulator for microphone capsule, gain adjustor, filter amplifier and line amplifier. It is able to set the output gain by external resistors. And it is able to adjust and memorize the gain after parts assembling.

The NJU72097 is the most suitable for the microphone module which required accurate sensitivity such as ECM and MEMS microphone.



- Microphone module
- Hands-free microphones

BLOCK DIAGRAM





■ PIN CONFIGURATION



	NAME			
FIN NO.		TUNCTION		
1	PREOUT	Pre-amplifier output terminal		
2	FAFB	Filter amplifier feedback terminal		
3	FAOUT	Filter amplifier output terminal		
4	LINEFB	Line amplifier feedback terminal		
5	LINEOUT	Line amplifier output terminal		
6	GND	Ground terminal		
7	VREF	Reference voltage terminal		
8	PROG	Serial clock input terminal		
9	VREG	Regulator output terminal for microphone capsule		
10	PREIN	Pre-amplifier input terminal		

PRODUCT NAME INFORMATION

<u>NJU72097</u>	<u>RB2</u>	<u>(TE1)</u>
		L
Part Number	Package	Taping Form

■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN- FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU72097RB2 (TE1)	MSOP10 (TVSP10)	Yes	Yes	Sn2Bi	72097	19	2000

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■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	
Operating Voltage	V _{DD}	18 ⁽¹⁾	V	
Maxim Input Voltage	Vimax	3.3 ⁽²⁾	V	
Power Dissipation ($T_a = 25^{\circ}C$)	D-	2-Layer	m\//	
MSOP10 (TVSP10)	FD	470 ⁽³⁾	TTIVV	
Storage Temperature	T _{stg}	-40 to 150	°C	
Junction Temperature	Tj	150	°C	

(1) LINEOUT terminal.

(2) FAFB, LINEFB, PREIN terminals.

(3) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage	V _{DD}	2.7 to 16 ⁽¹⁾	V
Operating Temperature	T _{opr}	-40 to 105	°C

(1) LINEOUT terminal.

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■ ELECTRICAL CHARACTERISTICS

$[V_S = 8V, R_L = 680\Omega, R_{INF} = R_{INL} = 6.2k\Omega, R_{FBF} = 6.2k\Omega, R_{FBL} = 180k\Omega, R_D = 27k\Omega, f = 1kHz, T_a = 25^{\circ}C \text{ unless otherwise noted.}]$									
PARAMETER SYMBOL TEST CONDITIONS				TYP	MAX	UNIT			
DC CHARACTERISTICS (Rg = 0Ω , No signal, unless otherwise noted.)									
Supply Current1	IDD1		4.2	4.8	5.4	mA			
Supply Current2	I _{DD2}	$V_S = 4.7V$, $VREG = No load$, $LINEFB = 0V$	-	280	-	μA			
Supply Current3	I _{DD3}	$R_L = 0\Omega$	-	24	32	mA			
Reference Voltage	V _{REF}	FAFB, LINEFB terminals	-	614	-	mV			
Output DC Voltage	Vout	LINEOUT terminal	-	4.7	-	V			
AMPLIFIER CHARACTERISTICS (F	PREIN to LINE	OUT, unless otherwise noted.)							
PREIN Input Resistance	Ri _{PRE}		-	15	-	MΩ			
Pre-Amplifier TYP Voltage Gain	Gvtyp	$V_{IN} = 10 \text{mVrms}$, GAIN setting = 0×00	-	9	-	dB			
Pre-Amplifier MAX Voltage Gain	Gvmax	$V_{IN} = 10 \text{mVrms}$, GAIN setting = 0 × 0F	-	12	-	dB			
Pre-Amplifier MIN Voltage Gain	Gvmin	$V_{IN} = 10 \text{mVrms}$, GAIN setting = 0 × 10	-	5.8	-	dB			
Filter-Amplifier Open loop Voltage Gain	AVFA	$R_{LFA} = 2k\Omega^{(1)}$	-	75	-	dB			
Filter-Amplifier Gain Bandwidth Product	GBPFA	$R_{LFA} = 2k\Omega^{(1)}$	-	1	-	MHz			
Filter-Amplifier Phase Margin	φfa	$R_{LFA} = 2k\Omega^{(1)}$	-	75	-	deg			
Voltage Gain	Gv	V _{IN} = 10mVrms	37.3	38.3	39.3	dB			
Frequency Response	ΔG _f	f = 1kHz to 10kHz	-0.5	0.0	0.5	dB			
Equivalent Input Noise Voltage	V _{NI}	Weighted-A	-	-112	-	dBV			
Total Harmonic Distortion	THD	V_{IN} = 10mVrms, BW = 400Hz to 30kHz	-	0.1	0.5	%			
Maximum Output Voltage	Vом	THD = 3%, I _{VREG} = 300µA	1.5	-	-	Vrms			
Ripple Rejection	RR	VRIPPLE = 0.5Vrms	25	30	-	dB			
REGULATOR CHARACTERISTICS	(No signal, un	less otherwise noted.)							
Output Voltage	VVREG	No load	-	1.6	-	V			
Output Current	IVREG		-	300	500	μA			
Filter Resistance	RFILTER		0.8	1.1	1.4	kΩ			

(1) Total load of the Filter-Amplifier

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■ THERMAL CHARACTERISTICS

PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance	Ο.	2-Layer	°CM/
MSOP10 (TVSP10)	Uja	266 (1)	C/W

(1) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



MSOP10 (TVSP10) Power Dissipation vs. Temperature $T_{opr} = -40^{\circ}C$ to 105°C, $T_{i} = 150^{\circ}C$

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■ TEST CIRCUIT



■ APPLICATION CIRCUIT



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I SB

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■ DEFINITION OF SERIAL REGISTER

Note) Please don't send except specified data for avoiding an incorrect operation.

SERIAL BUS FORMAT

1byte command



2byte command

	N	1SB	LSB	MSB		LSB	
P A Control Address		A		Data	E		
3bit	1bit	8bit	1b	it	8bit	2bi	t

P: Preamble

A: Acknowledge Bit (ACK)

E: End Mark

Control Address

Modo		Control Address							Hoy	Contonts	
wode	MSB		LSB						пех	Contents	
RESET	1	0	0	0	0	0	0	0	80(h)	Reload the setting from ROM.	
READ	1	0	0	0	0	0	0	1	81(h)	Output the setting to PROG terminal.	
TEST	1	0	0	0	0	0	1	0	82(h)	Write the setting on RAM and read it.	
WRITE	1	0	0	0	0	1	0	0	84(h)	Write the setting on ROM.	

CONTROL REGISTER DATA TABLE

<RESET Mode>

The Data of SERIAL BUS FORMAT is not required. Use the 1byte command format.

<READ Mode>

MSE	3
-----	---

Data								
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	Setting Data					

<TEST and WRITE Mode>

MSB							LSB		
Data									
D7	D6	D5	D4	D3	D2	D1	D0		
Don't Care	Don't Care	Don't Care	GAIN						

CONTROL REGISTER DEFAULT VALUE OF INTERNAL ROM

The NJU72097 read setting from internal ROM when power is turn on. Control register default value of internal ROM is all "0" before you write setting on ROM.

MSB							LSB
			Da	ata			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

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■ DEFINITION OF RESISTOR

The gain is controlled 5.8dB to 12.0dB in 0.2dB/step by 5-bit signed binary.

MSB							LSB
	Data						
D7	D6	D5	D4	D3	D2	D1	D0
Don't Care	Don't Care	Don't Care	GAIN				

<GAIN Data>

Data				Catting	
D4	D3	D2	D1	D0	Setting
1	0	0	0	0	+5.8dB
1	0	0	0	1	+6.0dB
1	0	0	1	0	+6.2dB
1	0	0	1	1	+6.4dB
1	0	1	0	0	+6.6dB
1	0	1	0	1	+6.8dB
1	0	1	1	0	+7.0dB
1	0	1	1	1	+7.2dB
1	1	0	0	0	+7.4dB
1	1	0	0	1	+7.6dB
1	1	0	1	0	+7.8dB
1	1	0	1	1	+8.0dB
1	1	1	0	0	+8.2dB
1	1	1	0	1	+8.4dB
1	1	1	1	0	+8.6dB
1	1	1	1	1	+8.8dB
0	0	0	0	0	+9.0dB ^(T)
0	0	0	0	1	+9.2dB
0	0	0	1	0	+9.4dB
0	0	0	1	1	+9.6dB
0	0	1	0	0	+9.8dB
0	0	1	0	1	+10.0dB
0	0	1	1	0	+10.2dB
0	0	1	1	1	+10.4dB
0	1	0	0	0	+10.6dB
0	1	0	0	1	+10.8dB
0	1	0	1	0	+11.0dB
0	1	0	1	1	+11.2dB
0	1	1	0	0	+11.4dB
0	1	1	0	1	+11.6dB
0	1	1	1	0	+11.8dB
0	1	1	1	1	+12.0dB
					(T) Initial Setting

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Serial bus (PROG) control

The NJU72097 has a single-wire serial interface with a PROG terminal which is three-state control of H (High Level), M (Middle Level), and L (Low Level), and data logical values are assigned to H and M as shown in Table 1.

Control	signal of PROG terminal	
State	Voltage value	
Н	Vprog [V]	1
М	1/2 Vprog[V]	0
L	0[V]	-

Table1	Control	logic table	of PROG	terminal
TUDIC I.	0011001	logio labic		

An example of writing circuit

Figure 1 is an example of a write circuit using a 3-state buffer consisting of Tr1 and Tr2. Table 2 is a truth table in which the PROG terminal is controlled in 3 states by CLK and DAT signals by this buffer. The buffer also supplies OTP write current from Tr1 and generates M level by RPULLUP_DATA and RPULLDOWN_DATA when the buffer is Hi-Z.



Fig1. An example of writing circuit

Table 2. A truth table of an example	le of writing	circuit.
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input	data	Control data		
CLK	DAT	PROG terminal	Assigned logical value	
Н	Н	H: Vprog [V]	1	
Н	L	M: 1/2Vprog [V]	0	
L	Н	Prohibit	-	
L	L	L: Vprog [V]	-	

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■ TIMING ON SERIAL BUS (PROG)

The NJU72097 adopts the single-wire serial interface by PROG terminal. The serial data is structured by Preamble, Acknowledge (ACK), Control Address, Data and End Mark. And PROG terminal is controlled by three values, H (High Level), M (Middle Level), and L (Low Level). Fig. 2 The upper part shows the control sequence diagram of the PROG terminal, and the lower part shows the sequence diagram of the DAT terminal and CLK terminal when the writing circuit example of Fig. 1 is used.



Wait Condition

The NJU72097 is wait condition when the CLK is "L", the DAT is "L" and the PROG terminal is "L" which is 0 [V] for 2msec or more.

Preamble

The serial control function of NJU72097 is activated by inputting three H level pulses (P0, P1, P2,). Then, the EN of the internal circuit in Fig. 1 becomes H, and the PROG terminal voltage is pulled down by the internal resistance of $3.9 \text{ k}\Omega$. Furthermore, by inputting the M level pulse at the timing of A0, the PROG terminal voltage becomes M (about 1/2Vprog [V]). By monitoring the PROG terminal voltage with the MCU, you can check the operating status of the NJU72097. If an error occurs, the PROG terminal voltage A0 becomes H (Vprog [V]).

Control Address

The NJU72097 is controlled by sending an 8-bit Control Address (C7 to C0).

If the control address is successfully read, the PROG terminal voltage of A1 becomes M (about 1/2Vprog [V]) by inputting the M level pulse at the timing of A1. If an error occurs, the PROG terminal voltage will be H (Vprog [V]).

Data

8-bit serial data (D7 to D0) sent to the internal register of NJU72097. The data truth table is shown in Tables 1 and 2.

In READ mode, M level 8-bit serial Data (D7 to D0) is transmitted and the data signal that appears as the PROG terminal voltage is read out. Table 3 shows the relationship between the transmitted data and the read data in the circuit shown in Fig. 1.

send	data	Read data				
CLK	DAT	PROG terminal voltage	Assigned logical value			
Н	L	H: Vprog [V]	1			
Н	L	M: 1/2Vreg [V]	0			

Table 3. Truth table of transmitted data and read data in READ mode

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End Mark

After sending the control address with the 1-byte command and sending or receiving data with the 2-byte command, you can confirm that the communication has ended by monitoring the PROG terminal voltage with the MCU. If the M level is transmitted at the timing of E0 and E1, the PROG terminal voltage will be M level (about 1/2 Vprog [V]) at E0 and H (Vprog [V]) at E1.If an error occurs, the value will be different.

■ CHARACTERISTICS OF I/O STAGES FOR SERIAL BUS (PROG)

 $(V_{S} = 8V, R_{L} = 680\Omega, R_{INF} = R_{INL} = 6.2k\Omega, R_{FBF} = 6.2k\Omega, R_{FBL} = 180k\Omega, R_{D} = 27k\Omega, V_{PROG} = 5V, R_{PULLUP_DATA} = 3.9k\Omega, T_{a} = 25^{\circ}C$ unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High Level Input Voltage	VIH	4.5	5.0	5.5	V
High Level Input Voltage for OTP Writing	VIHW	4.8	5.0	5.2	V
Low Level Input Voltage	VIL	0.0	-	0.3	V
Middle Level Output Voltage	Vo	2.25	-	2.75	V
Supply Current for OTP Writing	WRITE	-	-	100	mA

■ CHARACTERISTICS OF BUS LINE (PROG) FOR SERIAL BUS DEVICES

 $(V_{S} = 8V, R_{L} = 680\Omega, R_{INF} = R_{INL} = 6.2k\Omega, R_{FBF} = 6.2k\Omega, R_{FBL} = 180k\Omega, R_{D} = 27k\Omega, V_{PROG} = 5V, R_{PULLUP_DATA} = 3.9k\Omega, T_{a} = 25^{\circ}C$ unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Clock Frequency	f _{PROG}	-	50	-	kHz
Rise Time	t _R	-	-	1	µsec
Rise time for OTP Writing	t RH	-	-	300	nsec
Fall time	t⊧	-	-	300	nsec
Pulse Width	t₽	4.7	-	10.5	µsec
High Level Pulse Width for OTP Writing	t _{HVV}	9.5	10.0	10.5	µsec
Bus free time between the End Mark and the Preamble	t BUF	2	-	-	msec



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APPLICATION NOTES





1. Supply Voltage of Vs

The recommended supply voltage of Vs is as follows:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	Vs		-	8	-	V

2. Voltage Gain

2.1 Pre-Amplifier

 $G_{VP} = 9 [dB]$

2.2 Filter Amplifier

 $G_{VP} = 20 \cdot Log \left(\frac{R_{FBF}}{R_{INF}}\right) [dB]$ Ex. $G_{VF} = 20 \cdot Log \left(\frac{6.2k}{6.2k}\right) = 0 [dB]$

2.3 Line Amplifier

$$\begin{aligned} G_{VL} = 20 \cdot \text{Log} \left(\frac{\text{R}_{\text{FBL}}}{\text{R}_{\text{INL}}}\right) \text{ [dB]} & \text{Ex. } G_{VL} = 20 \cdot \text{Log} \left(\frac{180\text{k}}{6.2\text{k}}\right) \approx 29.3 \text{ [dB]} \\ V_{\text{OUT}} = V_{\text{REF}} \cdot \left(1 + \frac{\text{R}_{\text{FBL}}}{\text{R}_{\text{D}}}\right) \text{ [V]} & \text{Ex. } V_{\text{OUT}} = 614\text{m} \cdot \left(1 + \frac{180\text{k}}{27\text{k}}\right) \approx 4.7 \text{ [V]} \end{aligned}$$

2.4 NJU72097

$$G_{V} = G_{VP} + G_{VF} + G_{VL} = G_{VP} + 20 \cdot \text{Log} \left(\frac{R_{FBF}}{R_{INF}} \cdot \frac{R_{FBL}}{R_{INL}}\right) \text{ [dB]}$$

Ex. $G_{V} = 9 + 20 \cdot \text{Log} \left(\frac{6.2k}{6.2k} \cdot \frac{180k}{6.2k}\right) \approx 38.3 \text{ [dB]}$

Note) The value of R_{VREG} should use $1.1 k \Omega.$ Do not use $2.2 k \Omega.$

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3. Output Voltage Range

3.1 High side minimum saturation voltage $V_{\mbox{\tiny Hsat}}$

$$\begin{split} I_{RF} &= \frac{V_{OUT}}{R_{FBL} + R_D} \quad \cdots \quad \text{Current for feedback resistor } R_{FBL}, \ R_D \\ \text{Ex.} \ I_{RF} &= \frac{4.7}{180k + 27k} \approx 23 \ [\mu\text{A}] \\ V_{\text{Hsat}} &= (I_{DD2} + I_{RF}) \cdot R_L \ [V] \end{split}$$

Ex. $V_{Hsat} = (280\mu + 23\mu) \cdot 680 \approx 0.2 [V]$

3.2 Low side minimum saturation voltage $V_{\mbox{\tiny Lsat}}$

 $V_{Lsat} \approx 2.15 [V]$ (typ.) at $T_a = 25^{\circ}C$

3.3 Output Voltage Range Vo

 $V_{O} = V_{S} - (V_{Hsat} + V_{Lsat}) [V]$

Ex. $V_0 = 8 - (0.2 + 2.15) = 5.65 [V_{PP}] \approx 2.0 [Vrms]$





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NJU72097

Unit: mm

MSOP10 (TVSP10) MEET JEDEC MO-187-DA/THIN TYPE

■ PACKAGE DIMENSIONS





■ EXAMPLE OF SOLDER PADS DIMENSIONS







NJU72097

MSOP10 (TVSP10) MEET JEDEC MO-187-DA/THIN TYPE

Unit: mm

PACKING SPEC TAPING DIMENSIONS



SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
В	3.2	BOTTOM DIMENSION
DO	1.5 ^{+0.1}	
D1	1.5 ^{+0.1}	
E	1.75±0.1	
F	5.5±0.05	
PO	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
Т	0.3 ± 0.05	
T2	1.75 (MAX.)	
W 12.0±0.3		
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS



SYMBOL	DIMENSION
А	254 ± 2
В	100 ± 1
С	13±0.2
D	21 ± 0.8
Е	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE



PACKING STATE



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RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



а	Temperature ramping rate	1 to 4°C/s
h	Pre-heating temperature	150 to 180°C
υ	Pre-heating time	60 to 120s
С	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
е	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate 1 to 6°C/s	
The temperature indicates at the surface of mold package		

■ REVISION HISTORY

DATE	REVISION	CHANGES
December 7, 2020	Ver.1.0	Initial release

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