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CMOS linear image sensor

S16074

Low power consumption, capable of switching pixel sizes by SPI

The S16074 is a CMOS linear image sensor developed for industrial cameras. It comes with built-in timing generators, bias generators, amplifiers, and 12-bit A/D converters. The video signal is output serially in 320 MHz LVDS format. 3 lines of pixel size of 7 × 7 µm, 9.3 × 9.3 µm, and 14 × 14 µm are arranged in parallel in the photosensitive area and can be switched with the SPI settings.

Features

- **Pixel size: 7 × 7 µm, 9.3 × 9.3 µm, 14 × 14 µm**
- **High-speed readout: 65 klines/s max. (pixel size: 14 × 14 µm)**
- **Simultaneous integration of all pixels**
- **3.3 V power supply operation**
- **SPI communication function**
- **Built-in 12-bit A/D converter**

Applications

- **Machine vision**
- **Film inspection**
- **Printed circuit board appearance inspection**
- **Print inspection**

Structure

Parameter	Specification			Unit
Photosensitive area*1	①	②	③	-
Total number of pixels	4160	3120	2080	-
Number of effective pixels	4096	3072	2048	-
Dummy pixels*2 *3	16	12	8	pixels
Light-shielding pixels*3 *4	16	12	8	pixels
Pixel pitch*5	7	9.3	14	µm
Pixel height*5	7	9.3	14	µm
Package	Ceramic			-
Window material*6	Borosilicate glass			-

*1: See dimensional outline (P.15) and enlarged view of effective photosensitive area (P.16) capable of switching by SPI.
*2: The pixels on the left and right outside of effective pixels have the same structure as the effective pixels, so there is output according to incident light.
*3: These are not read out with initial settings. It is possible to switch to readout with SPI settings.
*4: Light-shielded pixels on the left and right outside of the dummy pixels (optical black)
*5: Can be selected by SPI
*6: With AR coat (double-sided multi-coat, reflectance 1% or less at 400 to 800 nm)

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	V
Digital input signal terminal voltage*7		Vi		-0.3 to +3.9	V
Vref_cp1 terminal voltage		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*8	-40 to +85	°C
Storage temperature		Tstg	No dew condensation*8	-40 to +85	°C

*7: CS, SCLK, MOSI, RSTB, MCLK, MST, All_Reset, PLL_Reset
*8: When there is a temperature difference between a product and the surrounding area in high humidity environments, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.15	3.3	3.45	V
	Digital terminal	Vdd(D)	3.15	3.3	3.45	
Digital input voltage	High level	Vi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.3	

Electrical characteristics

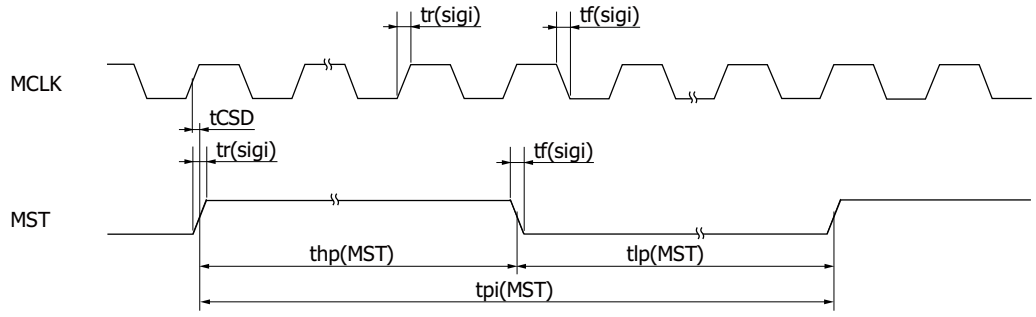
Digital input signal

[Ta=25 °C, Vdd (A)=Vdd (D)=3.3 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency		f(MCLK)	15	-	40	MHz
Master clock pulse duty cycle		D(MCLK)	45	50	55	%
Master start pulse cycle	7 × 7 µm	tpi(MST)	1127/f(MCLK)	-	-	s
	9.3 × 9.3 µm		871/f(MCLK)	-	-	
	14 × 14 µm		615/f(MCLK)	-	-	
Master start pulse	High period	thp(MST)	91/f(MCLK)	-	-	s
	Low period	tlp(MST)	21/f(MCLK)	-	-	
Delay between master clock and master start		tCSD	0	-	5	ns
Delay between master clock and reset*9		tCRD	-	-	5	ns
Rise time*10		tr(sigi)	-	5	7	ns
Fall time*10		tf(sigi)	-	5	7	ns

*9: Delay time of the rising edges of PLL_Reset and All_Reset relative to the rising edge of MCLK
*10: Time for the input voltage to rise or fall between 10% and 90%

■ MCLK, MST input timing



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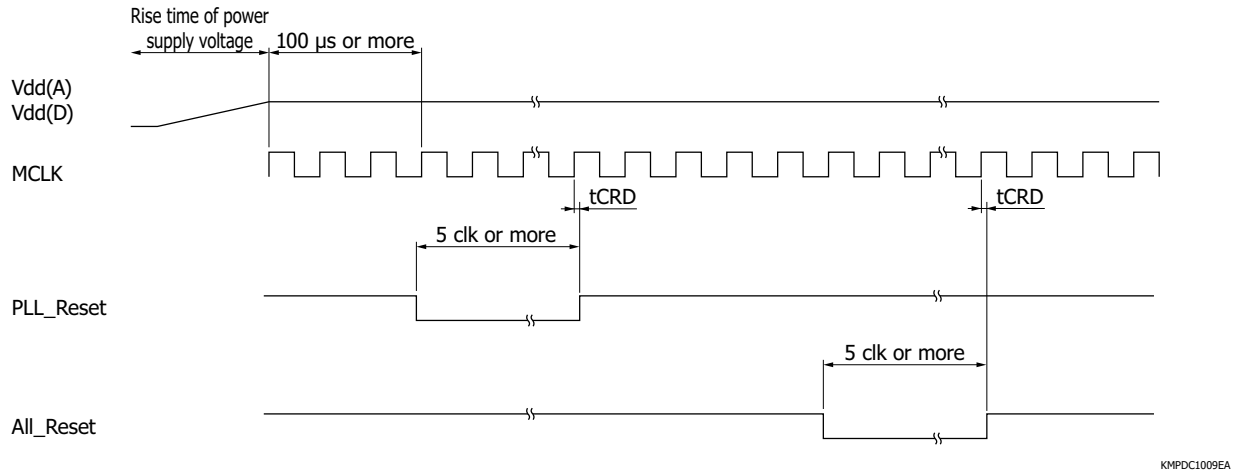
■ PLL_Reset, All_Reset input timing

After 100 µs or longer after turning on the power supply, set the PLL_Reset and the All_Reset to low in this order during the time period of the master clock pulse 5 clk or more.



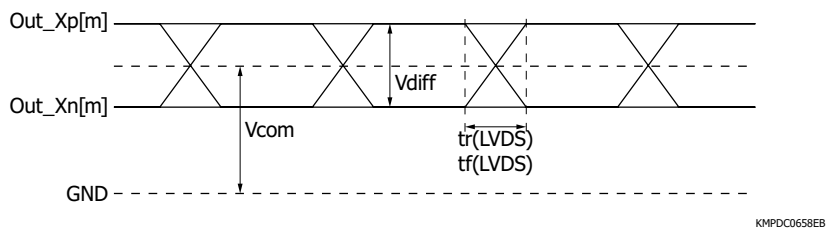
Digital output signal

[Ta=25 °C, Vdd (A)=Vdd (D)=3.3 V, f (MCLK)=40 MHz]

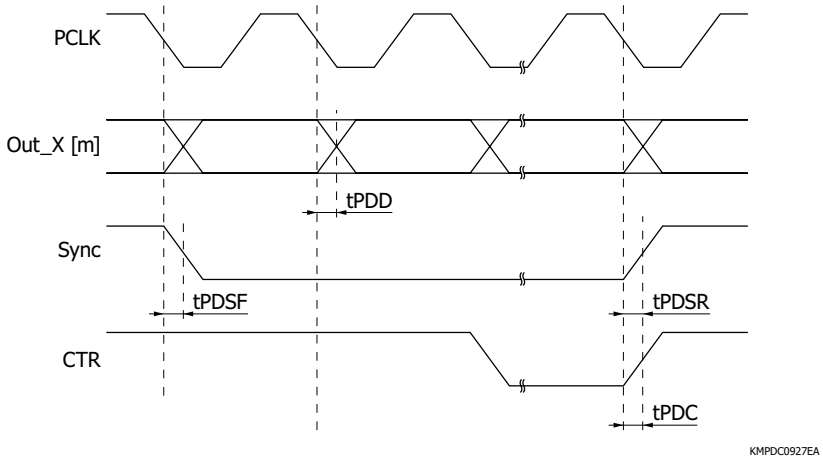
Parameter		Symbol	Min.	Typ.	Max.	Unit
Video data rate (LVDS)		DR		f(MCLK) × 8		MHz
Line rate	7 × 7 µm	LR	-	-	35	klines/s
	9.3 × 9.3 µm		-	-	46	
	14 × 14 µm		-	-	65	
LVDS output voltage*11	Offset	Vcom	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	
LVDS rise time*12		tr(LVDS)	-	0.9	1.3	ns
LVDS fall time*12		tf(LVDS)	-	0.9	1.3	ns
Delay between bit output sync signal and video output*13		tPDD	-0.8	0.1	1	ns
Delay between bit output sync signal and pixel sync signal*13		tPDC	-0.75	0.15	1.05	ns
Delay between bit output sync signal and frame sync signal	Rise time*13	tPDSR	-1.35	-0.45	0.55	ns
	Fall time*13	tPDSF	-1.35	-0.45	0.55	
CMOS output voltage	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	
Timing generator clock pulse frequency		f(TGCLK)	-	f(MCLK)	-	MHz
CMOS output rise time*14		tr(sigo)	-	10	12	ns
CMOS output fall time*14		tf(sigo)	-	10	12	ns

*11: Attach a 100 Ω terminator to the LVDS output terminal.
*12: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal
*13: pclk_delay [5:0]=6
*14: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal

■ LVDS output voltage



■ Sync signal, video signal



· Each waveform represents the difference between positive and negative signals of LVDS.
· Out_X[m] indicates video outputs.
  X: A, B (port)
  m: 0=0 to 3 bits, 1=4 to 7 bits, 2=8 to 11 bits
· Acquire the video output at the rising edge of PCLK.
· After the rise of Sync, video output starts. Use Sync as a reference when importing data [see timing chart (P.9)].
· Simultaneous with a rise of CTR , Out_X [0] is output from D0, Out_X [1] is output from D4, and Out_X [2] is output from D8. Use CTR as a reference when importing data [see timing chart (P.10)].

Current consumption

[Ta=25 °C, Vdd (A)=Vdd (D)=3.3 V, f(MCLK)=40 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vdd(A) terminal	Ic1	275	320	365	mA
Vdd(D) terminal	Ic2	135	160	185	

Electrical characteristics of A/D converters [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, f(MCLK)=40 MHz]

Parameter	Symbol	Specification	Unit
Resolution	RESO	12	bit
Conversion voltage range	-	0 to1.3	V

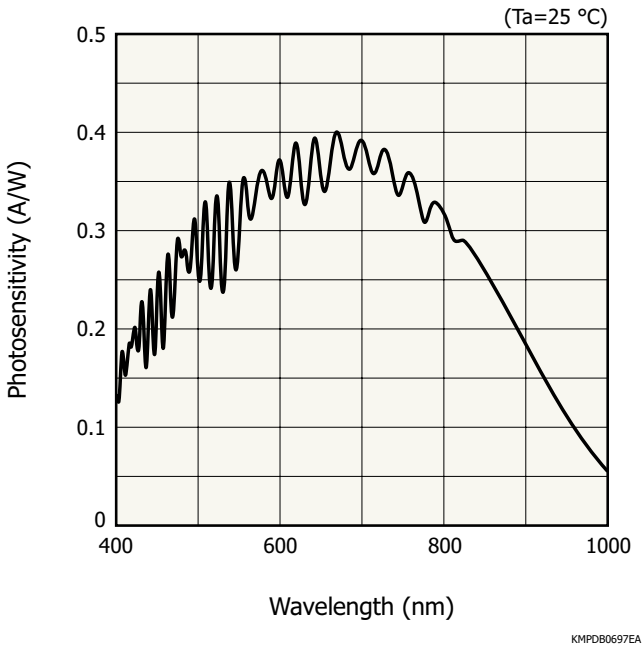
Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, f(MCLK)=40 MHz, offset: default value]

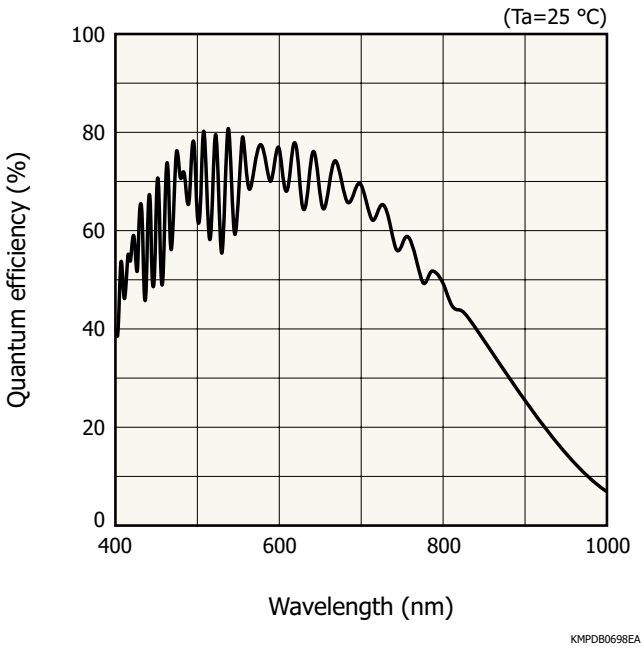
Parameter	Symbol	Gain	Pixel size	Min.	Typ.	Max.	Unit
Spectral response range	λ	-			400 to 1000		nm
Peak sensitivity wavelength	λp	-		-	700	-	nm
Photosensitivity*15	Sw	1	7 × 7 μm	-	45	-	V/(lx·s)
			9.3 × 9.3 μm	-	72	-	
			14 × 14 μm	-	54	-	
		8	7 × 7 μm	-	360	-	
			9.3 × 9.3 μm	-	574	-	
			14 × 14 μm	-	430	-	
Conversion factor	CE	1	7 × 7 μm	-	42	-	μV/e⁻
			9.3 × 9.3 μm	-	38	-	
			14 × 14 μm	-	13	-	
		8	7 × 7 μm	-	336	-	
			9.3 × 9.3 μm	-	304	-	
			14 × 14 μm	-	104	-	
Output offset level	Voffset	-		-	550	-	DN
Dark output*16	VD	1	7 × 7 μm	-	0.5	20	mV
			9.3 × 9.3 μm	-	0.4	15	
			14 × 14 μm	-	0.24	9.6	
		8	7 × 7 μm	-	4	160	
			9.3 × 9.3 μm	-	3.2	120	
			14 × 14 μm	-	1.9	77	
Saturation output	Vsat	-		1.05	1.13	-	V
Saturation charge	Qsat	1	7 × 7 μm	25	27	-	ke⁻
		1	9.3 × 9.3 μm	28	30	-	
		1	14 × 14 μm	81	87	-	
Readout noise*17	Nread	1		-	0.6	1.9	mV rms
		8		-	1.6	4.7	
SNR max.	-	1	7 × 7 μm	43	44	-	dB
			9.3 × 9.3 μm	44	45	-	
			14 × 14 μm	48	49	-	
		8	7 × 7 μm	34	35	-	
			9.3 × 9.3 μm	35	36	-	
			14 × 14 μm	39	40	-	
Dynamic range*18	Drange	1		550	1900	-	-
		8		220	700	-	
Photoresponse nonuniformity*19	PRNU	1		-	±5	±10	%
		8		-	±5	±10	
Image lag*20	Lag	1		-	-	0.1	%

*15: Measured with a 2856 K tungsten lamp
*16: Ts= 10 ms, difference from the offset output level
*17: Dark state
*18: Vsat/Nread
*19: Photoresponse nonuniformity is defined as follows when uniform light with an exposure of 50% of saturation enterd.
PRNU = ΔX/X × 100 (%)
X: average of the outputs of N pixels
ΔX: difference between the maximum or minimum output of N pixels and X
N: 4096 (pixel size: 7 × 7 μm), 3072 (pixel size: 9.3 × 9.3 μm), 2048 (pixel size: 14 × 14 μm)
*20: The signal component of the previous data that remains after data is read under saturation output conditions. Image lag increases if light greater than the saturation exposure is incident.

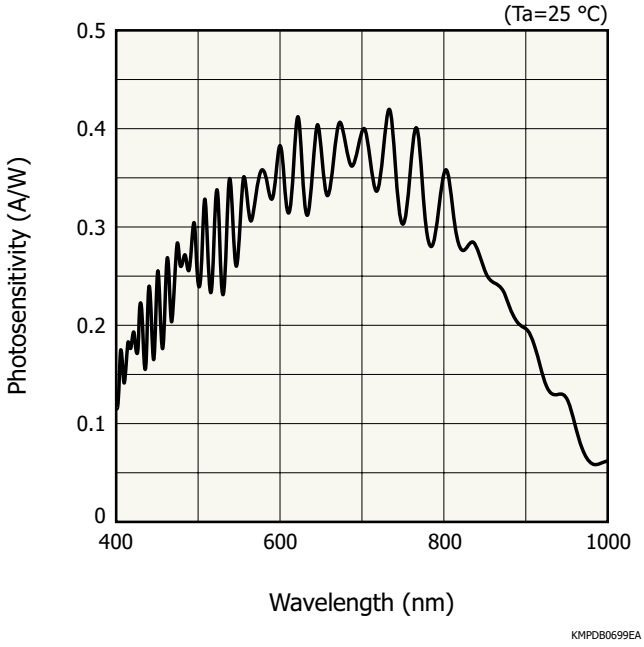
Spectral response (typical example)

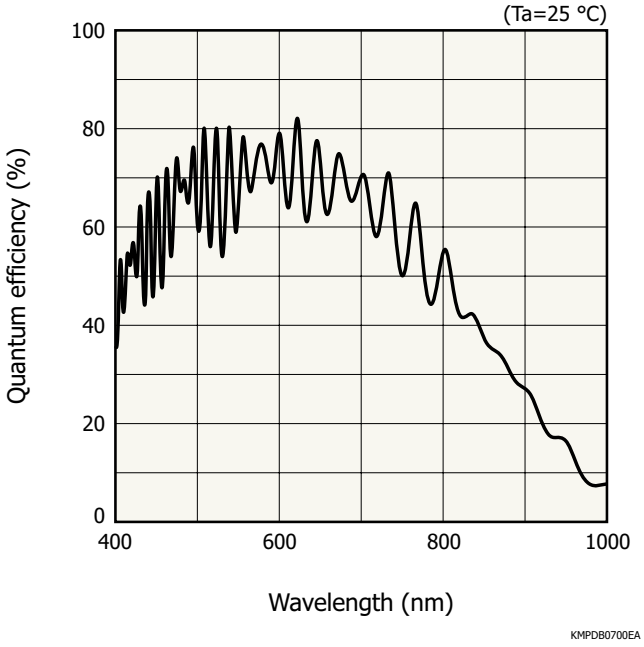
Pixel size: 7 × 7 µm



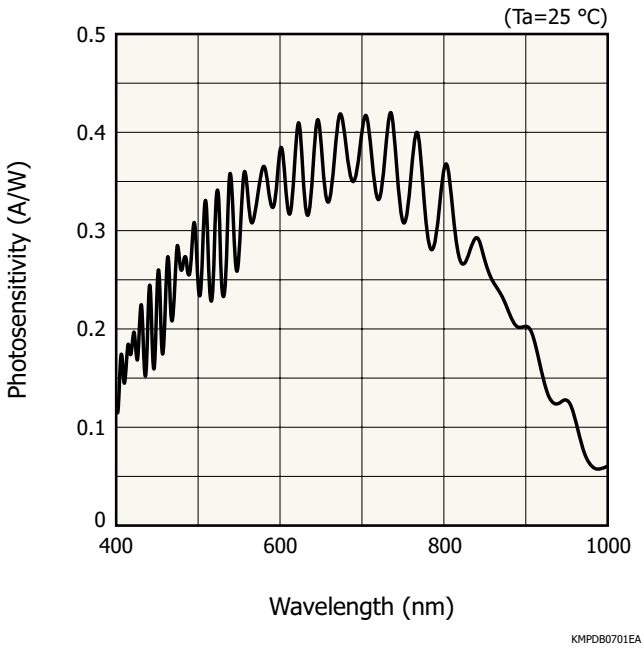


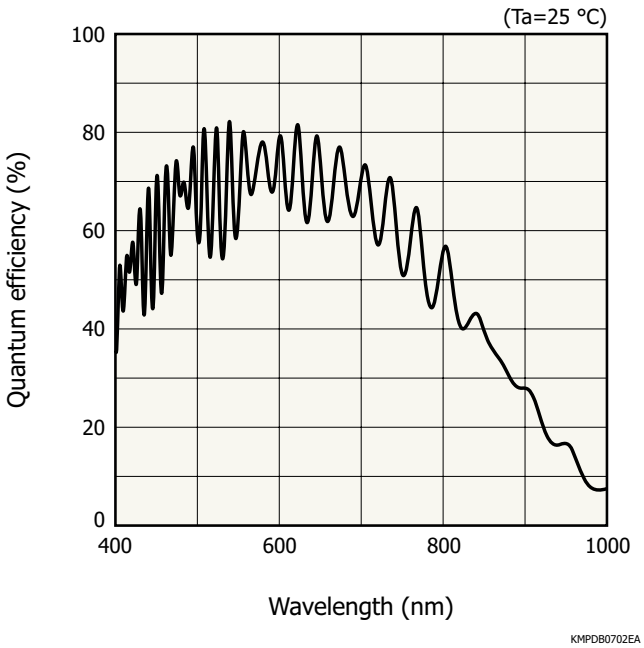
Pixel size: 9.3 × 9.3 µm



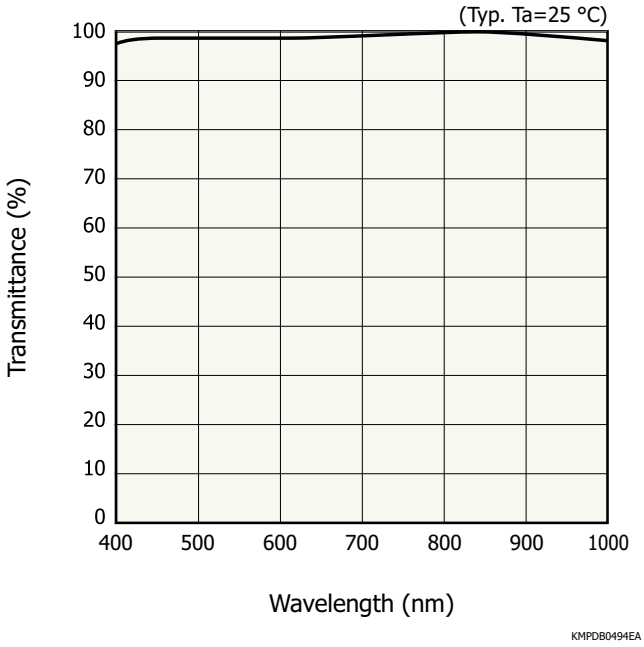


Pixel size: 14 × 14 µm



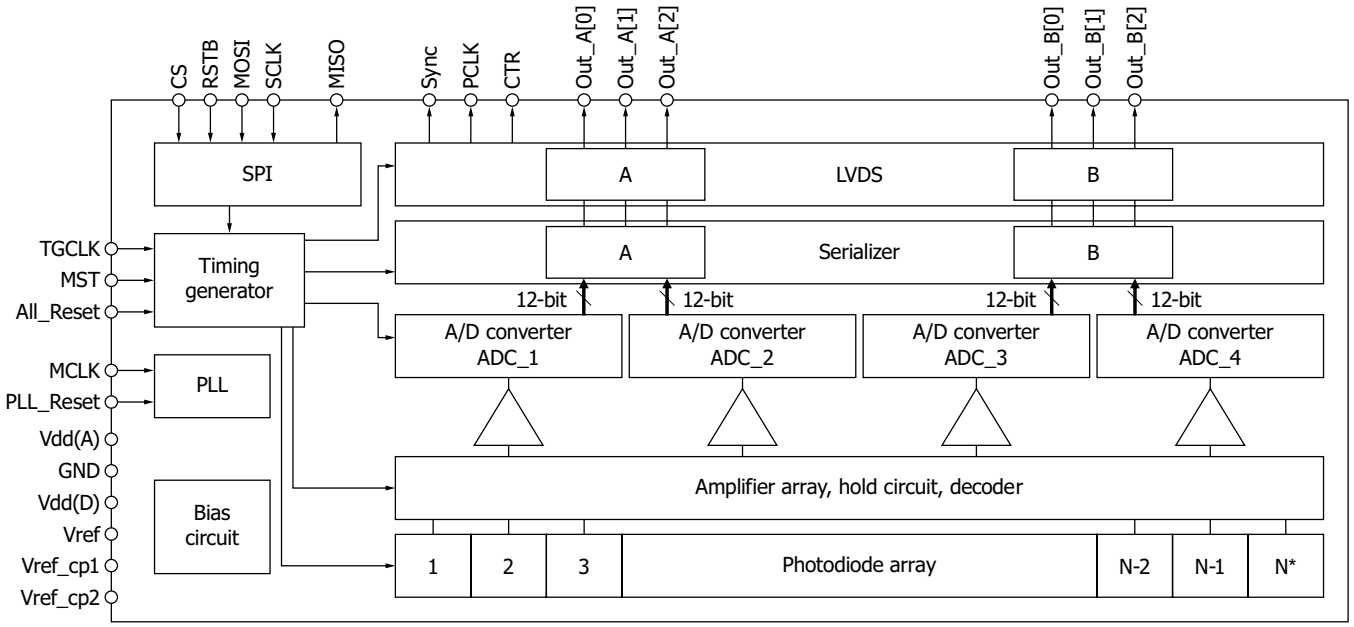


Spectral transmittance of window material



Block diagram

The video output signals are output separately to 2 ports: A and B.



N=4096 (pixel size: 7 × 7 μm)
3072 (pixel size: 9.3 × 9.3 μm)
2048 (pixel size: 14 × 14 μm)

Note: excluding dummy pixels and light-shielding pixels

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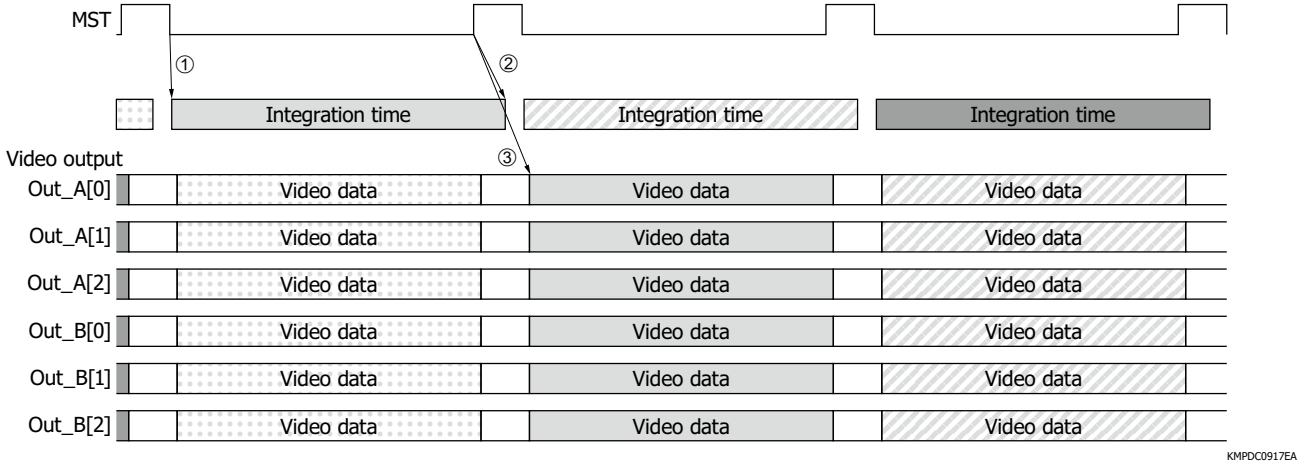
Timing chart

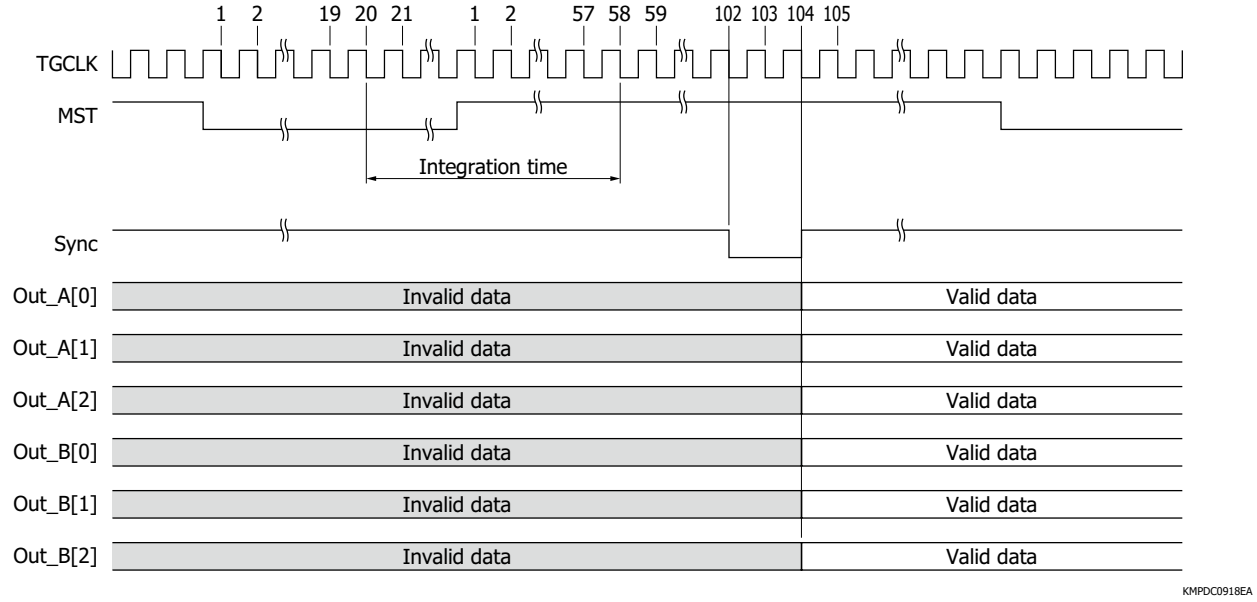
■ Description of operation

The integration time is determined by the low period of the master start pulse.



(1) The start of integration time is determined by the falling edge of the master start pulse.
(2) The end of integration time is determined by the rising edge of the master start pulse.
(3) Video data is output after the rising edge of the next frame after the master start pulse. Video data is output in order from the first pixel.
Note: Signal integration is possible even during video output.

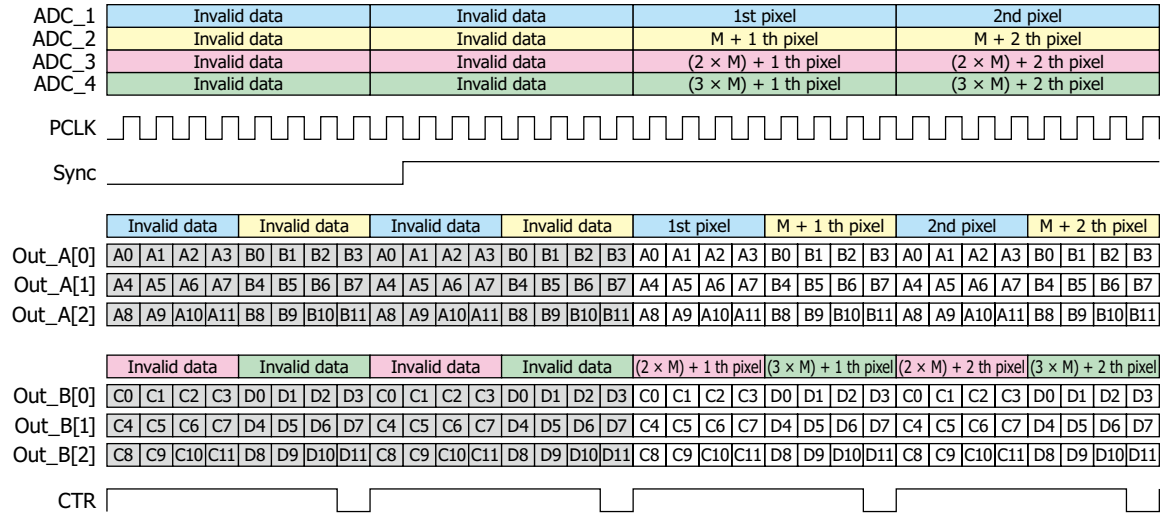
■ Start/end timing of the integration time, video output start position



· Line rate corresponds to the master start pulse period.
· TGCLK is a timing generator clock inside the sensor.
· The integration time corresponds to the low period of the master start pulse + 38 cycles of TGCLK.

■ Video output

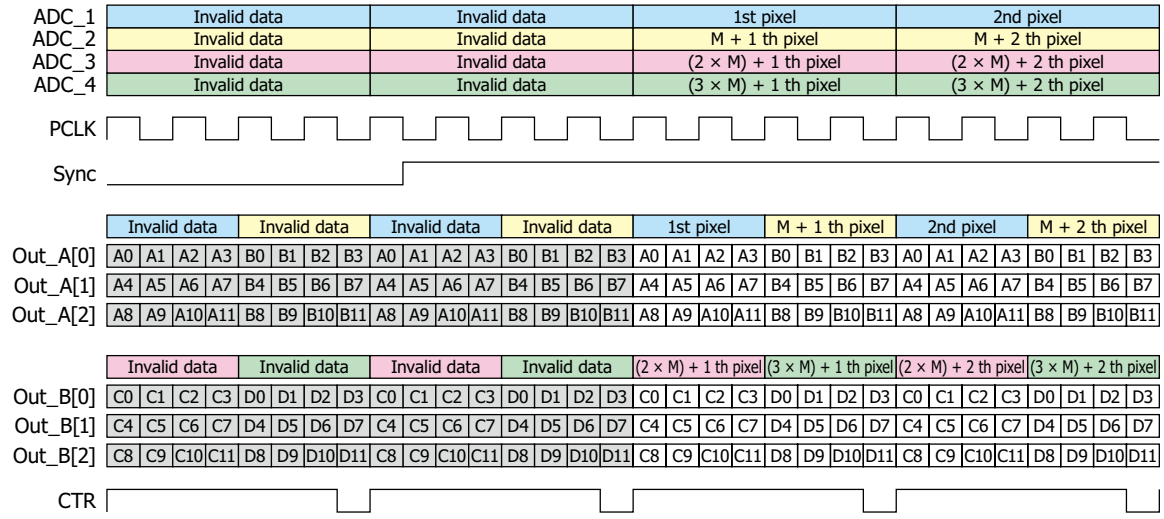
PCLK frequency = f(MCLK) × 8



Note: M=1024 (pixel size: 7 × 7 µm), 768 (pixel size: 9.3 × 9.3 µm), 512 (pixel size: 14 × 14 µm)

KMPDC0919EA

PCLK frequency = f(MCLK) × 4



Note: M=1024 (pixel size: 7 × 7 µm), 768 (pixel size: 9.3 × 9.3 µm), 512 (pixel size: 14 × 14 µm)

KMPDC0920EA

SPI address settings

Address (Decimal)	Register	Initial value		Setting
		Binary	Decimal	
0	Mode[1:0]	---- --00	0	Pixel size, number of pixels (initial setting: 7 × 7 µm, 4096 pixels)
1	fpclk	---- ---0	0	PCLK frequency [initial setting: f(CLK) × 8]
2	Dummy	---- ---0	0	Dummy/light-shielding pixels (initial setting: no readout)
19	pclk_delay[5:0]	---0 0000	0	PCLK timing (initial setting: pclk_delay[5:0]=0)
20	AGC[4:0]	---1 1101	29	Gain (initial setting: gain=1)
21 to 24	Offset 1 to 4[7:0]	1000 0000	128	Output offset (initial setting: Offset 1 to 4[7:0]=128)

Note: Be sure to set the addresses shown in the above table. Setting to the addresses not shown in the above table may cause errors.

Mode

It is possible to select pixel size and readout number of pixels, from the following three modes.
· Mode[1:0]=0: pixel size=7 × 7 µm, readout number of pixels=4096 pixels
· Mode[1:0]=1: pixel size=9.3 × 9.3 µm, readout number of pixels=3072 pixels
· Mode[1:0]=2: pixel size=14 × 14 µm, readout number of pixels=2048 pixels
The initial setting is 0. Do not set to Mode [1:0]=3.

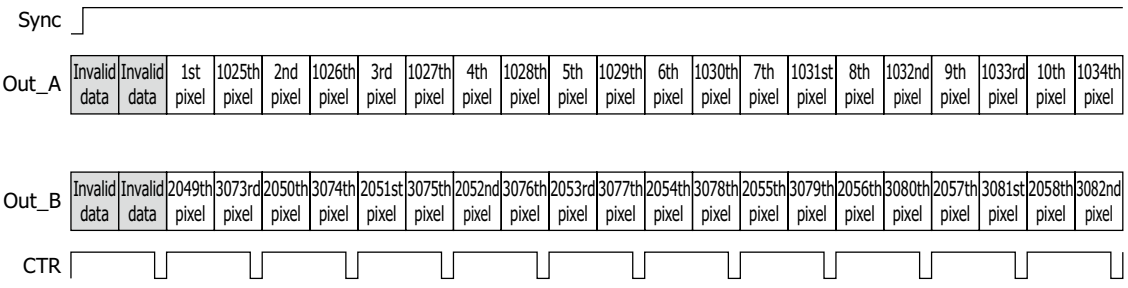
PCLK frequency

It is possible to select PCLK frequency from the following two settings.
· fpclk=0: PCLK = f(MCLK) × 8
· fpclk=1: PCLK = f(MCLK) × 4

Readout of dummy pixels and light-shielding pixels (OB pixels)

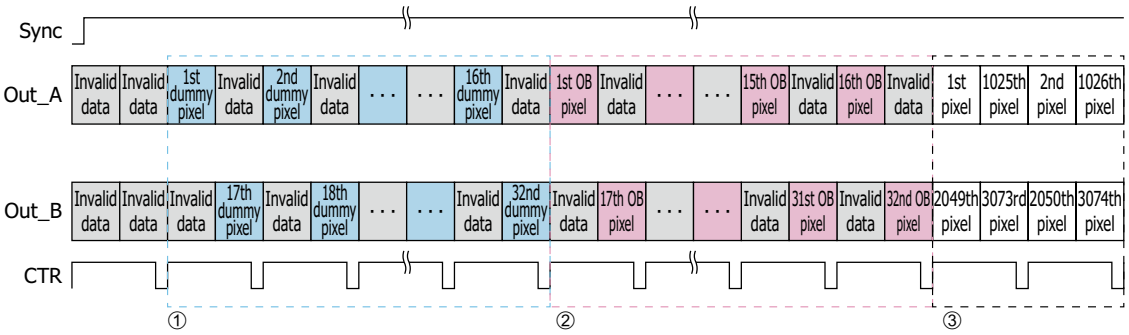
By setting Dummy, it is possible to select readout of dummy pixels and light-shielding pixels.
· Dummy=0: No readout of dummy pixels and light-shielding pixels
· Dummy=1: Output in the order of dummy pixels and light-shielding pixels before outputting effective pixels

Mode[1:0]=0, Dummy=0



KMPDC0921EA

Mode[1:0]=0, Dummy=1



① From Out_A, the 1st to 16th dummy pixels are read out sequentially.
From Out_B, the 17th to 32nd dummy pixels are read out sequentially.

② From Out_A, the 1st to 16th OB pixels are read out sequentially.
From Out_B, the 17th to 32nd OB pixels are read out sequentially.

③ After the dummy and OB pixels are read out, effective pixels are read out in sequence.

KMPDC0922EA

■ PCLK timing

PCLK can be delayed inside the sensor and output.
Increasing pclk_delay [5: 0] by 1 delays output of PCLK by about 0.15 ns.

■ Gain setting

The sensor may not operate properly if a setting not in the following table is specified. Specify a setting shown in the table.

AGC[4:0]						Gain	Description
Decimal	Binary						
	[4]	[3]	[2]	[1]	[0]		
2	0	0	0	1	0	8	
4	0	0	1	0	0	4	
12	0	1	1	0	0	2	
29	1	1	1	0	1	1	Initial setting

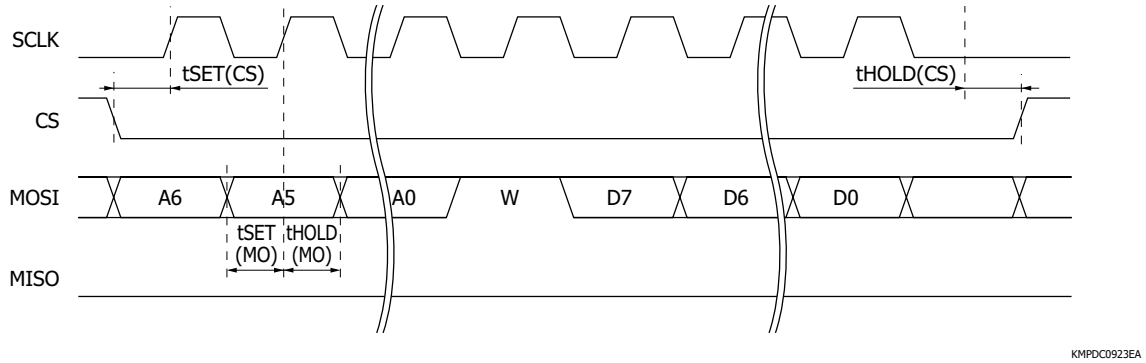
■ Output offset settings

Output offset value can be adjusted by setting Offset 1 to 4[7:0]. The default value is 128. When Offset is increased by 10, the offset value increases by about 1 DN. Pixels set differ according to addresses 21 to 24.
· Address 21: 1st pixel to M th pixel
· Address 22: M + 1 th pixel to 2 × M th pixel
· Address 23: 2 × M + 1 th pixel to 3 × M th pixel
· Address 24: 3 × M + 1 th pixel to 4 × M th pixel

Note: M=1024 (pixel size: 7 × 7 μm), 768 (pixel size: 9.3 × 9.3 μm), 512 (pixel size: 14 × 14 μm)

SPI settings

Set the SPI using SCLK, CS, and MOSI.



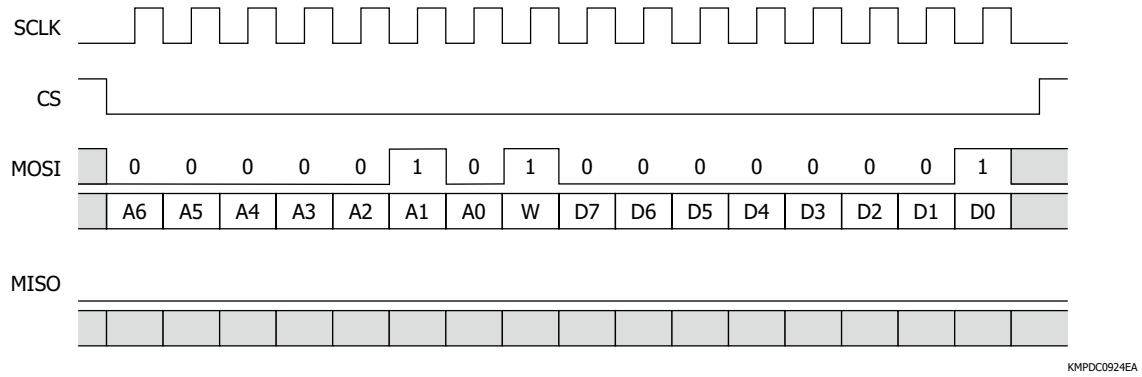
Note: Set SCLK to low when CS is on falling/rising edges.

[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency	f(SCLK)	-	7.5	10	MHz
SPI setup time (CS)	tSET(CS)	7	-	-	ns
SPI hold time (CS)	tHOLD(CS)	7	-	-	ns
SPI setup time (MOSI)	tSET(MO)	7	-	-	ns
SPI hold time (MOSI)	tHOLD(MO)	7	-	-	ns

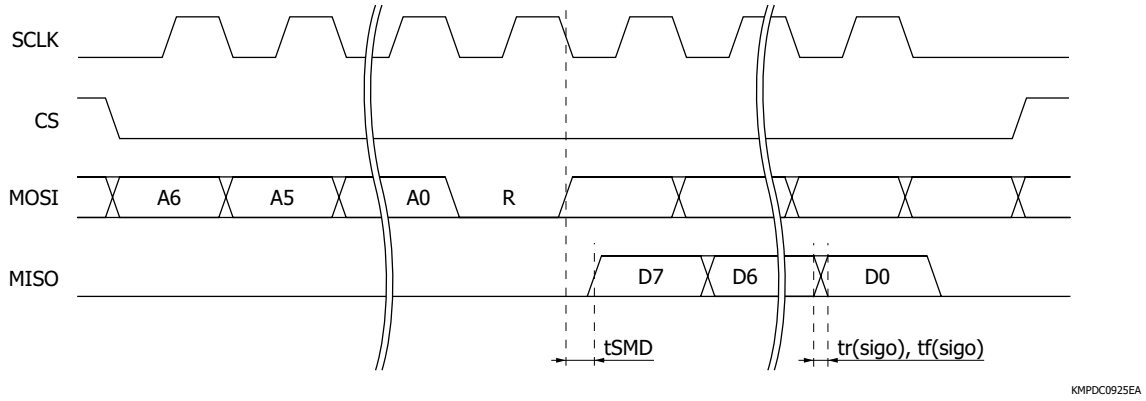
■ SPI setting example

Writing 0x01 to address 0x02



Checking the SPI setting

You can check the current SPI setting in the following manner.



Note: Set SCLK to low when CS is on falling/rising edges.

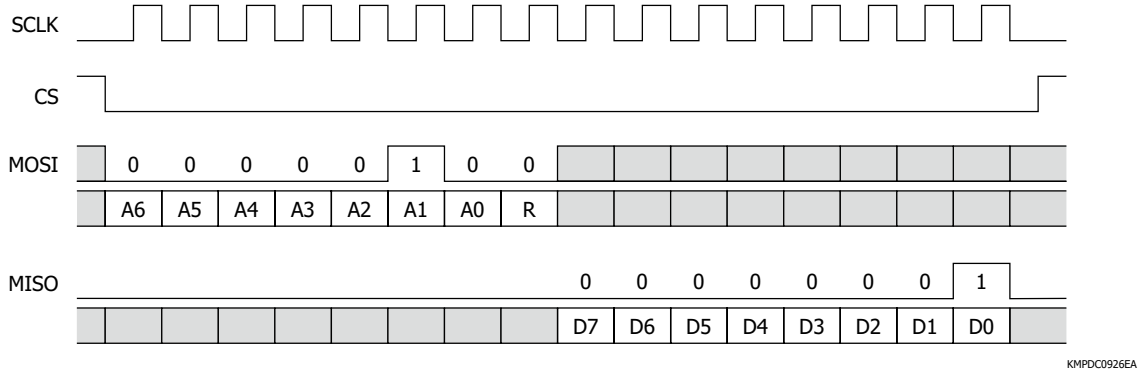
[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output signal rise time*21	tr(sigo)	-	10	12	ns
Output signal fall time*21	tf(sigo)	-	10	12	ns
Delay between SCLK and MISO output	tSMD	-	-	25	ns

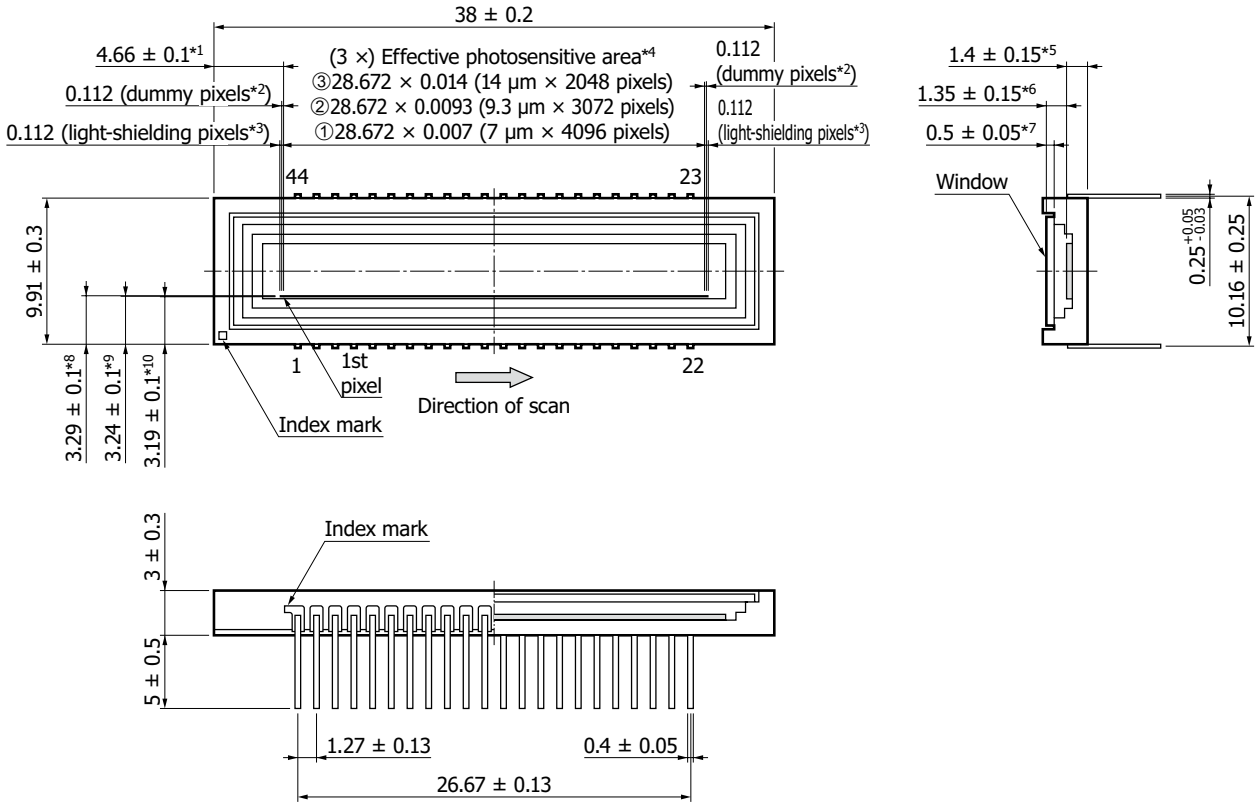
*21: Time for the output voltage to rise or fall between 10% and 90% when the load capacitance of the output terminal is 10 pF.

■ Example of checking the SPI setting

Check the value set with address 0x02



Dimensional outline (unit : mm)



Tolerance unless otherwise noted: ±0.2
*1: Distance from package edge to photosensitive area edge
*2: Pixels on the left and right outside of the effective pixels
*3: Pixels on the left and right outside of the dummy pixels
*4: See the enlarged view of effective photosensitive area (P.16) for details
*5: Distance from package bottom to photosensitive surface
*6: Distance from glass surface to photosensitive surface
*7: Glass thickness
*8: Distance from package edge to photosensitive area ③ center
*9: Distance from package edge to photosensitive area ② center
*10: Distance from package edge to photosensitive area ① center

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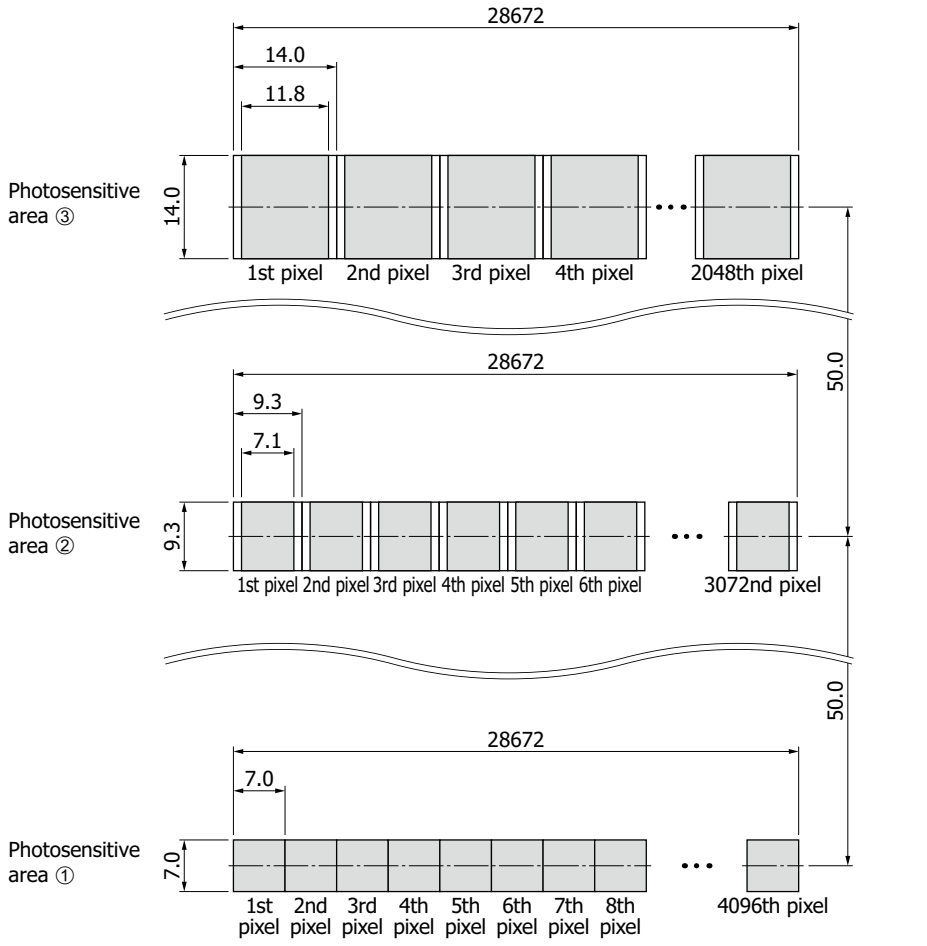
Enlarged view of effective photosensitive area (unit: µm)



Pin connections

Pin no.	Symbol	Function	I/O	Pin no.	Symbol	Function	I/O
1	MISO	SPI output signal	O	23	Vref1	Bias voltage*22	O
2	SCLK	SPI clock signal	I	24	Out_Bp[0]	Video output signal (LVDS)	O
3	RSTB	SPI reset signal	I	25	Out_Bn[0]	Video output signal (LVDS)	O
4	MOSI	SPI input signal	I	26	Out_Bp[1]	Video output signal (LVDS)	O
5	CS	SPI enable signal	I	27	Out_Bn[1]	Video output signal (LVDS)	O
6	MST	Master start signal	I	28	Out_Bp[2]	Video output signal (LVDS)	O
7	All_Reset	Timing generator reset signal	I	29	Out_Bn[2]	Video output signal (LVDS)	O
8	MCLK	Master clock signal	I	30	PCLKn	Bit output sync signal (LVDS)	O
9	PLL_Reset	Multiplication/divider circuit reset signal	I	31	PCLKp	Bit output sync signal (LVDS)	O
10	TGCLK	Timing generator clock signal	O	32	CTRn	Pixel sync signal (LVDS)	O
11	GND	Ground	-	33	CTRp	Pixel sync signal (LVDS)	O
12	Vdd(D)	Supply voltage (3.3 V)	I	34	Syncn	Frame sync signal (LVDS)	O
13	GND	Ground	-	35	Syncp	Frame sync signal (LVDS)	O
14	Vdd(D)	Supply voltage (3.3 V)	I	36	Out_Ap[0]	Video output signal (LVDS)	O
15	GND	Ground	-	37	Out_An[0]	Video output signal (LVDS)	O
16	Vdd(D)	Supply voltage (3.3 V)	I	38	Out_Ap[1]	Video output signal (LVDS)	O
17	GND	Ground	-	39	Out_An[1]	Video output signal (LVDS)	O
18	Vdd(A)	Supply voltage (3.3 V)	I	40	Out_Ap[2]	Video output signal (LVDS)	O
19	GND	Ground	-	41	Out_An[2]	Video output signal (LVDS)	O
20	Vdd(A)	Supply voltage (3.3 V)	I	42	Vref2	Bias voltage*22	O
21	GND	Ground	-	43	Vref_cp2	Bias voltage for charge pump circuit (-1.5 V)*22	O
22	Vdd(A)	Supply voltage (3.3 V)	I	44	Vref_cp1	Bias voltage for charge pump circuit (5.5 V)*22	O

*22: Insert a 1 µF capacitor between Vref and GND.
Note: Leave NC pins open; do not connect to GND.

Note: The video output symbols are defined as follows:

Out_An[0]
- [0]: 0to 3-bit, [1]: 4 to 7-bit, [2]: 8 to 11-bit
- p: positive input of the differential pair, n: negative input of the differential pair
- A to B: output ports

Recommended soldering conditions

Parameter	Specification	Note
Soldering temperature	260 °C max. (within 5 seconds)	

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

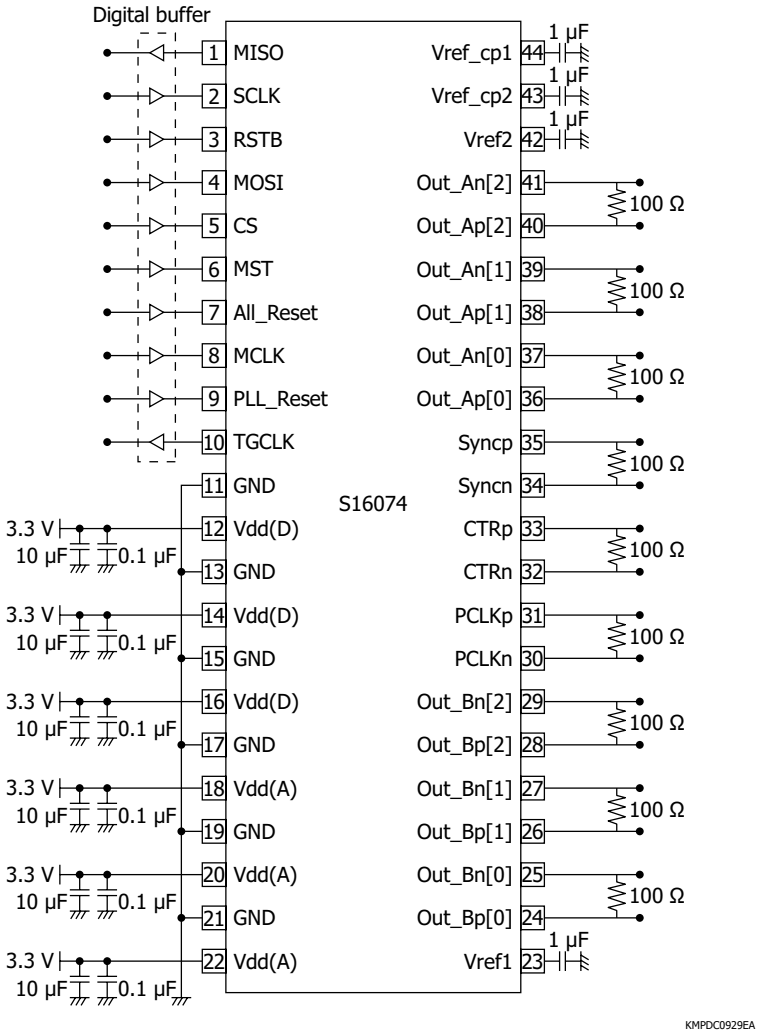
Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench, and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Input window
If dust or stain adheres to the surface of the input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) UV light irradiation
Because this product is not designed to resist characteristic deterioration under UV light irradiation, do not apply UV light irradiation to it.

Connection circuit example



Note: Digital buffer is not necessary when MISO and TGCLK are not used.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical note
· CMOS linear image sensors

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