SymPol™ Transceiver

Check for Samples: SN65HVD96

FEATURES

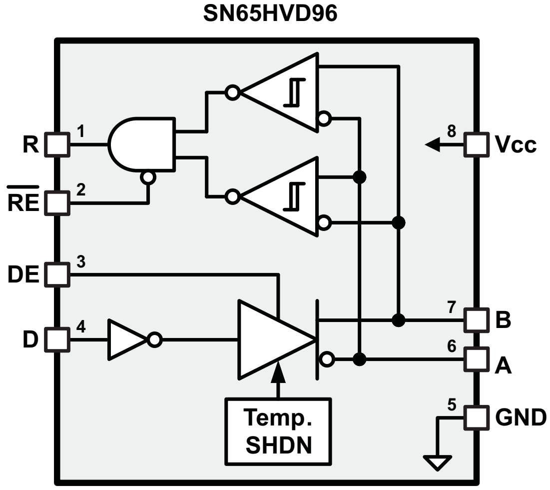
- **Communicate Without Errors on Normal or Reversed-Wire Bus Lines**
- **Up to 5 Mbps Signaling**
- **Industrial Temperature Range: –40°C to 85°C**
- **Symmetric Polarity Receiver Thresholds ≥ 100 mV Receiver Hysteresis**
- **Connect up to 32 Nodes on one Bus**
- **Transient Protection**
  - **±12 kV Human Body Model on Bus Pins**
  - **±25 V Repetitive Transient Pulse on Bus Pins**
- **Additional Reliability Features:**
  - **Bus Standoff From –35 V to 40 V**
  - **Driver Output Short-Circuit Current Limit**
  - **Automatic Thermal Shutdown and Recovery**

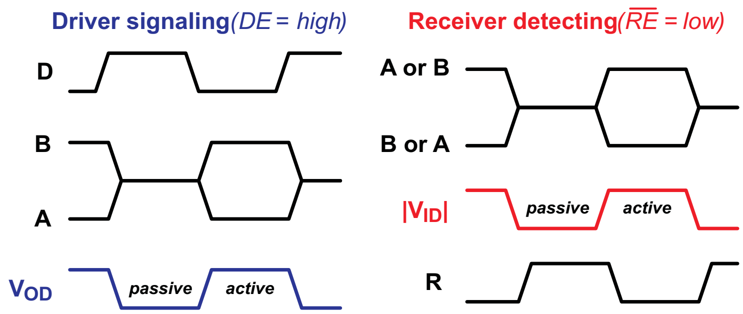
DESCRIPTION

The SN65HVD96 is specifically designed to meet the requirements for a transceiver which operates with no errors if the twisted-pair signal wires are connected normally or reversed. This allows for error free operation in applications where the signal wires may become inadvertently reversed during installation or maintenance. This feature is corrected internally so no intervention from the controller or operator is required.

Similar to RS-485, these transceivers can be used for point-to-point, multi-drop, or multi-point networks. Sympol™ devices are not backwards compatible with, but are an upgrade to, existing RS-485 networks. The pin-out is identical to the industry-standard SN75176 transceiver, allowing direct upgrade from RS-485 to SymPol. Current-limited differential outputs protect in case of driver contention on a *party-line* bus. High receiver input impedance allows connection of at least 32 nodes. Several fault tolerant features are integrated into the device from operational hazards. Current limiting on the driver outputs protects against short-circuit faults, and operates independently on each driver output. An automatic thermal shutdown protects the driver circuits against over temperature conditions. The receiver output enters a deterministic *failsafe* state if the bus connection is left disconnected or if the bus wires are shorted together.

The small outline integrated circuit (SOIC) package saves board space compared to equivalent discrete implementations. These devices are fully characterized for operation over the industrial temperature range of –40°C to 85°C.





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ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
Supply voltage, V_{CC}	–0.5 to 7	V
Voltage range at A or B	–35 to 40 dc	V
Voltage range at logic pins (D, DE, $\overline{RE}$)	–0.3 to V_{CC}+0.3	V
Voltage input range, transient pulse, A and B, through 100Ω	±25 dc	V
Voltage input transient pulse, A and B, per ISO 7637	±200	V
Electro-static discharge per JEDEC Std. 22 A114 A and B, Human Body Model	±12	kV
Electro-static discharge per JEDEC Std. 22 A114 all pins, Human Body Model	±5	kV
Electro-static discharge per JEDEC Std. 22 C101 all pins, Charged Device Model	±2	kV
Electro-static discharge per JEDEC Std. 22 A115 all pins, Machine Model	±200	V
Receiver output current	±20	mA
Junction temperature, T_J	170	°C
Continuous total power dissipation	(see Dissipation Rating Table)	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)			SN65HVD96	UNITS
			8 PINS SOIC	
θ_{JA}	Junction-to-ambient thermal resistance(2)		124.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)		55.9	
θ_{JB}	Junction-to-board thermal resistance (4)		50.2	
ψ_{JT}	Junction-to-top characterization parameter (5)		4.9	
ψ_{JB}	Junction-to-board characterization parameter (6)		46.0	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)		n/a	
		TEST CONDITIONS		
P_d	Power Dissipation	VCC = 5.25 V, TJ = 150°C, RL = 300 Ω, CL = 50 pF (driver), CL = 15 pF (receiver) 290 5-V supply, unterminated(8)	188	mW
		VCC = 5.25 V, TJ = 150°C, RL = 100 Ω, CL = 50 pF (driver), CL = 15 pF (receiver) 5-V supply, RS-422 load(8)	251	
		VCC = 5.25 V, TJ = 150°C, RL = 54 Ω, CL = 50 pF (driver), CL = 15 pF (receiver) 5-V supply, RS-485 load(8)	319	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(8) Driver and receiver enabled, 50% duty cycle square-wave signal at 5 Mbps.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_I	Input voltage at any bus terminal (separately or common mode)[(1)]	–7		12	V
V_{IH}	High-level input voltage (Driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (Driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	–12		12	V
I_O	Output current, Driver	–70		70	mA
I_O	Output current, Receiver	–2		2	mA
R_L	Differential load resistance	54	60		Ω
$1/t_{UI}$	Signaling rate	0		5	Mbps
T_A	Operating free-air temperature	–40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD(ACT)}\|$	Driver differential output voltage magnitude (active)	RS-485 common-mode load, see Figure 2		1.5			V
		RS-485 differential load R_L = 54 Ω, C_L = Open, see Figure 3		1.5			
		RS-422 differential load R_L = 100 Ω, C_L = Open, see Figure 3		2			
$\|V_{OD(PAS)}\|$	Driver differential output voltage magnitude (passive)	RS-485 common-mode load, See Figure 2				50	mV
		RS-485 differential load R_L = 54 Ω, C_L = Open, see Figure 3				20	
		RS-422 differential load R_L = 100 Ω, C_L = Open, see Figure 3				25	
		No Load				50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	$Voc = (V_A + V_B) / 2$ $R_L = 54Ω$		1	Vcc/2	3	V
$ΔV_{OC}$	Change in differential driver output common-mode voltage	$Voc_{(D=High)} – Voc_{(D=Low)}$ $R_L = 54Ω$		–0.2		0.2	V
$V_{IT(ACT)}$	Active-going receiver differential input threshold	$V_{ID} = V_A – V_B$ or $V_{ID} = V_B – V_A$			775	900	mV
$V_{IT(PASS)}$	Passive-going receiver differential input threshold			500	625		mV
V_{HYS}	Receiver differential input threshold hysteresis (VIT(ACT) - VIT(PASS))			100	150		mV
V_{OH}	Receiver high-level output voltage	–20 µA ≥ I_O ≥ –2 mA		2.4		3.7	V
V_{OL}	Receiver low-level output voltage	20 µA ≤ I_O ≤ 2 mA				0.4	V
I_I	Logic pins input current			–100		100	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or Vcc, $\overline{RE}$ at Vcc		–10		10	uA
I_{OS}	Driver short-circuit output current	–7 V < Vo < +12 V		–350		350	mA
I_I	Bus input current (passive driver)	Vcc = 4.75 to 5.25 V or Vcc=0V, DE at 0V, other bus pin at 0V	V_I = 12 V			1	mA
			V_I = –7 V	–0.8			mA
I_{CC}	Supply current (quiescent), no load					20	mA

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{rise} , t_{fall}	Driver differential output rise/fall time	R_L= 54 Ω, C_L= 50 pF, See Figure 3		15	30	ns
t_{pAP} , t_{pPA}	Driver propagation delay			40	80	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{pAP} – t_{pPA}\|$			1	10	ns
t_{pZA}, t_{pAZ}	Driver enable/disable time	D = GND, R_L= 54 Ω, C_L= 50 pF, See Figure 4		50	80	ns
RECEIVER						
t_{rise}, t_{fall}	Receiver output rise/fall time	C_L= 15 pF, See Figure 5		8	15	ns
t_{PHL} , t_{PLH}	Receiver propagation delay time			70	90	ns
$t_{SK(P)}$	Receiver output pulse skew,$\|t_{PHL} – t_{PLH}\|$			5	15	ns
t_{PZL}, t_{PZH}, t_{PLZ}, t_{PHZ}	Receiver enable/disable time	See Figure 6		20	100	ns

FUNCTION TABLE

DRIVER	**DE**	**D**	**V_{OD}**	
	L or OPEN	X	Z	Driver Disabled (Passive)
	H	L	H	Driver Active
		H or Open	Z	Driver Passive
RECEIVER	**$\overline{RE}$**	**V_{ID}**	**R**	
	H or OPEN	X	Z	Receiver Disabled
	L	V_{ID} < –0.9 V	L	Active Bit Received
		–0.9 V < V_{ID} < –0.5	?	Indeterminate bus
		–0.5 V < V_{ID} < 0.5 V	H	Passive Bit Received
		0.5 V < V_{ID} < 0.9 V	?	Indeterminate bus
		0.9 V < V_{ID}	L	Active Bit Received
		Open, Short, Idle	H	Failsafe Condition

DEVICE INFORMATION

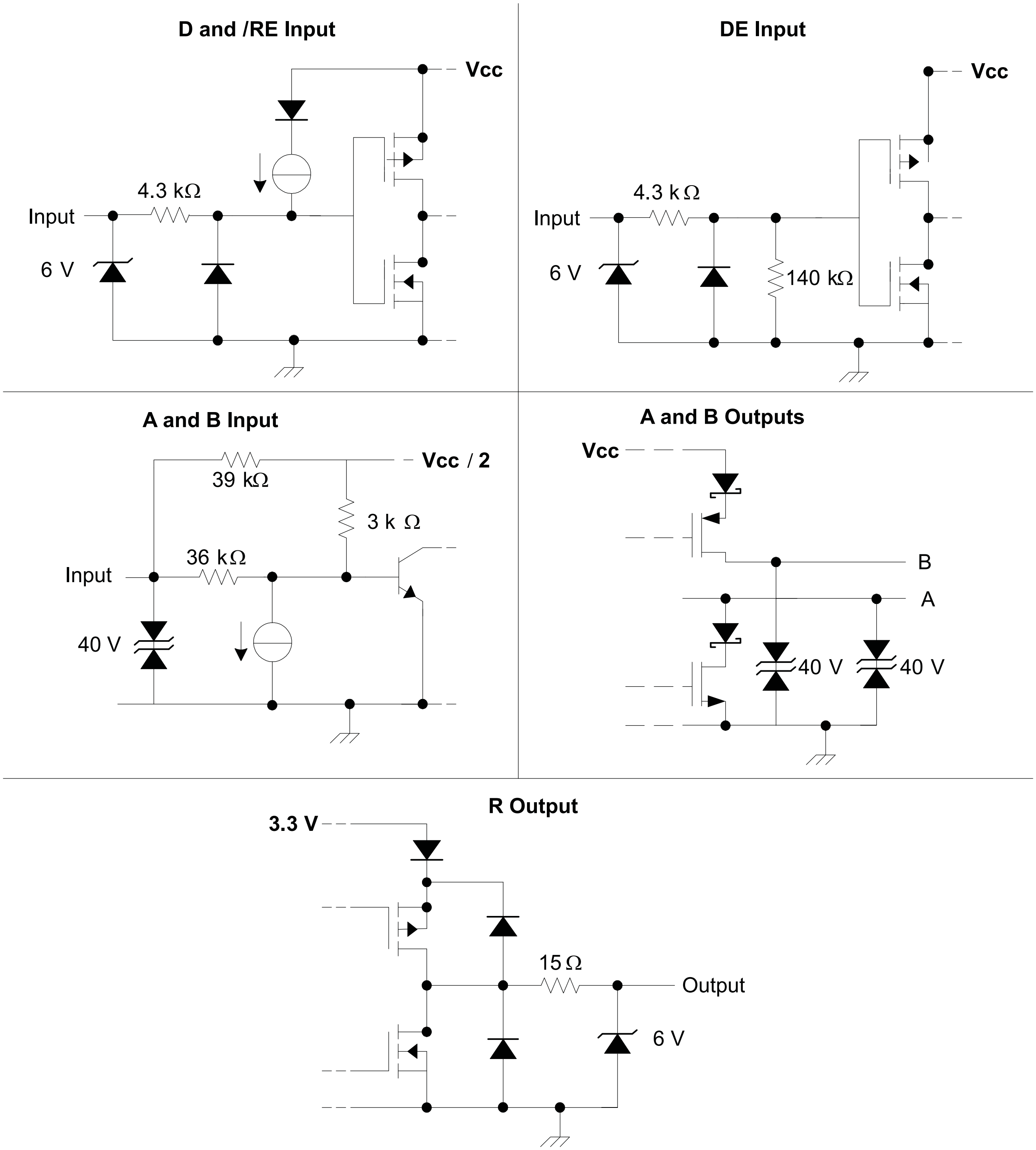
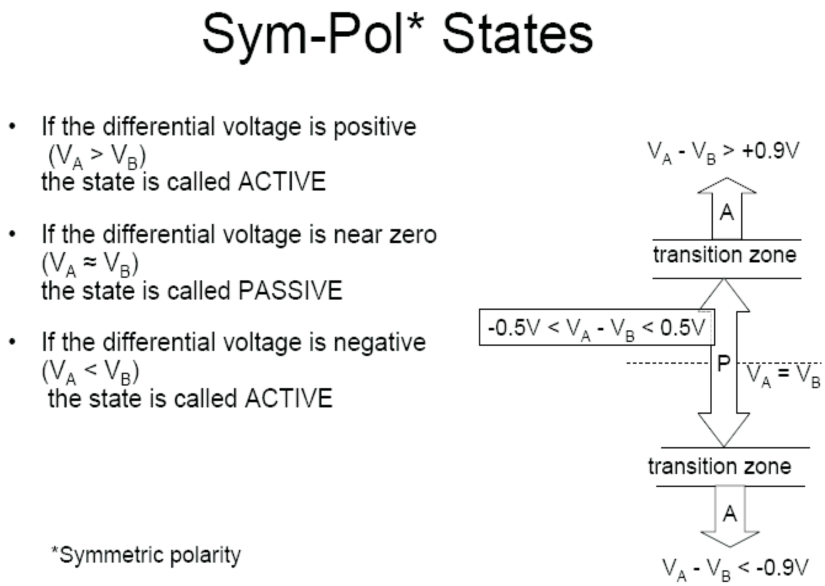


Figure 1. Equivalent Input and Output Schematic Diagrams

APPLICATION INFORMATION

Sympol™ States



Using Sympol to Achieve Immunity to Crossed Bus Wire

Many applications which use RS-422 or RS-485 are wired on-site by third-party installers. This opens the door to the possibility of miss-wiring, especially for far-flung networks with many stations (or nodes). Neither RS-422 nor RS-485 allows correct communications when the bus wires (typically a twisted-pair) are swapped.

The existing solutions for this case require active intervention, either by the installer or maintenance technician, or by an automated controller. Sympol offers a way to replace RS-422 or RS-485 networks with communication over the same bus lines. Due to the innovative nature of Sympol signalling levels, a Sympol network is immune to communication errors caused by crossed bus wires.

Signaling levels are similar to RS-422 and RS-485, so signalling rates, cable lengths, and noise immunity will be comparable.

Sympol is NOT interoperable with RS-422 or RS-485; that is, designers may not mix Sympol nodes with existing RS-485 nodes.

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100kbps, 50% duty-cycle, transition times less than 6 ns for all figures.

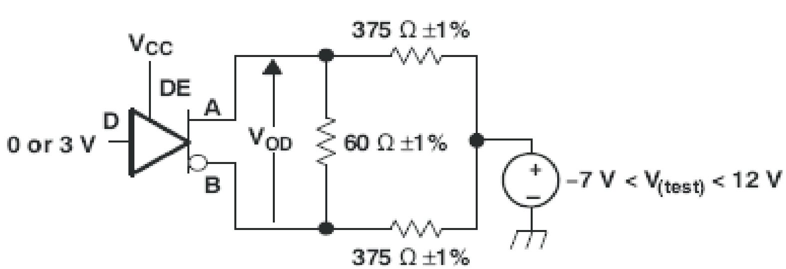


Figure 2. Measurement of Driver Differential Output Voltage With Common-Mode Load

PARAMETER MEASUREMENT INFORMATION (continued)

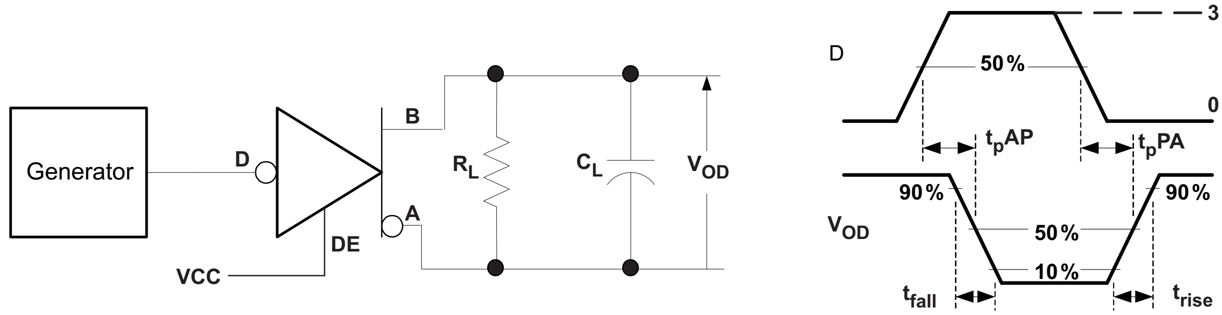


Figure 3. Measurements of Driver Differential Output Rise and Fall Times and Propagation delays

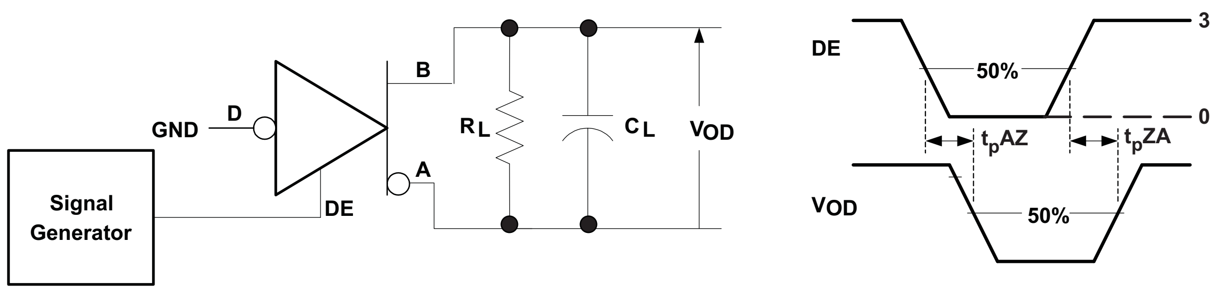


Figure 4. Measurements of Driver Enable and Disable Times With Active Output

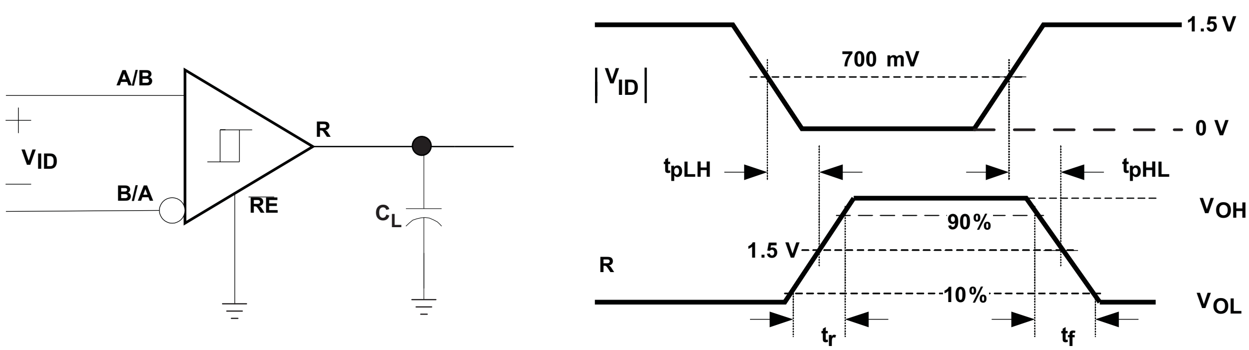


Figure 5. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

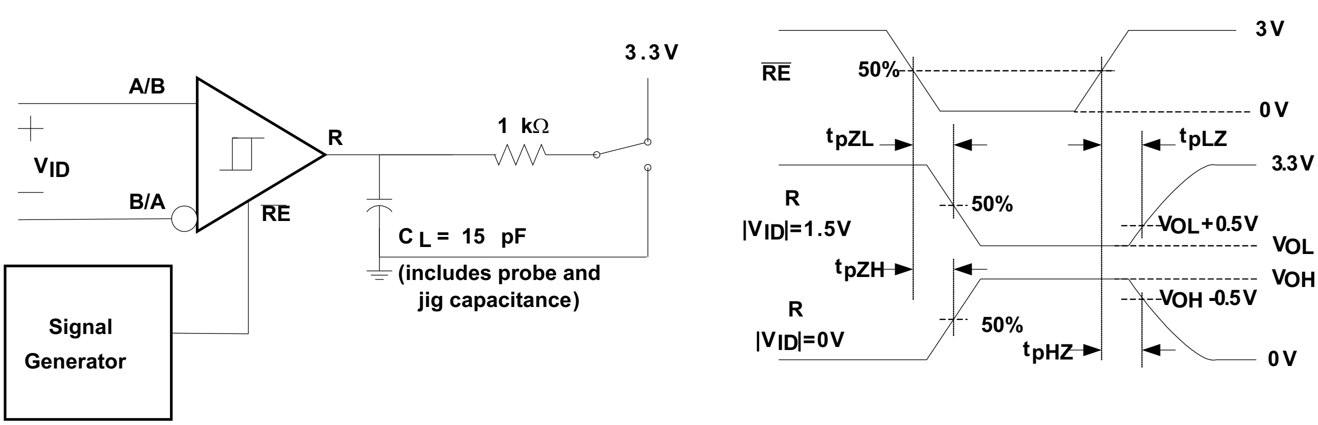


Figure 6. Measurement of Receiver Enable Times With Driver Disabled

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD96D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
SN65HVD96DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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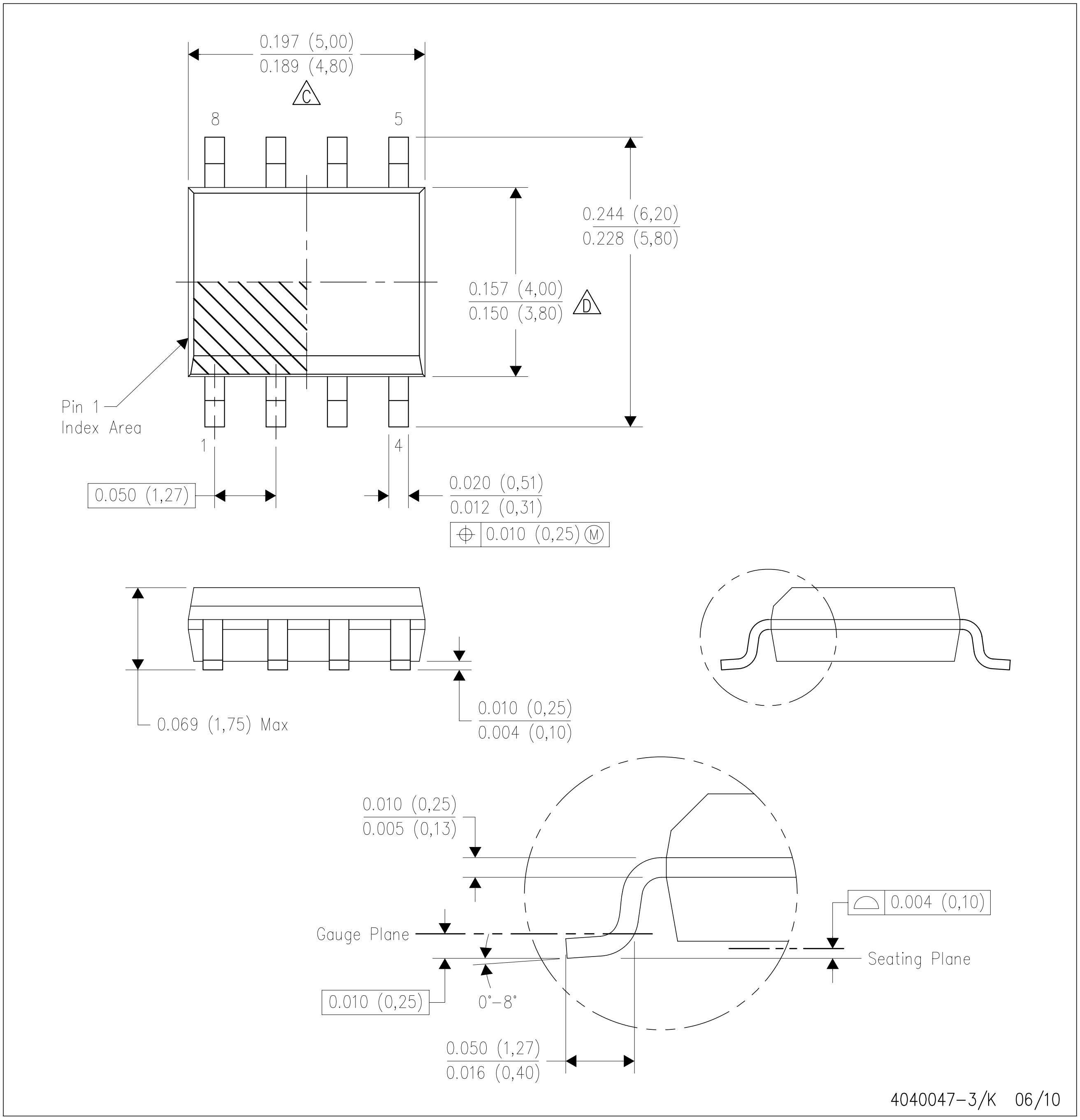
D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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