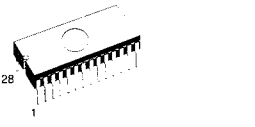
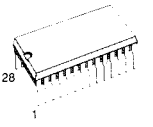
64K (8K x 8) CMOS UV EPROM - OTPROM

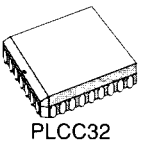
- FAST ACCESS TIME : 200 ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- 28-PIN JEDEC APPROVED PIN-OUT.
- LOW POWER CONSUMPTION :
  - ACTIVE 30mA Max
  - STANDBY 100µA Max
- PROGRAMMING VOLTAGE : 12.5V.
- HIGH SPEED PROGRAMMING (< 1 minute).
- ELECTRONIC SIGNATURE.



FDIP-28



PDIP-28



PLCC32

(Ordering information at the end of the datasheet)

DESCRIPTION

The TS27C64A is a high speed 65,536 bit UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The TS27C64A is housed in a 28 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIL or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A12	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O0-O7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NON CONNECTED

Figure 1 : Pin Connection

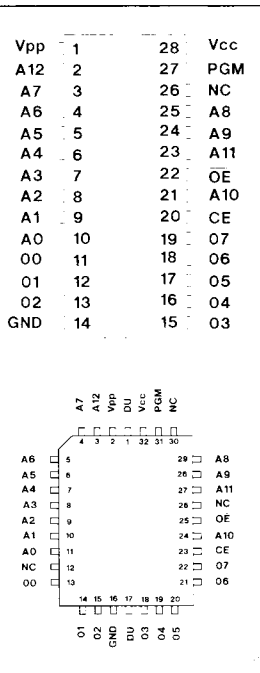
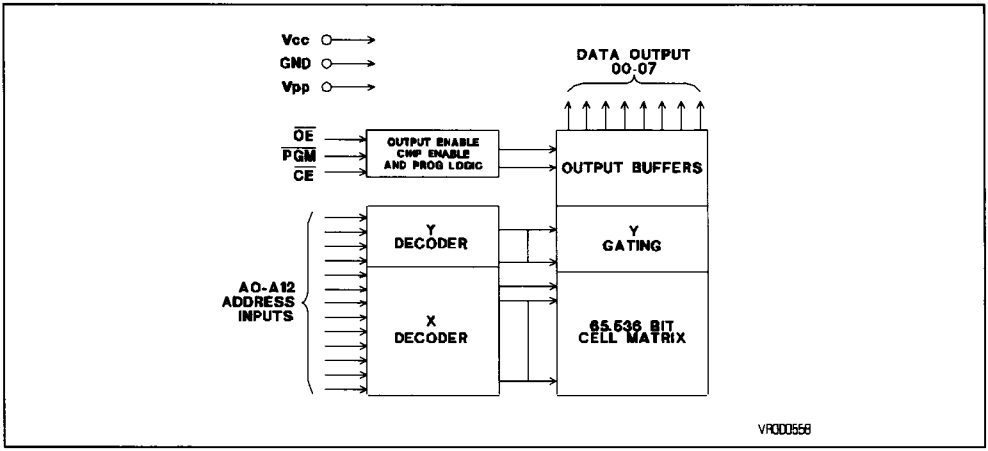


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Values	Unit
T_{AMB}	Operating temperature range TS27C64ACQ TS27C64AVQ	T_L to T_H 0 to +70 -40 to +85	°C
T_{STG}	Storage temperature range	-65 to +125	°C
V_{PP}(2)	Supply voltage	-0.6 to +14	V
V_{IN}(2)	Input voltages A9 Except V_{PP}, A9	-0.6 to +13.5 -0.6 to 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering : 10 seconds)	+300	°C

NOTES : 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except to "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to GND.

OPERATING MODES

MODE	PINS						
	$\overline{CE}$	OE	A9	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	CODE

NOTES : 1. X can be either V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code : 9B) to V_{IH} (type code : 08).

READ OPERATION

DC CHARACTERISTICS

(T_{AMB} = T_L to T_H, V_{CC} = 5V ± 10%, V_{SS} = 0V. Unless otherwise specified) (5)

Symbol	Parameter	Test Conditions	Values			Unit
			Min	Typ(1)	Max	
I_{LI}	Input Load Current	V_{IN} = V_{CC} or GND			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS} $\overline{CE}$ = V_{IH}			10	µA
V_{PP}	V_{PP} Read voltage		V_{CC} - 0.7		V_{CC}	V
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA I_{OL} = 0 µA			0.45 0.1	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = 0 µA	2.4 V_{CC}-0.1			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE}$=$\overline{OE}$=V_{IL}, Inputs=V_{IH} or V_{IL}, f = 5 MHz, I/O = 0mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	$\overline{CE}$ = V_{IH}		0.5	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$\overline{CE}$ = V_{CC}		10	100	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC} = 5.5V			100	µA

NOTE : 1. Typical conditions are for operation at : T_{AMB} = +25°C, V_{CC} = 5V, V_{PP} = V_{CC} and V_{SS} = 0V

AC CHARACTERISTICS(1)

(T_{AMB} = T_L to T_H)(5)

Symbol	Parameter	Test condition	27C64A						Unit
			-20		-25		-30		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$= $\overline{OE}$=V_{IL}		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		80		100		120	ns
t_{DF}(2,4)	$\overline{OE}$ or $\overline{CE}$ High to Output Float		0	50	0	60	0	105	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		ns

CAPACITANCE

T_{AMB} = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Test Condition	Min	Typ.(2)	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. V_{PP} may be connected to V_{CC} except during program.
2. The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured $V_{OH}^{(DC)}$ -0.1V
Low to THREE-STATE the measured $V_{OL}^{(DC)}$ + 0.1V.
3. Capacitance is guaranteed by periodic testing. T_{AMB} = +25°C, f=1MHz.
4. T_{DF}, is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first. This parameter is only sampled and not 100 % tested.
5. All parameters are specified at V_{CC} = 5V ± 5% for 27C64-20X, 27C64-25X and 27C64-30X.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Reference Level :	
Input pulse levels	:	0.45V to 2.4V	Inputs : 0.8V and 2V - Outputs : 0.8V and 2V	

Figure 3 : AC Testing Input/Output Waveform

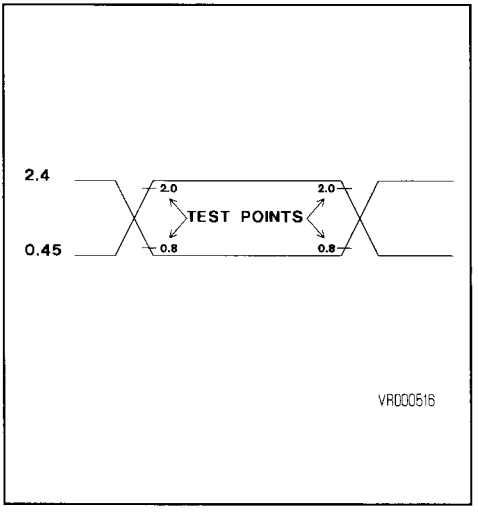


Figure 4 : AC Testing Load Circuit

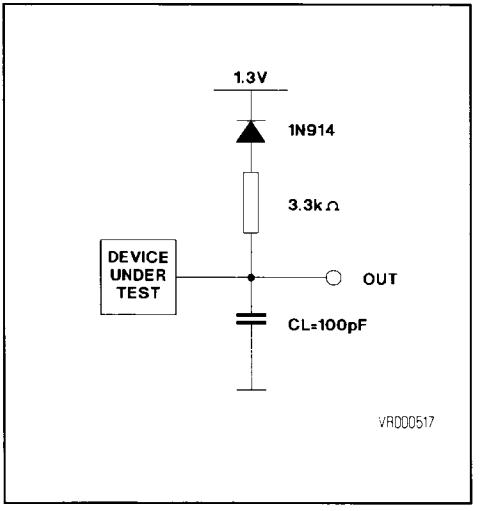
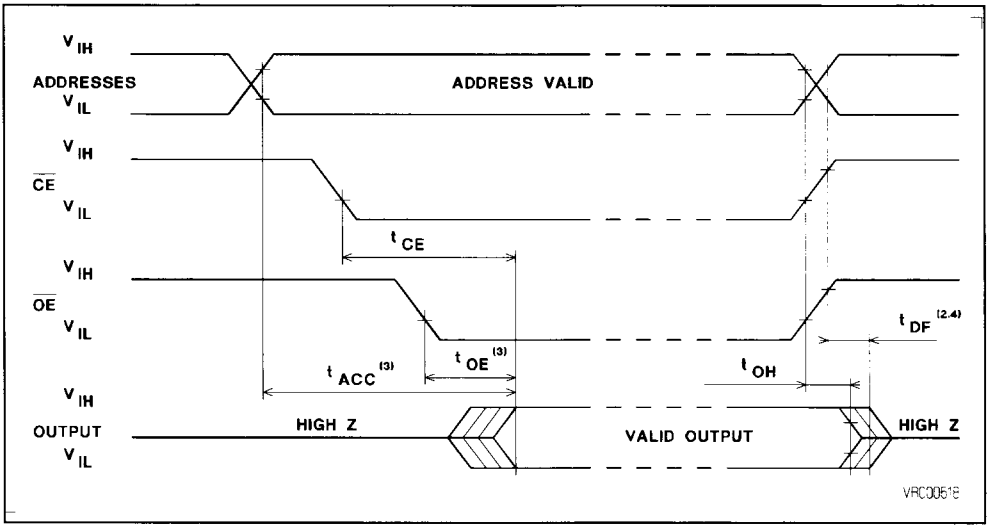


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - $t\overline{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the TS27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 in electronic signature mode.

READ MODE

The TS27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The TS27C64A has a standby mode which reduces the maximum power dissipation to 5.5mW. The TS27C64A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is required from a particular memory device.

PROGRAMMING MODES

Caution : Exceeding 14V on V_{PP} will damage the TS27C64A.

Initially, (and after each erasure for UV EPROM), all bits of the TS27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C64A is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. To avoid damage to the device from spurious voltage transients, a 0.1 µF filter capacitor must be placed accross V_{PP}, V_{CC} and ground. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled TS27C64As.

HIGH SPEED PROGRAMMING

The high speed programming algorithm described in the flowchart rapidly programs the TS27C64A using an efficient and reliable method particularly suited to the production programming environment. An individual device will take around 1 minute to program.

PROGRAM INHIBIT

Programming of multiple TS27C64As in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64As from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64As may be common. A TTL low-level pulse applied to a TS27C64A $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at 12.5V will program that TS27C64A.

PROGRAM VERIFY

A verify may be performed on the programmed bits to ensure that they were correctly programmed. The verify routine is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will identify the EPROM manufacturer and type.

This mode is intended for use with programming equipment in oder to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64A. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 of the TS27C64A. Two bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

ERASING (applies for UV EPROM)

The TS27C64A is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C64A be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces I_{CC} due to photodiode currents. An ultraviolet source of 2537A yielding a total integrated dosage of 15 watt seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 $\mu W/cm^2$ power rating is used. The TS27C64A to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PROGRAMMING OPERATIONS(1)

(T_{AMB} = 25 ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (all inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low voltage during verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High voltage during verify	I_{OH} = -400 µA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				30	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Set-up time		2			µs
t_{OES}	$\overline{OE}$ Set-up Time		2			µs
t_{DS}	Data Set-up Time		2			µs
t_{AH}	Address Hold time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			µs
t_{VCS}	V_{CC} set-up time		2			µs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}(2)	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{CES}	$\overline{CE}$ set-up time		2			µs
t_{OE}	Data valid from $\overline{OE}$				150	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

AC TEST CONDITIONS

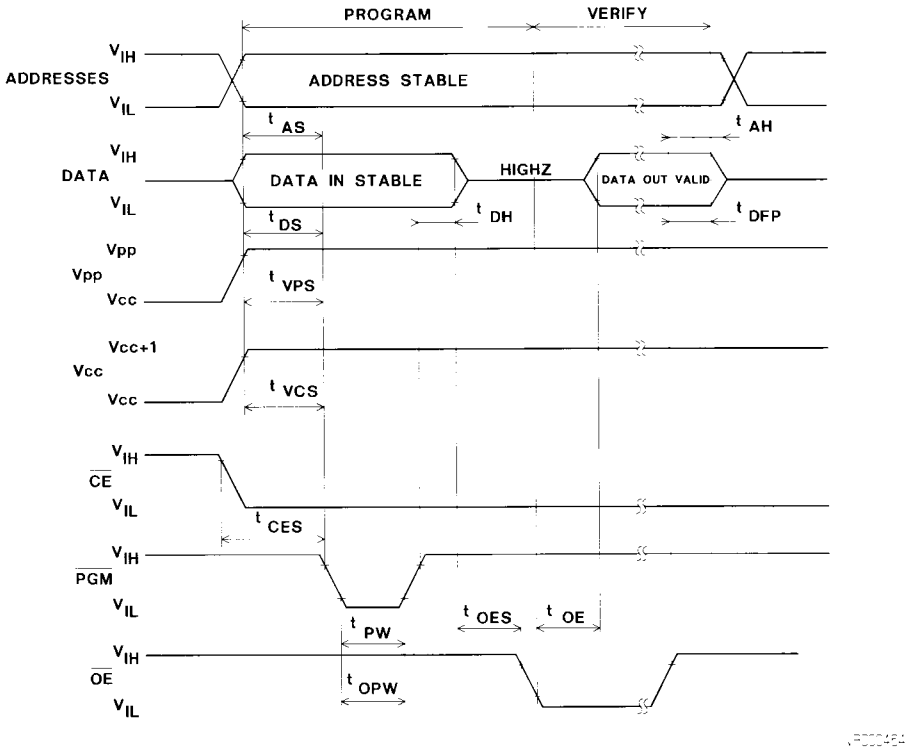
Input rise and fall times (10% to 90%) : ≤ 20ns

Input pulse levels : 0.45V to 2.4V

Timing reference levels :

Inputs : 0.8V and 2.0V - Outputs : 0.8V and 2.0V

Figure 6 : High Speed Programming Waveforms

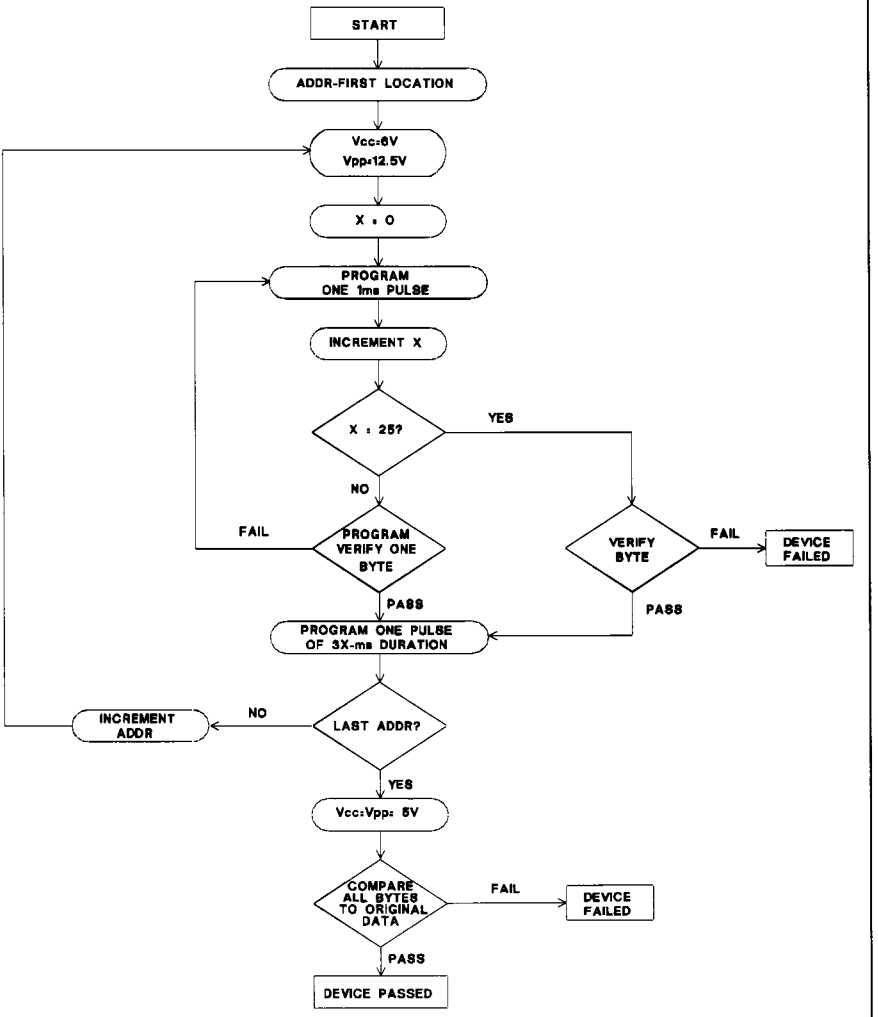


NOTES : 1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

3. When programming the TS27C64A, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 7 : High Speed Programming Flow Chart

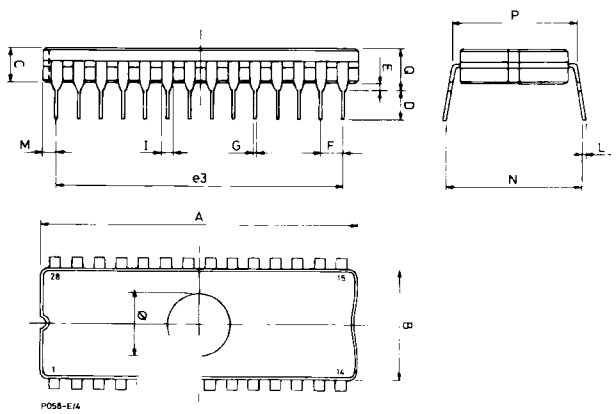


ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-20XCQ	200 ns	5V ± 5%	0°C to + 70°C	FDIP-28
TS27C64A-25XCQ	250 ns	5V ± 5%	0°C to +70°C	FDIP-28
TS27C64A-30XCQ	300 ns	5V ± 5%	0°C to + 70°C	FDIP-28
TS27C64A-20CQ	200 ns	5V ± 10%	0°C to + 70°C	FDIP-28
TS27C64A-25CQ	250 ns	5V ± 10%	0°C to + 70°C	FDIP-28
TS27C64A-30CQ	300 ns	5V ± 10%	0°C to + 70°C	FDIP-28
TS27C64A-20VQ	200 ns	5V ± 10%	-40°C to + 85°C	FDIP-28
TS27C64A-25VQ	250 ns	5V ± 10%	-40°C to + 85°C	FDIP-28
TS27C64A-30VQ	300 ns	5V ± 10%	-40°C to + 85°C	FDIP-28

PACKAGE MECHANICAL DATA

Figure 8 : 28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

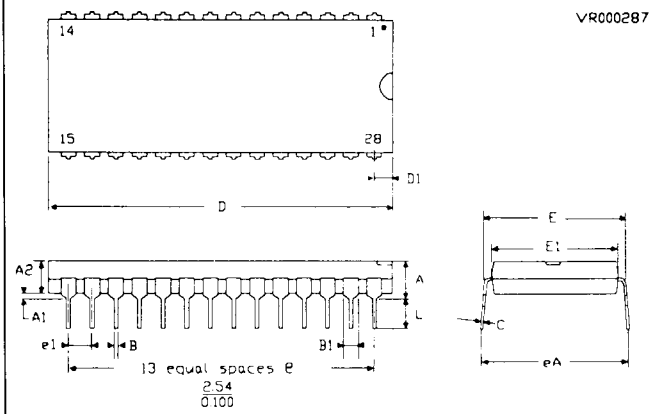
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-20CP	200 ns	5V ± 10%	0°C to + 70°C	PDIP28
TS27C64A-25CP	250 ns	5V ± 10%	0°C to + 70°C	PDIP28
TS27C64A-20VP	200 ns	5V ± 10%	-40°C to + 85°C	PDIP28
TS27C64A-25VP	250 ns	5V ± 10%	-40°C to + 85°C	PDIP28
TS27C64A-35TP(1)	350 ns	5V ± 10%	-40°C to + 105°C	PDIP28
TS27C64A-20CFN	200 ns	5V ± 10%	0°C to + 70°C	PLCC32
TS27C64A-25CFN	250 ns	5V ± 10%	0°C to + 70°C	PLCC32
TS27C64A-20VFN	200 ns	5V ± 10%	-40°C to + 85°C	PLCC32
TS27C64A-25VFN	250 ns	5V ± 10%	-40°C to + 85°C	PLCC32

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.
(1) Specification available upon request.

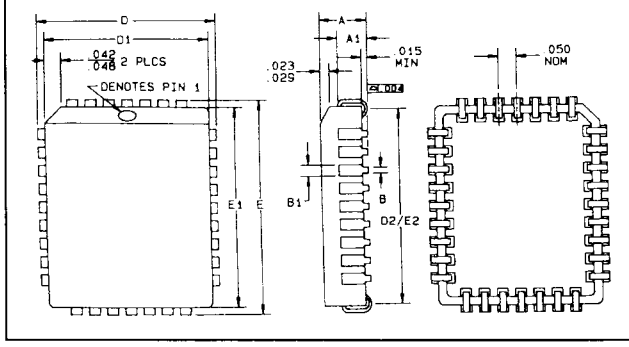
PACKAGE MECHANICAL DATA - OTP ROM

Figure 9 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e3		33.02			1.300	
e4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	

Figure 10 : PLCC32 32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04		3.55	.120		.140
A1	1.96		2.41	.078		.095
B	0.33		0.53	.013		.021
B1	0.66		0.81	.026		.032
D	12.31		12.57	.485		.495
D1	11.35		11.50	.447		.453
D2	9.90		10.92	.390		.430
E	14.85		15.11	.585		.595
E1	13.89		14.04	.547		.553
E2	12.44		13.46	.490		.530