AU6850B Datasheet

USB Host MP3 Decoder SOC

Rev 0.1

Sep 11, 2008

DISCLAIMER

All information and data contained in this document are without any commitment, are not to be considered as an offer for conclusion of a contract, nor shall they be construed as to create any liability. Any new issue of this document invalidates previous issues. Product availability and delivery are exclusively subject to our respective order confirmation form; the same applies to orders based on development samples delivered. By this publication, Shanghai Mountain View Silicon Technology Co. Ltd.("MVSILICON") does not assume responsibility for patent infringements or other rights of third parties that may result from its use.

No part of this publication may be reproduced, photocopied, stored in a retrieval system, or translated in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without the prior written permission of Shanghai Mountain View Silicon Technology Co. Ltd.

Shanghai Mountain View Silicon Technology Co. Ltd. assumes no responsibility for any errors contained herein.

Revision History

Data	Revision	Description
2008-9-11	0.1	initial

Contents

Revision History iii
Contents iv
Figures v
Tables vi
1. Overview 1
    1.1 Features 1
    1.2 Chip Architecture 1
2. System Application 2
3. Pin Description 3
    3.1 Pin Description 3
4. Package 5
    4.1 Package Diagram 5
    4.2 Package Dimension Parameter 6
5. Electrical Specification 7
    5.1 Absolute Maximum Ratings (Note 1) 7
    5.2 Recommended Operating Conditions 7
    5.3 Electrical Characteristics 7
Contact Information 8

Figures

Figure 1 AU6850B Functional Block Diagram 1
Figure 2 MP3 Audio System 2
Figure 3 Package Diagram (LQFP64-10x10mm / TOP View) 5
Figure 4 LQFP64-10x10mm Package Dimension Parameter 6

Tables

Table 1 Pin Description 3
Table 2 Absolute Maximum Ratings 7
Table 3 Recommended Operating Conditions 7
Table 4 Electrical Characteristics 7

1. Overview

A highly integrated SOC for MP3 player, AU6850B integrates MCU, MP3 decoder, USB Host controller, SD/MMC card controller, a 16-bit audio decoder and an IR decoder in a single chip. Compared with traditional flash-MP3 player, AU6850B offers a lower cost, lower power consumption, flexible and more powerful host MP3 player solution.

1.1 Features

- Low power 0.18um CMOS technology
- Power supply 1.8V/3.3V, power consumption 85mw
- Enhanced 8051, up to 10 times faster than standard 8051
- Dynamic MCU running clock frequency adjustment to reduce power consumption and EMI
- USB2.0 full-speed host controller
- SD/MMC card controller
- Support MPEG 1/2/2.5 layer2/3 decoding, data rate 32kbps ~ 320kbps, including VBR
- Support 9 sampling frequency: 8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 16-bit sigma-delta audio DAC
- Embedded headphone amplifier
- Support IR Remote control
- GPIO for various purposes
- Embedded LDO 3.3V->1.8V
- Pin to Pin compatible with AU6850[1]
- Embedded 32KB OTP memory for program code storage

Note 1: Contact with MVsilicon's FAE for detail.

1.2 Chip Architecture

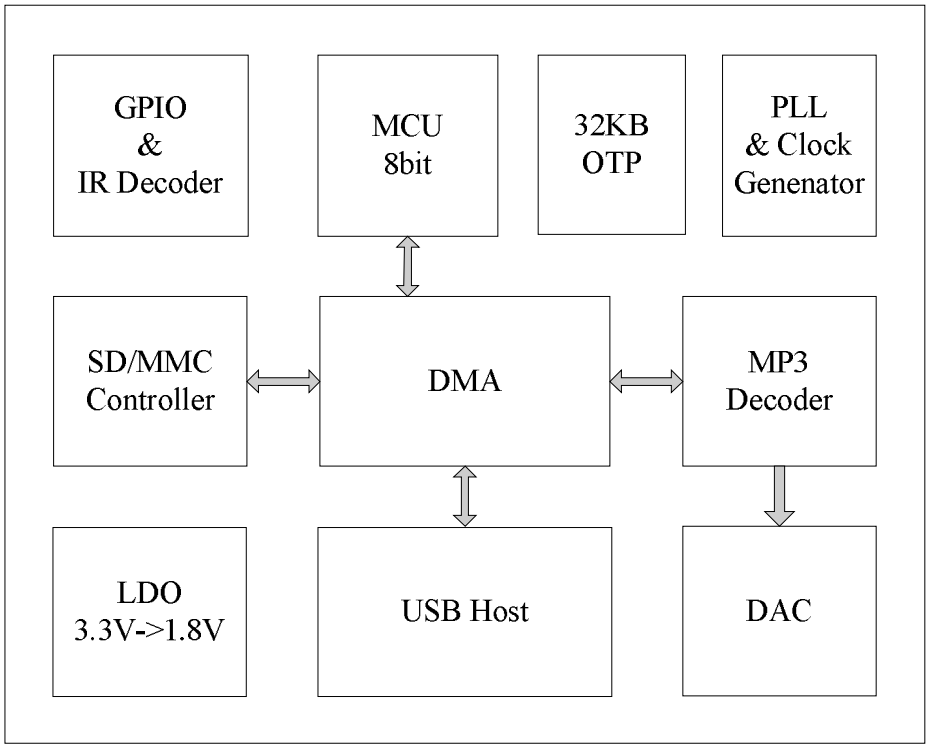

Figure 1 AU6850B Functional Block Diagram

2. System Application

- **MP3 mini audio system**

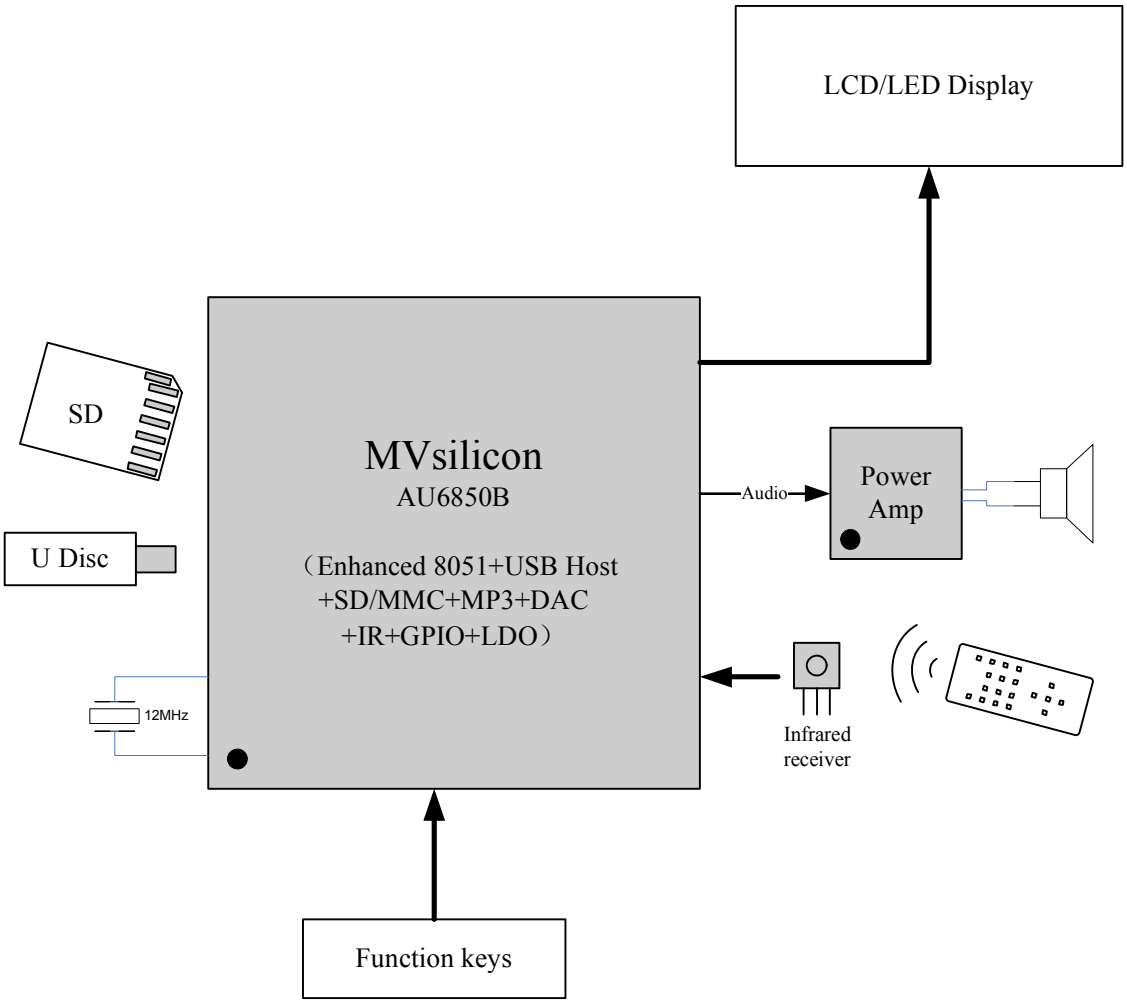

Figure 2 MP3 Audio System

3. Pin Description

AU6850B is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
AI	Analog Input
AO	Analog Output
PWR	Power
GND	Ground

3.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
			USB interface pins
USB_DP	31	I/O	USB Function D+ bus
USB_DM	30	I/O	USB Function D- bus
			CARD interface pins
SD_CLK	36	O	SD Card clock
SD_CMD	38	I/O	SD Card command line
SD_DAT0	39	I/O	SD Card data line
			DAC AUDIO interface pins
HPOUTR	1	AO	Head phone right channel output
HPOUTL	3	AO	Head phone left channel output
VREF	5	AI	Internal voltage reference
			GPIO/MCU IO pins
GPIO_A[1:0]	34:33	I/O	GPIO PORT, bank A
GPIO_A[4:2]	42:44	I/O	GPIO PORT, bank A
GPIO_A[6:5]	46:45	I/O	GPIO PORT, bank A
GPIO_A[7]	49	I/O	GPIO PORT, bank A
GPIO_B[3:0]	20:17	I/O	GPIO PORT, bank B
GPIO_B[7:4]	27:24	I/O	GPIO PORT, bank B
GPIO_C[2:0]	52:50	I/O	GPIO PORT, bank C
GPIO_C[7:3]	59:55	I/O	GPIO PORT, bank C
GPIO_D[0]	16	I/O	GPIO PORT, bank D
GPIO_D[2:1]	12:13	I/O	GPIO PORT, bank D
			CLK & Reset pins
XIN	9	I	12MHz Crystal oscillator input for PLL

XOUT	10	O	12MHz Crystal oscillator output for PLL
RESETN	15	I	System reset, active low
			mod pins
MOD0	14	I	Chip run mode configure pin
MOD1	41	I	Chip run mode configure pin
RUN	35	I	Chip run mode configure pin
			Power/Ground pins
AVDD33	4	PWR	Analog power(3.3V)
AVSS	2	GND	Analog ground
VPP	48	PWR	OTP program power
IO_VDD	23 32 47	PWR	Digital power for I/O(3.3V)
VSS	21 29 37	GND	Digital IO/core ground
VDD	8 22 40	PWR	Digital power for core(1.8V)
Reserved	7:6 11 28 54:53 64:60	NC	

4. Package

4.1 Package Diagram

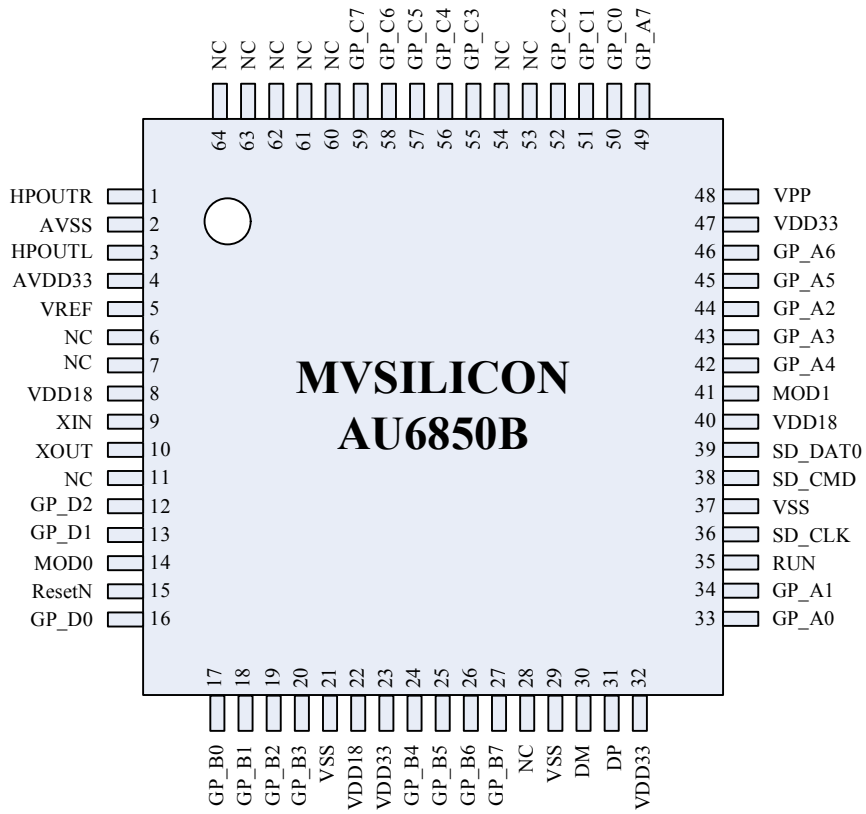

Figure 3 Package Diagram (LQFP64-10x10mm / TOP View)

4.2 Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00BSC	
θ	0	—	8°

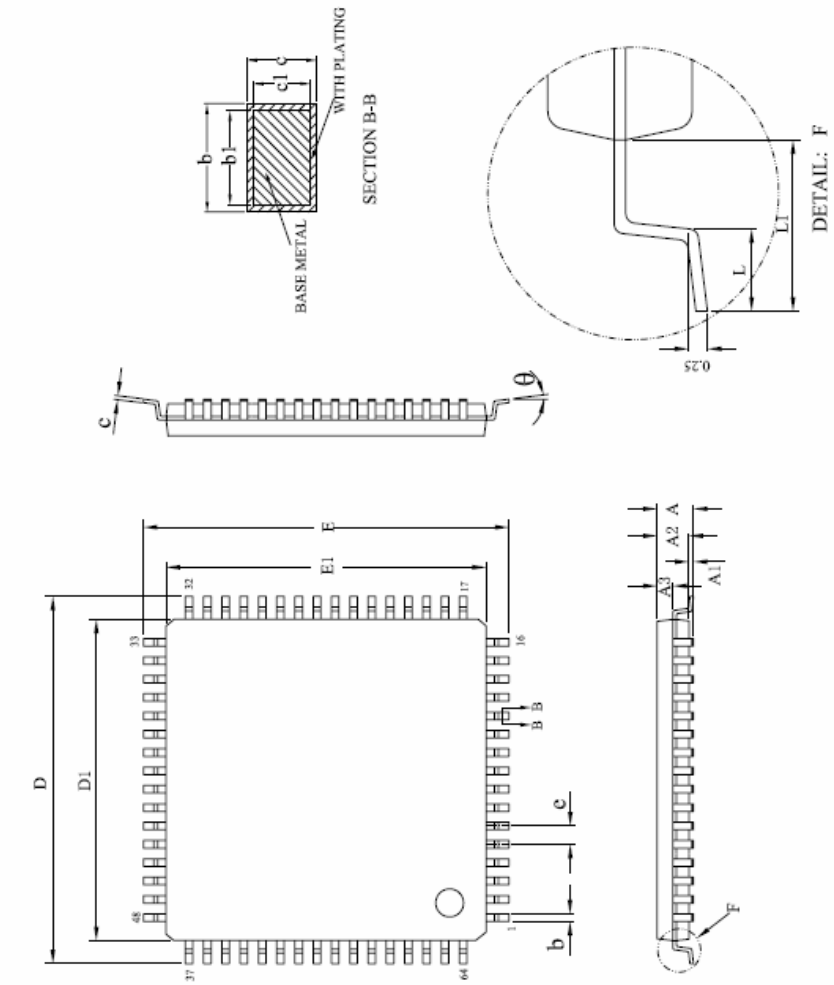

Figure 4 LQFP64-10x10mm Package Dimension Parameter

5. Electrical Specification

5.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCC_IO_AB	-0.5 to 4.6	V
Power Supply Voltage (Core)	VCC_CORE_AB	0 to 2	V
Power Supply Voltage (DAC)	VCC_DAC_AB	-0.3 to 3.6	V
Storage Temperature	TEMP_STG	-65 to 150	C

5.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (IO)	VCC_IO_OP	3	3.3	3.6	V
Power Supply Voltage (Core)	VCC_CORE_OP	1.62	1.8	1.98	V
Power Supply Voltage (DAC)	VCC_DAC_OP	3.0	3.3	3.6	V
Input Voltage (digital)	VIN	-0.3		5.5	V
Operating_Free Air Temperature	TEMP_OPR	-10		70	C

5.3 Electrical Characteristics

Table 4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		2.0		5.5	V
VIL	Input Low Voltage		-0.3		0.8	V
VOH	Output high voltage	@IOH=2mA	2.4			V
VOL	Output low voltage	@IOL=2mA			0.4	V
IL	Input leakage current		-10		10	uA
P_PLAY	Power consumption when playing	Playing mode		85		mW

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Contact Information

Shanghai Mountain View Silicon Technology Co Ltd

Shanghai Headquarter:
Suite 403, Jinying Tower A, 1518 Minsheng Road, Pudong New Area,
Shanghai, P.R. China
Zip code: 200135
Tel: 86-21-68549851
Fax: 86-21-68549859

Shenzhen Sales & Technical Support Office:
Suite 8C Olympic Plaza, Shangbao Road, Futian District,
Shenzhen, Guangdong, P.R. China
Zip code: 518034
Tel: 86-755-83522955
Fax: 86-755-83522957

Email: support@mvsilicon.com
Website: http://www.mvsilicon.com