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RTL8218B-CG

INTEGRATED 10/100/1000 OCTAL GIGABIT ETHERNET TRANSCEIVER

Brief

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8218B IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Author	Summary
Pre-0.1	2012/10/30	Davis	Preliminary Release.
Pre-0.2	2013/01/11	Davis	Add Order information
Pre-0.3	2013/01/18	Davis	Revised section 3.3, Table 1, Table 3, Table 5., Table 6., section10.2Mechanical Dimensions Notes
Pre-0.4	2013/05/07	Davis	1. Revised section 11 Order Information 2. Remove Package Identification in section 5 3. Revised section9, Table 28, Table 32, Table 33, Table 34, Table 35 4. Revised section 11
Pre-0.5	2013/05/15	Davis	1. Revised Table of Contents 2. section2
Pre-0.6	2013/06/27	Davis	1. Revised Table 1 Table 5. Table 6. Table 28

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1. General Description

The RTL8218B integrates octal independent Gigabit Ethernet transceivers into a single IC. The device performs all the physical layer (PHY) functions for 1000Base-T, 100Base-TX, and 10Base-T Ethernet on category 5 UTP cable except 1000Base-T half-duplex. 10Base-T functionality can also be achieved on standard category 3 or 4 cable.

This device includes PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. The device also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer modules.

Each of the four independent transceivers features an innovative RSGMII-plus/QSGMII for reduced PCB traces. All transceivers can communicate with the MAC simultaneously through the same RSGMII-plus/QSGMII.

2. Features

- Qctal-port integrated 10/100/1000Base-T Gigabit Ethernet transceiver
- Each port supports full duplex in 10/100/1000M mode (half duplex is only supported in 10/100M mode)
- Supports RSGMII-plus (5Gbps serial high speed interface) in 10/100/1000 mode
- Supports QSGMII (5Gbps serial high speed interface) in 10/100/1000 mode
- Supports IEEE 802.3az Energy Efficient Ethernet (EEE)
- Supports crossover detection and auto correction in 10Base-T/100Base-T
- Supports Sync Ethernet
- Supports IEEE 1588 v2
- Support Realtek EEEP
- Auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Supports Realtek’s Cable Test (RTCT)
- Supports Realtek’s Green Ethernet
  - Link-Up Power Saving
  - Link-Down Power Saving
- Low power consumption < 300mW per port
- Easy layout, good EMI, and good thermal performance
- 25MHz crystal or 3.3V OSC input
- 3.3V and 1.1V power supply
- RTL8218B: LQFP-128 E-PAD package

3. System Applications

3.1. 16-Port Gigabit Ethernet Switch

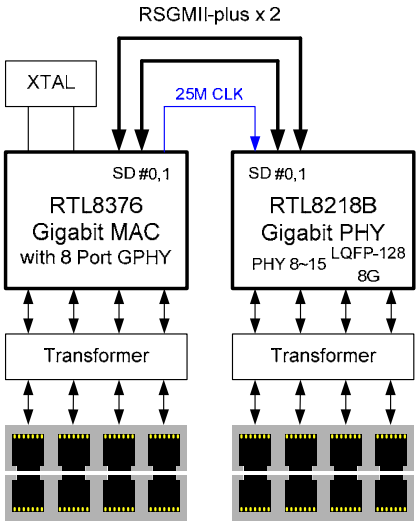


Figure 1. 16-Port Gigabit Ethernet Switch

3.2. 24-Port Gigabit Ethernet Switch

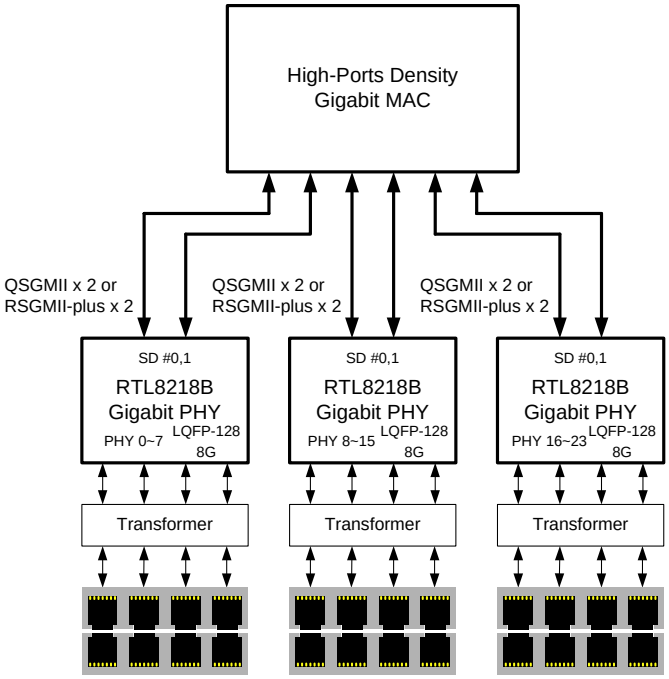


Figure 2. 24-Port Gigabit Ethernet Switch (QSGMII or RSGMII-plus Interface)

3.3. 24+4 Combo-Port Gigabit Ethernet Switch

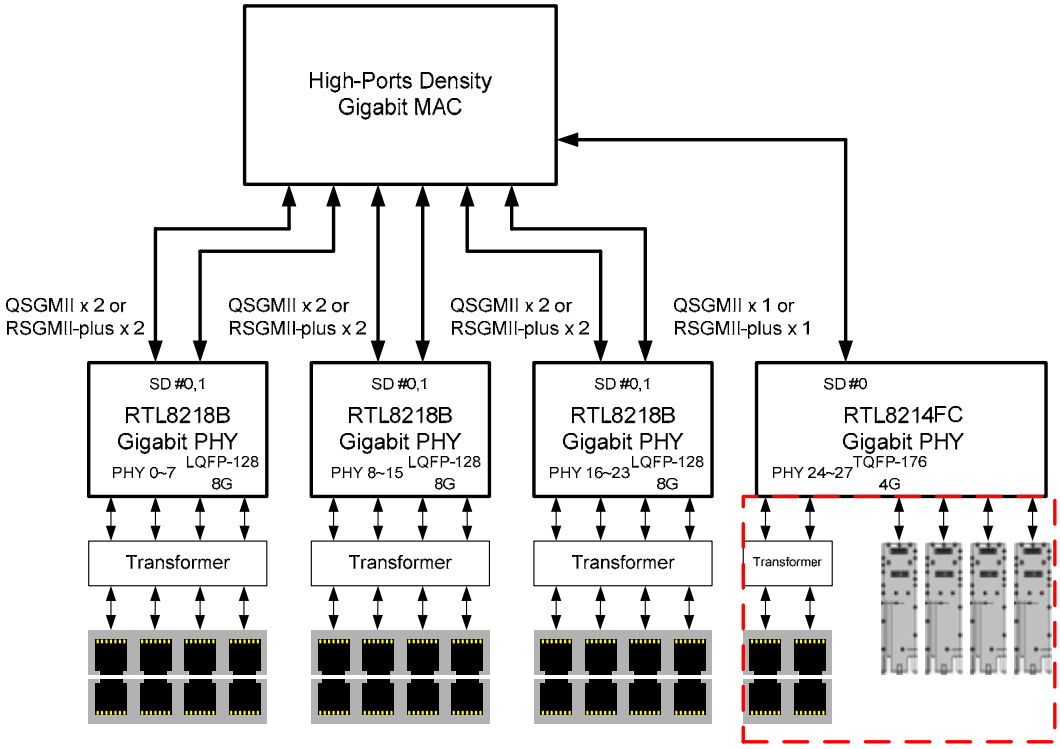


Figure 3. 28-Port Gigabit Ethernet Switch (QSGMII or RSGMII-plus Interface)

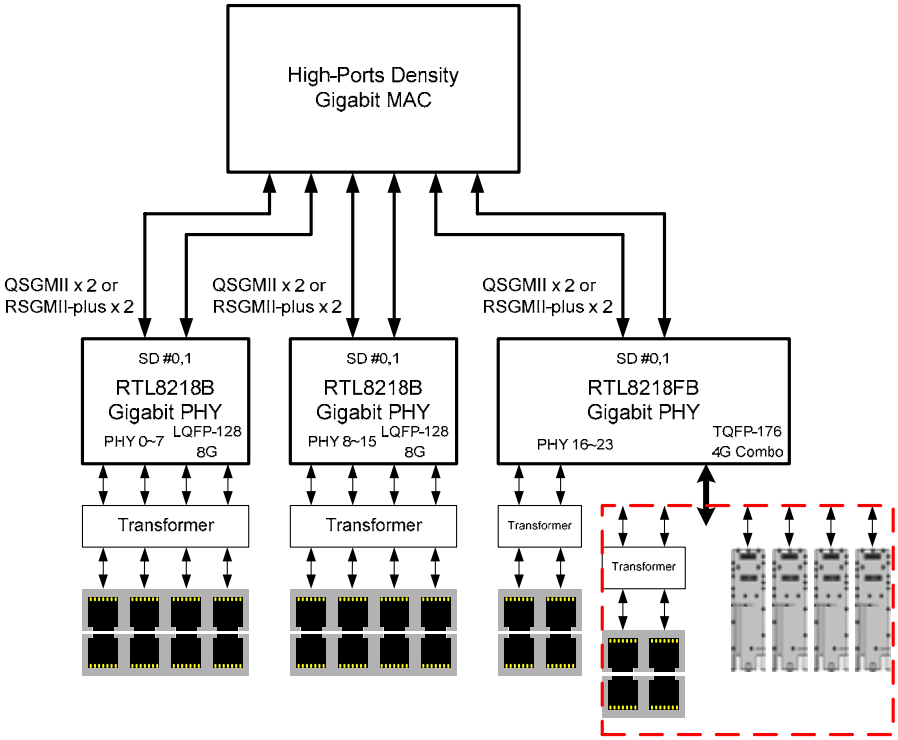


Figure 4. 20 + 4-Port Combo Gigabit Ethernet Switch (QSGMII or RSGMII-plus Interface)

4. Block Diagram

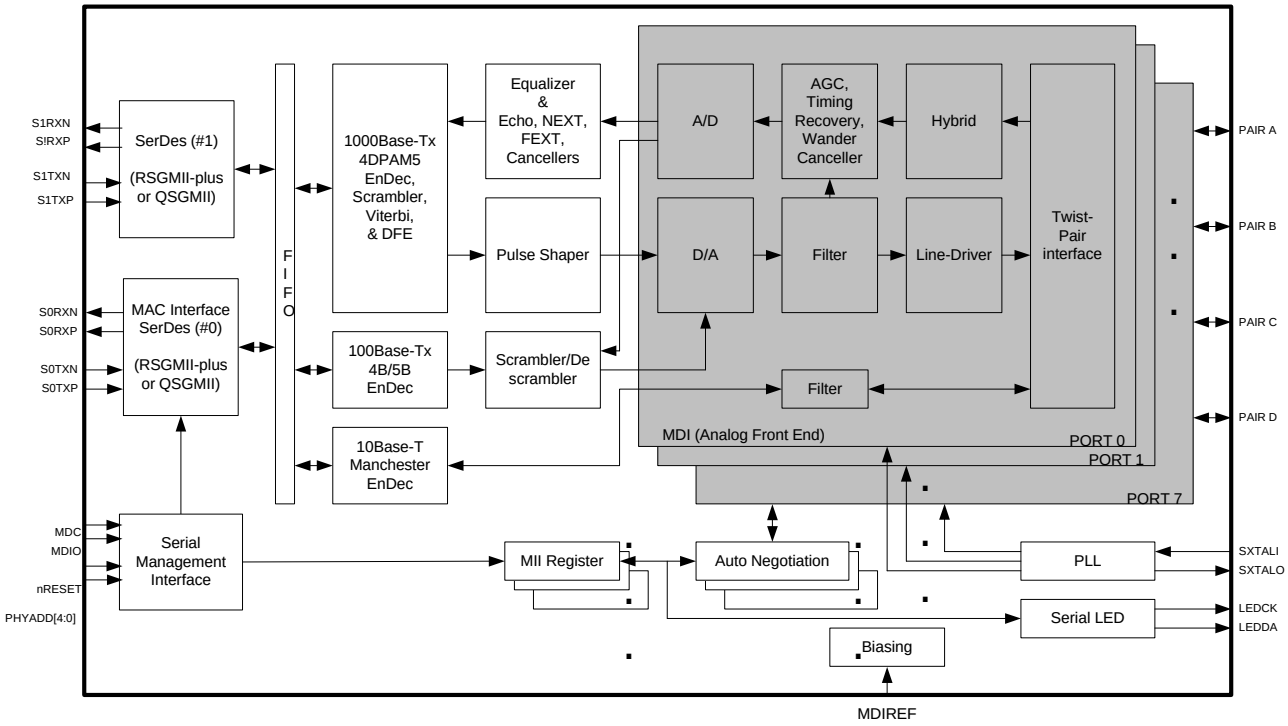


Figure 5. Block Diagram

5. Pin Assignments

5.1. RTL8218B Pin Assignments (LQFP-128)

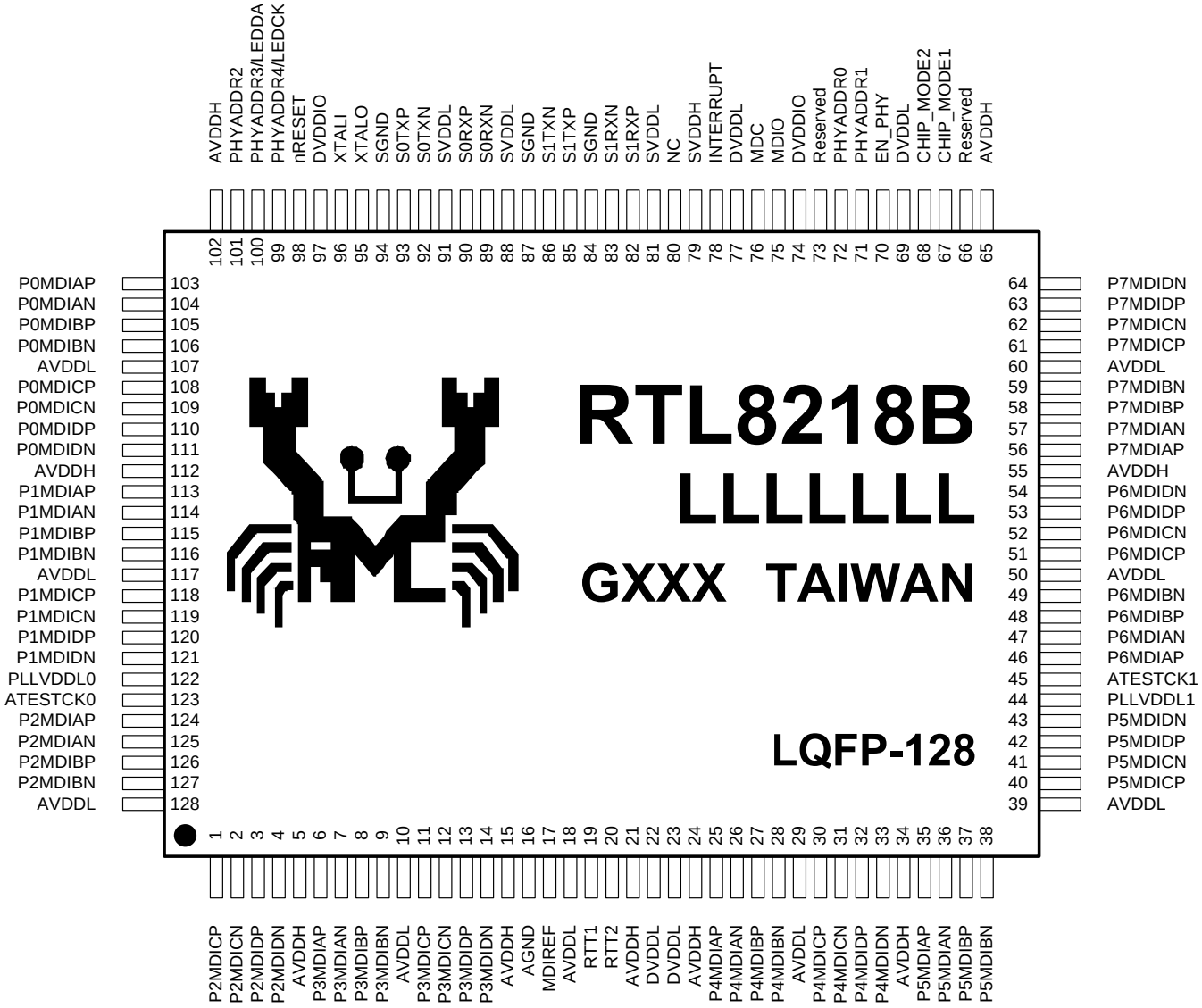


Figure 6. RTL8218B Pin Assignments (LQFP-128)

5.2. Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PD}: Input Pin With Pull-Down Resistor

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

SP SerDes Power Pin

I_S Schmitt Trigger Input Pin

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

A: Analog Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

SG SerDes Ground Pin

Table 1. RTL8218B Pin Assignment Table (LQFP-128)

Pin Name	Pin No.	Type
P2MDICP	1	AI/O
P2MDICN	2	AI/O
P2MDIDP	3	AI/O
P2MDIDN	4	AI/O
AVDDH	5	AP
P3MDIAP	6	AI/O
P3MDIAN	7	AI/O
P3MDIBP	8	AI/O
P3MDIBN	9	AI/O
AVDDL	10	AP
P3MDICP	11	AI/O
P3MDICN	12	AI/O
P3MDIDP	13	AI/O
P3MDIDN	14	AI/O
AVDDH	15	AP
AGND	16	AG
MDIREF	17	AO
AVDDL	18	AP

Pin Name	Pin No.	Type
RTT1	19	AO
RTT2	20	AO
AVDDH	21	AP
DVDDL	22	P
DVDDL	23	P
AVDDH	24	AP
P4MDIAP	25	AI/O
P4MDIAN	26	AI/O
P4MDIBP	27	AI/O
P4MDIBN	28	AI/O
AVDDL	29	AP
P4MDICP	30	AI/O
P4MDICN	31	AI/O
P4MDIDP	32	AI/O
P4MDIDN	33	AI/O
AVDDH	34	AP
P5MDIAP	35	AI/O
P5MDIAN	36	AI/O

Pin Name	Pin No.	Type
P5MDIBP	37	AI/O
P5MDIBN	38	AI/O
AVDDL	39	AP
P5MDICP	40	AI/O
P5MDICN	41	AI/O
P5MDIDP	42	AI/O
P5MDIDN	43	AI/O
PLLVDDL1	44	AP
ATESTCK1	45	AO
P6MDIAP	46	AI/O
P6MDIAN	47	AI/O
P6MDIBP	48	AI/O
P6MDIBN	49	AI/O
AVDDL	50	AP
P6MDICP	51	AI/O
P6MDICN	52	AI/O
P6MDIDP	53	AI/O
P6MDIDN	54	AI/O
AVDDH	55	AP
P7MDIAP	56	AI/O
P7MDIAN	57	AI/O
P7MDIBP	58	AI/O
P7MDIBN	59	AI/O
AVDDL	60	AP
P7MDICP	61	AI/O
P7MDICN	62	AI/O
P7MDIDP	63	AI/O
P7MDIDN	64	AI/O
AVDDH	65	AP
Reserved	66	I/O_{PU}
CHIP_MODE1	67	I_{PU}
CHIP_MODE2	68	I_{PU}
DVDDL	69	P
EN_PHY	70	I/O_{PU}
PHYADDR1	71	I/O_{PD}
PHYADDR0	72	I/O_{PD}
Reserved	73	I/O_{PU}
DVDDIO	74	P
MDIO	75	I/O_{PU}
MDC	76	I
DVDDL	77	P
INTERRUPT	78	I/O_{PU}
SVDDH	79	SP
NC	80	-

Pin Name	Pin No.	Type
SVDDL	81	SP
S1RXP	82	AO
S1RXN	83	AO
SGND	84	SG
S1TXP	85	AI
S1TXN	86	AI
SGND	87	SG
SVDDL	88	SP
S0RXN	89	AO
S0RXP	90	AO
SVDDL	91	SP
S0TXN	92	AI
S0TXP	93	AI
SGND	94	SG
XTALO	95	AO
XTALI	96	AI
DVDDIO	97	P
nRESET	98	I
PHYADDR4/LEDCK	99	I/O_{PD}
PHYADDR3/LEDDA	100	I/O_{PD}
PHYADDR2	101	I_{PD}
AVDDH	102	AP
P0MDIAP	103	AI/O
P0MDIAN	104	AI/O
P0MDIBP	105	AI/O
P0MDIBN	106	AI/O
AVDDL	107	AP
P0MDICP	108	AI/O
P0MDICN	109	AI/O
P0MDIDP	110	AI/O
P0MDIDN	111	AI/O
AVDDH	112	AP
P1MDIAP	113	AI/O
P1MDIAN	114	AI/O
P1MDIBP	115	AI/O
P1MDIBN	116	AI/O
AVDDL	117	AP
P1MDICP	118	AI/O
P1MDICN	119	AI/O
P1MDIDP	120	AI/O
P1MDIDN	121	AI/O
PLLVDDL0	122	AP
ATESTCK0	123	AO
P2MDIAP	124	AI/O

Pin Name	Pin No.	Type
P2MDIAN	125	AI/O
P2MDIBP	126	AI/O

Pin Name	Pin No.	Type
P2MDIBN	127	AI/O
AVDDL	128	AP

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	RTL8218B Pin No.	Type	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	103, 104 105, 106 108, 109 110, 111	AI/O	Port 0 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	113, 114 115, 116 118, 119 120, 121	AI/O	Port 1 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	124, 125 126, 127 1, 2 3, 4	AI/O	Port 2 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	6, 7 8, 9 11, 12 13, 14	AI/O	Port 3 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	25, 26 27, 28 30, 31 32, 33	AI/O	Port 4 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.

Pin Name	RTL8218B Pin No.	Type	Description
P5MDIAP/N P5MDIBP/N P5MDICP/N P5MDIDP/N	35, 36 37, 38 40, 41 42, 43	AI/O	Port 5 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P6MDIAP/N P6MDIBP/N P6MDICP/N P6MDIDP/N	46, 47 48, 49 51, 52 53, 54	AI/O	Port 6 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P7MDIAP/N P7MDIBP/N P7MDICP/N P7MDIDP/N	56, 57 58, 59 61, 62 63, 64	AI/O	Port 7 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.

6.2. RSGMII-Plus / QSGMII Interface Pins

Table 3. RSGMII Pins

Pin Name	RTL8218B Pin No.	Type	Description
S0RXP/N S1RXP/N	90, 89 82, 83	AO	RSGMII-Plus / QSGMII Differential Output. 5GHz serial interfaces to receive data from an External device that supports the RSGMII-Plus interface. (Ref. ChipMode configuration for RSGMII-Plus and QSGMII)
S0TXP/N S1TXP/N	93, 92 85, 86	AI	RSGMII-Plus Differential Input. 5GHz serial interfaces to transfer data from the RTL8218B to an External device that supports the RSGMII-Plus interface. (Ref. ChipMode configuration for RSGMII-Plus and QSGMII)

6.3. Configuration Strapping Pins

Table 4. Configuration Strapping Pins

Pin Name	RTL8218B Pin No.	Type	Description
CHIP_MODE2	68	I_{PU}	MAC Interface Configuration: CHIP_MODE[2:1] = 11: RSGMII-Plus 10: QSGMII
CHIP_MODE1	67	I_{PU}	Reference CHIP_MODE2

Pin Name	RTL8218B Pin No.	Type	Description
EN_PHY	70	I_{PU}	Upon Reset, EN_PHY 1: Power up all ports 0: Power down all ports and set the MII register 0.11 power down as 1.
PHYADDR[4:0]	99,100,101, 71, 72	I/O_{PD}	Upon Reset PHYADDR [4:0] PHY Address Bits 4:0.

6.4. Power and GND Pins

Table 5. Power and GND Pins

Pin Name	RTL8218B Pin No.	Type	Description
DVDDIO	74, 97	P	Digital I/O High Voltage Power for MDC,MDIO, LED, nRESET
DVDDL	22, 23, 69, 77	P	Digital Low Voltage Power
SVDDH	79	SP	RSGMII-Plus / QSGMII High Voltage Power
SVDDL	81, 88, 91	SP	RSGMII-Plus / QSGMII Low Voltage Power
AVDDH	5, 15, 21, 24, 34, 55, 65, 102, 112	AP	Analog High Voltage Power
AVDDL	10, 18, 29, 39, 50, 60, 107, 117, 128	AP	Analog Low Voltage Power
PLLVDDL0 PLLVDDL1	122 44	AP	PLL Low Voltage Power
AGND	16	AG	Analog GND
SGND	84, 87, 94	SG	RSGMII-Plus / QSGMII GND
GND	EPAD	G	Digital/Analog GND

6.5. Miscellaneous Pins

Table 6. Miscellaneous Pins

Pin Name	RTL8218B Pin No.	Type	Description
MDIREF	17	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
MDIO	75	I/O_{PU}	MII Management Interface Data Pin.
MDC	76	I	MII Management Interface Clock Pin.
INTERRUPT	78	I/O_{PU}	Interrupt will active high if INTERRUPT pin be tied to GND via 1K resister at power on, Interrupt will active low if INTERRUPT pin be tied to DVDDIO via 4.7K resister at power on

Pin Name	RTL8218B Pin No.	Type	Description
nRESET	98	I	System Pin Reset Input. When low active will reset the RTL8218B.
LEDCK	99	I/O_{PD}	Serial LED Clock Output
LEDDA	100	I/O_{PD}	Serial LED Data Output.
ATESTCK0	123	AO	Reserved for Internal Use. Must be left floating.
ATESTCK1	45	AO	Reserved for Internal Use. Must be left floating.
RTT1	19	AO	Reserved for Internal Use. Must be left floating or pull-up to DVDDIO via 4.7K resister.
RTT2	20	AO	Reserved for Internal Use. Must be left floating or pull-up to DVDDIO via 4.7K resister.
Reserved	66	I/O_{PU}	Reserved for Internal Use, Must be left floating or pull-up to DVDDIO via 4.7K resister.
Reserved	73	I/O_{PU}	Reserved. Must be tied to GND via 1K resister for normal operation
NC	80		No Connection

7. Function Description

7.1. MDI Interface

The RTL8218B embeds Octal Gigabit Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-Tx, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

The RTL8218B also support Giga-Lite (500Mbps) function, only pairs A and B are used when links and during auto-negotiation at Giga-Lite.

7.2. 1000Base-T Transmit Function

The 1000Base-T transmit function performs 8B/10B coding, scrambling, 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

7.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.8. Auto-Negotiation for UTP

The RTL8218B obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8218B advertises full capabilities (1000full, 100full, 100half, 10full, 10half) together with flow control ability.

7.9. Crossover Detection and Auto Correction

The RTL8218B automatically determines whether or not it needs to crossover between pairs, so that an external crossover cable is not required. When connecting to a device that does not perform MDI crossover, the RTL8218B automatically switches its pin pairs to communicate with the remote device. When connecting to a device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The RTL8218B is set to MDI Crossover by default. The pin mapping in MDI and MDI Crossover mode is given below.

Table 7. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

7.10. Polarity Correction

The RTL8218B automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-Tx mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when 10Base-T links up. The polarity becomes unlocked when the link is down.

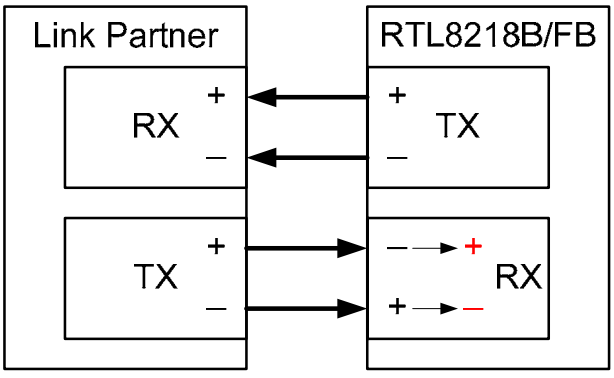


Figure 7. Conceptual Example of Polarity Correction

7.11. MDC/MDIO Interface

The RTL8218B supports the IEEE compliant Management Data Input/Output (MDIO) Interface. This is the only method for the MAC to acquire the status of the PHY. The MII management interface (MIIM) registers are written and read serially, using the MDC/MDIO pins. Data transferred to and from the MDIO pins is synchronized with the MDC clock. All transfers are initiated by the MAC. A clock of up to 12.5MHz must drive the MDC pin of the RTL8218B.

The MII register is a block of 32 registers, each 16 bits wide. Certain registers are defined by the IEEE 802.3 and are required for compliance (0-10, 15).

The MDIO frame structure starts with a 32-bit preamble, which is required by the RTL8218B. The following data includes a start-of-frame marker, an op-code, a 10-bit address field, and a 16-bit data field. The address field is divided into two 5-bit segments. The first segment identifies the PHY address and the second identifies the register being accessed.

The four uppermost bits of the 5-bit PHY address are determined by the hardware strapping values during power up. The LSB of the PHY address is '0' for Port0 and '1' for Port1. The MDIO protocol provides both read and write operations. During a write operation, the MAC drives the MDIO line for the entire frame. For a read operation, a turn-around time is inserted in the frame to allow the PHY to drive back to the MAC. The MDIO pin of the MAC must be put in high-impedance during these bit times. Figure 8 and Figure 9 depict the MDIO read and write frame format respectively.

The RTL8218B is permanently programmed for preamble suppression. A preamble of 32 1 bits is required only for the first read or write. The management preamble may be as short as 1 bit.

RTL8218B MDC support clock frequency up to 12.5MHz.

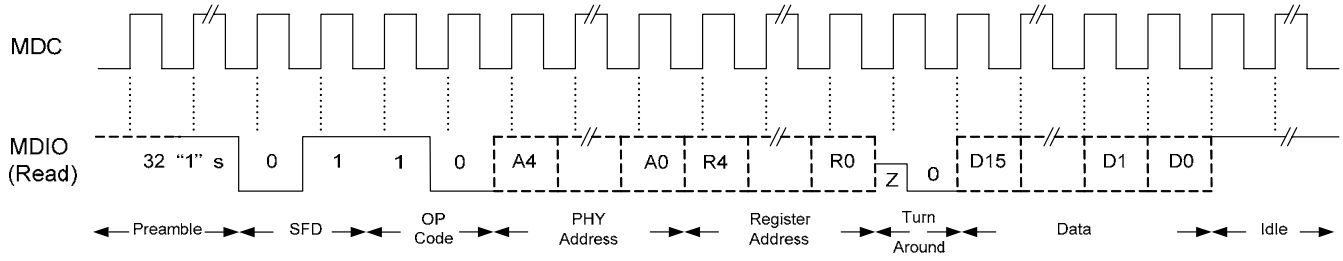


Figure 8. MDIO Read Frame Format

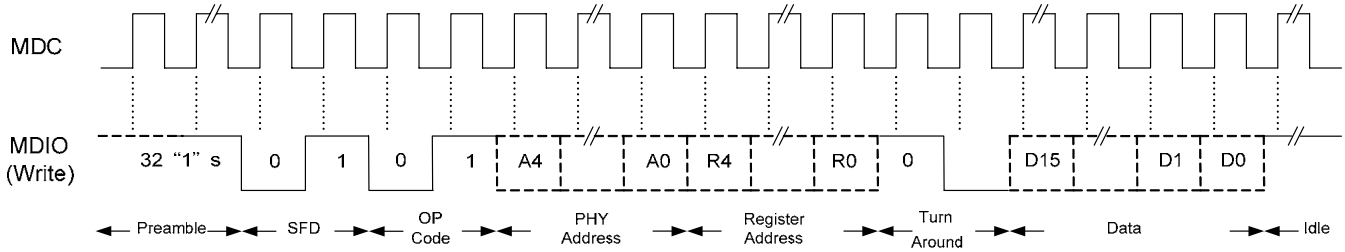


Figure 9. MDIO Write Frame Format

7.12. Reduced Serial Gigabit Media Independent Interface Plus (RSGMII-plus)

RSGMII-plus (Reduced Serial Gigabit Media Independent Interface plus) reduces PCB complexity and IC pin count. This innovative 5Gbps serial interface provides an up to 10 inch MAC to PHY communication path. RSGMII-plus can carry the full duplex gigabit Ethernet data streams of four ports simultaneously, using only 4 pins.

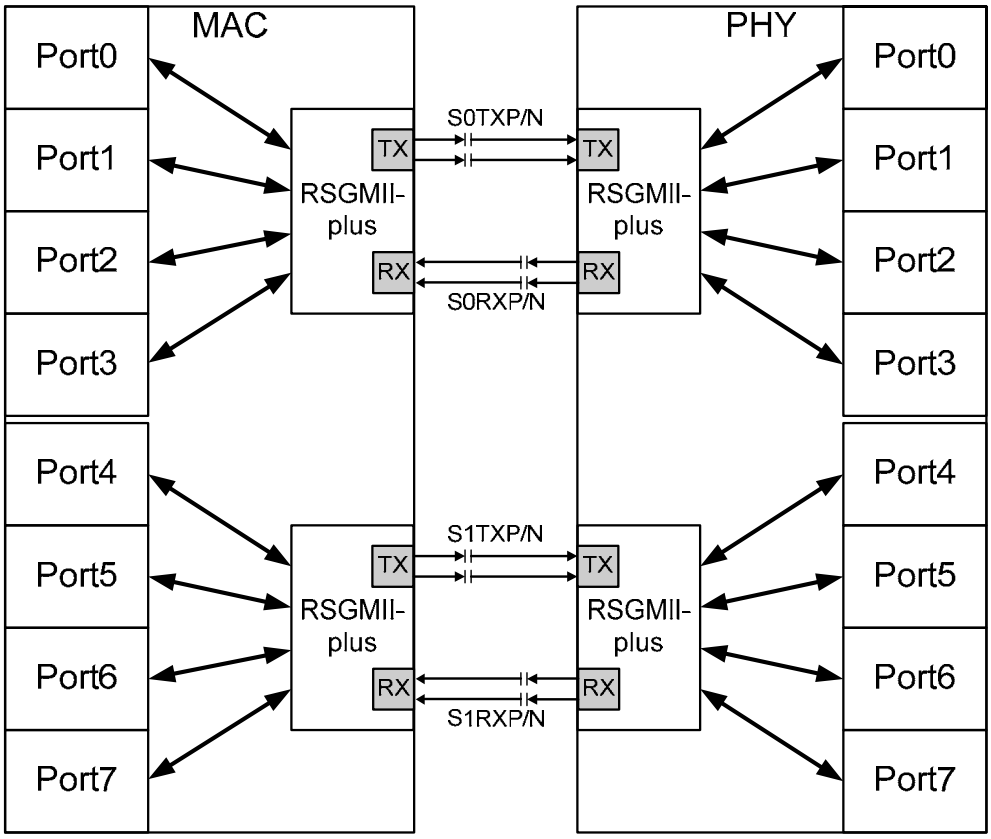


Figure 10. RSGMII-plus Interconnection Diagram

7.13. Quad Serial Gigabit Media Independent Interface (QSGMII)

QSGMII (Quad Serial Gigabit Media Independent Interface) reduces PCB complexity and IC pin count. This innovative 5Gbps serial interface provides an up to 10 inch MAC to PHY communication path. QSGMII can carry the full duplex gigabit Ethernet data streams of four ports simultaneously, using only 4 pins.

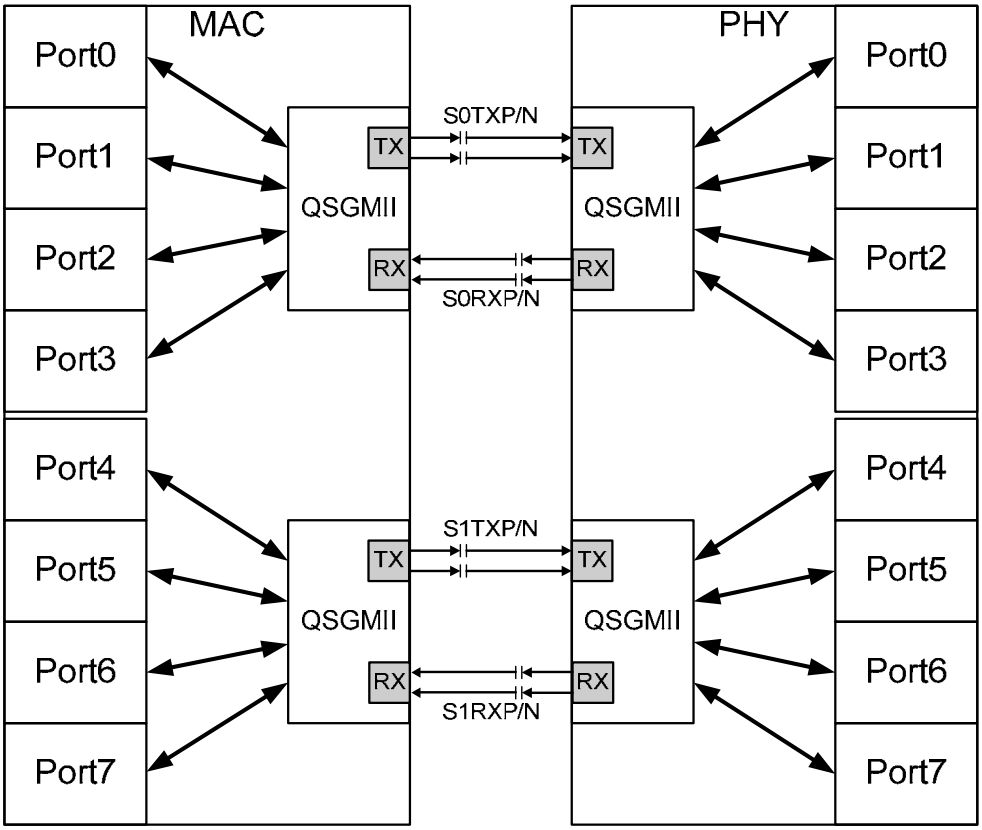
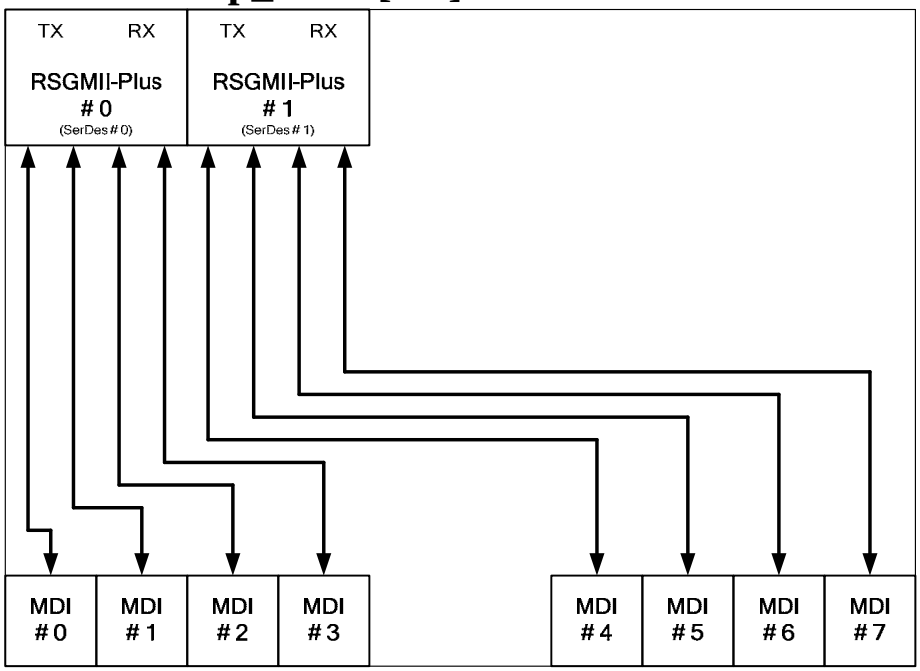


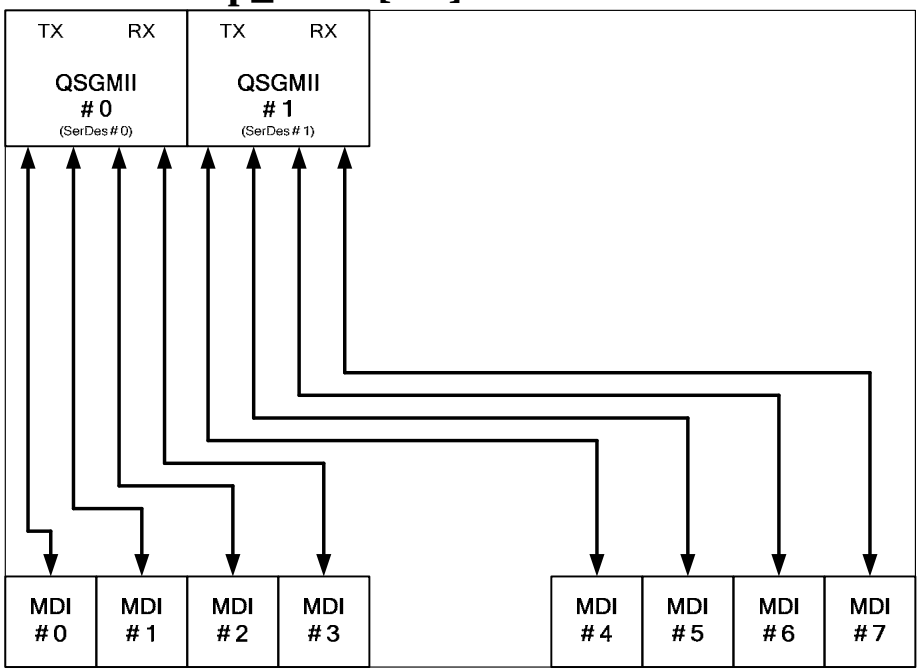
Figure 11. QSGMII Interconnection Diagram

7.14. RTL8218B Chip Mode Definition

7.14.1. Chip_Mode[2:1] = 2b11



7.14.2. Chip_Mode[2:1] = 2b10



7.15. Serial LED

7.15.1. Port Status Indicator

The RTL8218B supports serial LED mode. In the serial LED mode, the data is clocked through a shift register and the shifted symbols are output to the 36 LED pins. Each MDI port has three indicator symbols. Each symbol may have different indicator information as below.

7.16. Serial LED

7.16.1. Port Status Indicator

The RTL8218B supports serial LED mode. In the serial LED mode, the data is clocked through a shift register and the shifted symbols are output to the 36 LED pins. Each MDI port has three indicator symbols and each fiber port has three indicator symbols. Each symbol may have different indicator information as below.

7.16.2. LED configuration

Table 8. Serial LED Per-LED Control

PHY0 , Reg.29 = 8, Reg.=31=0x281				
Reg.bit	**Name**	**Mode**	**Description**	**Default**
18.[15:12]	LED_00_Mode	RW	Assign LEDn to Port. 0000: MDI0 0001: MDI1 0010: MDI2 0011: MDI3 0100: MDI4 0101: MDI5 0110: MDI6 0111: MDI7 1000~1110: Reserved 1111: Disable	0x0
18.11		RW	1000M Speed Indicator.	0x0
18.10		RW	100M Speed Indicator.	0x0
18.9		RW	10M Speed Indicator.	0x0
18.8		RW	Reserved	0x0
18.7		RW	1000M Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.	0x0
18.6		RW	100M Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.	0x0
18.5		RW	10M Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.	0x0
18.4		RW	Reserved	0x0
18.3		RW	Duplex Indicator.	0x0
18.2		RW	Collision Indicator. Blinking when the collision is occurs.	0x0
18.1		RW	Tx Activity Indicator. Act blinking when the corresponding port is transmitting.	0x0
18.0		RW	Rx Activity Indicator. Act blinking when the corresponding port is receiving.	0x0
19[15:0]	LED_01_Mode	RW	Same as LED_00_Mode	
20[15:0]	LED_02_Mode	RW	Same as LED_00_Mode	
21[15:0]	LED_03_Mode	RW	Same as LED_00_Mode	
22[15:0]	LED_04_Mode	RW	Same as LED_00_Mode	
23[15:0]	LED_05_Mode	RW	Same as LED_00_Mode	
PHY0 , Reg.29 = 8, Reg.=31=0x282				

Reg.bit	Name	Mode	Description	Default
16[15:0]	LED_06_Mode	RW	Same as LED_00_Mode	
17[15:0]	LED_07_Mode	RW	Same as LED_00_Mode	
18[15:0]	LED_08_Mode	RW	Same as LED_00_Mode	
19[15:0]	LED_09_Mode	RW	Same as LED_00_Mode	
20[15:0]	LED_10_Mode	RW	Same as LED_00_Mode	
21[15:0]	LED_11_Mode	RW	Same as LED_00_Mode	
22[15:0]	LED_12_Mode	RW	Same as LED_00_Mode	
23[15:0]	LED_13_Mode	RW	Same as LED_00_Mode	
PHY0 , Reg.29 = 8, Reg.=31=0x283				
Reg.bit	**Name**	**Mode**	**Description**	**Default**
16[15:0]	LED_14_Mode	RW	Same as LED_00_Mode	
17[15:0]	LED_15_Mode	RW	Same as LED_00_Mode	
18[15:0]	LED_16_Mode	RW	Same as LED_00_Mode	
19[15:0]	LED_17_Mode	RW	Same as LED_00_Mode	
20[15:0]	LED_18_Mode	RW	Same as LED_00_Mode	
21[15:0]	LED_19_Mode	RW	Same as LED_00_Mode	
22[15:0]	LED_20_Mode	RW	Same as LED_00_Mode	
23[15:0]	LED_21_Mode	RW	Same as LED_00_Mode	
PHY0 , Reg.29 = 8, Reg.=31=0x284				
Reg.bit	**Name**	**Mode**	**Description**	**Default**
16[15:0]	LED_22_Mode	RW	Same as LED_00_Mode	
17[15:0]	LED_23_Mode	RW	Same as LED_00_Mode	
18[15:0]	LED_24_Mode	RW	Same as LED_00_Mode	
19[15:0]	LED_25_Mode	RW	Same as LED_00_Mode	
20[15:0]	LED_26_Mode	RW	Same as LED_00_Mode	
21[15:0]	LED_27_Mode	RW	Same as LED_00_Mode	
22[15:0]	LED_28_Mode	RW	Same as LED_00_Mode	
23[15:0]	LED_29_Mode	RW	Same as LED_00_Mode	
PHY0 , Reg.29 = 8, Reg.=31=0x285				
Reg.bit	**Name**	**Mode**	**Description**	**Default**
16[15:0]	LED_30_Mode	RW	Same as LED_00_Mode	
17[15:0]	LED_31_Mode	RW	Same as LED_00_Mode	
18[15:0]	LED_32_Mode	RW	Same as LED_00_Mode	
19[15:0]	LED_33_Mode	RW	Same as LED_00_Mode	
20[15:0]	LED_34_Mode	RW	Same as LED_00_Mode	
21[15:0]	LED_35_Mode	RW	Same as LED_00_Mode	

Table 9. Serial LED Mode Configuration (Per-Port 3 LEDs)

of Per-LED Register	LED_MODE [1:0]=11	LED_MODE [1:0]=10	LED_MODE [1:0]=01	LED_MODE [1:0]=00
LED35	0x0FF0	0x0880	0x0880	0x0FF0
LED34	0x1FF0	0x1880	0x1880	0x1FF0
LED33	0x2FF0	0x2880	0x2880	0x2FF0
LED32	0x3FF0	0x3880	0x3880	0x3FF0
LED31	0x4FF0	0x4880	0x4880	0x4FF0
LED30	0x5FF0	0x5880	0x5880	0x5FF0
LED29	0x6FF0	0x6880	0x6880	0x6FF0
LED28	0x7FF0	0x7880	0x7880	0x7FF0
LED27	0x0800	0x0440	0x0660	0x8CC0
LED26	0x1800	0x1440	0x1660	0x9CC0
LED25	0x2800	0x2440	0x2660	0xACC0
LED24	0x3800	0x3440	0x3660	0xBCC0
LED23	0x4800	0x4440	0x4660	0xF000
LED22	0x5800	0x5440	0x5660	0xF000
LED21	0x6800	0x6440	0x6660	0xF000
LED20	0x7800	0x7440	0x7660	0xF000
LED19	0x0400	0x0220	0x8880	0xF000
LED18	0x1400	0x1220	0x9880	0xF000
LED17	0x2400	0x2220	0xA880	0xF000
LED16	0x3400	0x3220	0xB880	0xF000
LED15	0x4400	0x4220	0x8440	0xF000
LED14	0x5400	0x5220	0x9440	0xF000
LED13	0x6400	0x6220	0xA440	0xF000
LED12	0x7400	0x7220	0xB440	0xF000
LED11	0x8CC0	0x8880	0xF000	0xF000
LED10	0x9CC0	0x9880	0xF000	0xF000
LED09	0xACC0	0xA880	0xF000	0xF000
LED08	0xBCC0	0xB880	0xF000	0xF000
LED07	0x8800	0x8440	0xF000	0xF000
LED06	0x9800	0x9440	0xF000	0xF000
LED05	0xA800	0xA440	0xF000	0xF000
LED04	0xB800	0xB440	0xF000	0xF000
LED03	0x8400	0xF000	0xF000	0xF000
LED02	0x9400	0xF000	0xF000	0xF000
LED01	0xA400	0xF000	0xF000	0xF000
LED00	0xB400	0xF000	0xF000	0xF000

of Per-LED Register	LED_MODE [1:0]=11	LED_MODE [1:0]=10	LED_MODE [1:0]=01	LED_MODE [1:0]=00
Note	LED_MODE [1:0]=11 MDI: [Link/Act] [SPD1000] [SPD100] FX: [Link/Act] [SPD1000] [SPD100] LED_MODE [1:0]=10 MDI: [SPD1000/Act] [SPD100/Act] [SPD10/Act] FX: [SPD1000/Act] [SPD100/Act] [Disable] LED_MODE [1:0]=01 MDI: [SPD1000/Act] [SPD100(10)/Act] FX: [SPD1000/Act] [SPD100/Act] LED_MODE [1:0]=00 MDI: [Link/Act] FX: [Link/Act]			

7.16.3. Serial LED configuration Register

Table 10. Serial LED Per-LED Control

Reg.bit	Name	Mode	Description	Default
16[15:14]	Reserved	RW	Reserved	00
16[13:12]	cfg_led_mode	RW	00: LED_Mode0. Per-Port 2 LEDs 01: LED_Mode1. Per-Port 2 LEDs 10: LED_Mode2. Per-Port 3 LEDs 11: LED_Mode3. Per-Port 3 LEDs default values should refer to chip_mode	11
16[11]	Reserved	RW	Reserved	0
16[10:8]	Serial Blink Rate	RW	LED Blink Rate Configuration. 000: 32ms 001: 64ms 010: 128ms 011: 256ms 100: 512ms 101: 1024ms 110: 48ms 111: 96ms	000
16[7:6]	serial led burst cycle	RW	2'b00:8 (ms) 2'b01:16 2'b10:32 2'b11:64	10
16[5:4]	serial led clock cycle	RW	2'b00:32 (ns) 2'b01:64 2'b10:96 2'b11:192	11

16[3]	**led_seri_active_low**	**RW**	**Serial LED active LOW** **0: LED status active high** **1: LED status active low**	**1**
16[2]	**led_seri_disable**	**RW**	**Disable Serial LED.** **1: Disable** **0: Enable**	
16[1]	**led_data_e_b**	**RW**	**Serial LED DATA_EN**	
16[0]	**led_clk_e_b**	**RW**	**Serial LED CLK_EN**	

Upon reset, the RTL8218B supports LED functions by blinking all LEDs once

7.17. Realtek Cable Test (RTCT)

The RTL8218B physical layer transceivers use DSP technology to implement the Realtek Cable Tester (RTCT) feature. The RTCT function could be used to detect short, open or impedance mismatch in each differential pair.

7.18. Green Ethernet

7.18.1. Link-Up and Cable Length Power Saving

The RTL8218B provides link-up and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

7.18.2. Link-Down Power Saving

The RTL8218B implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

7.19. IEEE 802.3az Energy Efficient Ethernet (EEE)

The RTL8218B supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T and 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

8. Register Descriptions

The registers 0~15 of the MII are defined by the MII specification. Other registers are defined by Realtek Semiconductor Corp. for internal use and are reserved for specific uses.

The following abbreviations are used:

RW: Read/Write RO: Read Only SC: Self Clearing

LL: Latch Low until clear LH: Latch High until clear

Table 11. Register Descriptions

Page	Register	Description	Default
0x0A42	0	Control	0x1140
	1	Status	0x7949
	2	PHY Identifier 1	0x001C
	3	PHY Identifier 2	0xC981
	4	Auto-Negotiation Advertisement	0x05E1
	5	Auto-Negotiation Link Partner Ability	0x0000
	6	Auto-Negotiation Expansion	0x0064
	7	Auto-Negotiation Next Page Transmit	0x2801
	8	Auto-Negotiation Link Partner Next Page Ability	0x0000
	9	1000Base-T Control	0x0E00
	10	1000Base-T Status	0x0000
	11 ~ 14	Reserved	0x0000
	15	Extended Status	0x2000

8.1. Register 0: Control

Table 12. Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset 0: Normal operation This bit is self-clearing	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex, 100Base-TX full duplex, or 1000Base-T full duplex.	0
0.13	Speed Selection[0]	RW	[0.6,0.13] Speed Selection[1:0] 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps This bit can be set through SMI (Read/Write)	0
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write)	1
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from RSGMII or QSGMII. PHY is still able to respond to MDC/MDIO 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation This bit can be set through SMI (Read/Write)	1
0.7	Collision Test	RO	1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN	0
0.6	Speed Selection[1]	RW	See Bit 13	1
0.5	Reserved	RW	Reserved	
0.[4:0]	Reserved	RO	Reserved	000000

8.2. Register 1: Status

Table 13. Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base-T4	RO	0: No 100Base-T4 capability The RTL8218B does not support 100Base-T4 mode, and this bit should always be 0	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-TX half duplex capable	1
1.10	100Base-T2-FD	RO	0: No 100Base-T2 full duplex capability The RTL8218B does not support 100Base-T2 mode, and this bit should always be 0	0
1.9	100Base-T2-HD	RO	0: No 100Base-T2 half duplex capability The RTL8218B does not support 100Base-T2 mode, and this bit should always be 0	0
1.8	Extended Status	RO	1: Extended status information in Register 15 The RTL8218B always supports Extended Status Register	1
1.7	Unidirectional ability	RO	1: PHY able to transmit regardless PHY has determined that a valid link has been established. 0: PHY able to transmit only when link has been established	0
1.6	MF Preamble Suppression	RO	The RTL8218B will accept management frames with preamble suppressed	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1: Remote fault indication from link partner has been detected 0: No remote fault indication detected This bit will remain set until it is cleared by reading register 1 via the management interface	0
1.3	Auto-Negotiation Ability	RO	1: Auto-negotiation capable (permanently =1) 0: Without Auto-negotiation capability	1
1.2	Link Status	RO/LL	1: Link has not failed since previous read 0: Link has failed since previous read If the link fails, this bit will be set to 0 until this bit is read	0
1.1	Jabber Detect	RO/LH	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode	0
1.0	Extended Capability	RO	1: Extended register capable (permanently =1) 0: Not extended register capable	1

8.3. Register 2: PHY Identifier 1

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY part of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number, and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 14. Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th Bits of the Organizationally Unique Identifier (OUI), Respectively	0x001C

8.4. Register 3: PHY Identifier 2

Table 15. Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th Bits of the OUI	110010
3.[9:4]	Model Number	RO	Manufacturer's Model Number (14: Indicates RTL8218B)	011000
3.[3:0]	Revision Number	RO	Manufacturer's Revision Number	0001

8.5. Register 4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Note: Each time the link ability of the RTL8218B is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 16. Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8218B has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved	0
4.11	Asymmetric Pause	RW	1: Advertises that the RTL8218B has asymmetric flow control capability 0: No asymmetric flow control capability	0
4.10	Pause	RW	1: Advertises that the RTL8218B has flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	1: 100Base-T4 capable 0: Not 100Base-T4 capable (Permanently =0)	0

Reg.bit	Name	Mode	Description	Default
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	00001: IEEE 802.3	00001

Note 1: This Register 4 setting has no effect unless auto-negotiation is restarted or link down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted.

8.6. Register 5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after a successful Auto-negotiation.

Table 17. Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Technology Ability Field Received code word bit 12	0
5.11	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (Read only)	0
5.10	Pause	RO	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability. (Read only)	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner	0

Reg.bit	Name	Mode	Description	Default
5.[4:0]	Selector Field	RO	00001: IEEE 802.3	00000

8.7. Register 6: Auto-Negotiation Expansion

Table 18. Register 6: Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:5]	Reserved	RO	Ignore On Read	0
6.6	Receive Next Page Location Able	RO	1 = Received next page storage location is specified by bit (6.5) 0 = Received next page storage location is not specified by bit (6.5)	1
6.5	Received Next Page Storage Location	RO	1 = Link Partner next pages are stored in Register 8 0 = Link Partner next pages are stored in Register 5	1
6.4	Parallel Detection Fault	RO/LH	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
6.3	Link Partner Next Page Ability	RO	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	0
6.2	Local Next Page Ability	RO	1: RTL8218B is Next Page able	1
6.1	Page Received	RO/LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is Enabled, this bit means 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	0

8.8. Register 7: Auto-Negotiation Next Page Transmit

Table 19. Register 7: Auto-Negotiation Next Page Transmit

Reg.bit	Name	Mode	Description	Default
7.15	Next Page	RW	1: Another next page desired 0: No other next page to send	0
7.14	Reserved	RO	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
7.13	Message Page	RW	1: Message page	1
7.12	Acknowledge 2	RW	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	0
7.11	Toggle	RO	Toggle Bit	1
7.[10:0]	Message/ Unformatted Field	RW	Content of Message/Unformatted Page	00000000001

8.9. Register 8: Auto-Negotiation Link Partner Next Page Ability

Table 20. Register 8: Auto-Negotiation Link Partner Next Page Ability

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received Link Code Word Bit 15	0
8.14	Acknowledge	RO	Received Link Code Word Bit 14	0
8.13	Message Page	RO	Received Link Code Word Bit 13	0
8.12	Acknowledge 2	RO	Received Link Code Word Bit 12	0
8.11	Toggle	RO	Received Link Code Word Bit 11	0
8.[10:0]	Message/Unformatted Field	RO	Received Link Code Word Bit 10:0	0

8.10. Register 9: 1000Base-T Control

Table 21. Register 9: 1000Base-T Control

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test Mode Select 000: Normal mode 001: Test mode 1 – Transmit waveform test 010: Test mode 2 – Transmit jitter test in MASTER mode 011: Test mode 3 – Transmit jitter test in SLAVE mode 100: Test mode 4 – Transmitter distortion test 101, 110, 111: Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1: Enable MASTER/SLAVE manual configuration 0: Disable MASTER/SLAVE manual configuration	0
9.11	MASTER/SLAVE Configuration Value	RW	1: Configure PHY as MASTER during MASTER/SLAVE negotiation, only when 9.12 is set to logical one 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when 9.12 is set to logical one	1
9.10	Port Type	RW	1: Multi-port device 0: Single-port device	1
9.9	1000Base-T Full-Duplex	RW	1: Advertise PHY is 1000Base-T Full-Duplex capable 0: Advertise PHY is not 1000Base-T Full-Duplex capable	1
9.8	1000Base-T Half-Duplex	RW	1: Advertise PHY is 1000Base-T Half-Duplex capable 0: Advertise PHY is not 1000Base-T Half-Duplex capable	0
9.[7:0]	Reserved	RW	Reserved	0

8.11. Register 10: 1000Base-T Status

Table 22. Register 10: 1000Base-T Status

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH/SC	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1: Local receiver OK 0: Local receiver not OK	0
10.12	Remote Receiver Status	RO	1: Remote receiver OK 0: Remote receiver not OK	0
10.11	Link Partner 1000Base-T Full-Duplex	RO	1: Link partner is capable of 1000Base-T Full-Duplex 0: Link partner is not capable of 1000Base-T Full-Duplex	0
10.10	1000Base-T Half-Duplex	RO	1: Link partner is capable of 1000Base-T Half-Duplex 0: Link partner is not capable of 1000Base-T Half-Duplex	0
10.[9:8]	Reserved	RO	Reserved	0
10.[7:0]	Idle Error Count	RO/SC	Idle Error Counter The counter stops automatically when it reaches 0xFF.	0

8.12. Register 13: MMD access control register

Table 23. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
13.[15:14]	Function	RW	13.[15:14] 00: address 01: data, no post increment 10: data, post increment on read and writes 11: data, post increment on writes only	0
13.[13:5]	Reserved	RW	Write as 0, ignore on read.	0
13.[4:0]	DEVAD	RW	Device address	0

8.13. Register 14: MMD access address data register

Table 24. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
14.[15:0]	Address Data	RW	If 13.[15:14] = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the content of its address register	0

8.14. Register 15: Extended Status

Table 25. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
15.15	1000Base-X Full-Duplex	RO	1: 1000Base-X Full-Duplex capable 0: Not 1000Base-X Full-Duplex capable	0
15.14	1000Base-X Half-Duplex	RO	1: 1000Base-X Half-Duplex capable 0: Not 1000Base-X Half-Duplex capable	0
15.13	1000Base-T Full-Duplex	RO	1: 1000Base-T Full-Duplex capable 0: Not 1000Base-T Full-Duplex capable	1
15.12	1000Base-T Half-Duplex	RO	1: 1000Base-T Half-Duplex capable 0: Not 1000Base-T Half-Duplex capable	0
15.[11:0]	Reserved	RO	Reserved	0

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability may be affected. All voltages are specified reference to GND unless otherwise specified.

Table 26. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-10	+125	°C
DVDDIO, AVDDH, SVDDH Supply Voltage Referenced to DGND, AGND, and SGND	GND-0.3V	+3.63	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Referenced to DGND, AGND, SGND, and PLLGND	GND-0.3	+1.21V	V

9.2. Operating Range

Table 28. Operating Range

Parameter	Min	Typ	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDDIO, AVDDH, SVDDH Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Range	0.95	1.1	1.15	V

9.3. Power Consumption

9.4. RSGMII-Plus Mode Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
Idle (All ports are in link-down state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		75		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		449		mA
Total Power Consumption for All Ports	-		696.5		mW
1000Base-T Active (8 1000base-T Ports are in linkup state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		399		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		1383		mA
Total Power Consumption for All Ports	-		2699.7		mW
100Base-TX Active (84 100base-TX Ports are in linkup state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		196		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		633		mA
Total Power Consumption for All Ports	-		1279.8		mW
10Base-T Active (8 10base-T Ports are in linkup state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		283		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		452		mA
Total Power Consumption for All Ports	-		1385.9		mW

9.5. QSGMII Mode Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
Idle (All ports are in link-down state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		75		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		449		mA
Total Power Consumption for All Ports	-		696.5		mW
1000Base-T Active (8 1000base-T Ports are in linkup state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		400		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		1385		mA
Total Power Consumption for All Ports	-		2705		mW
100Base-TX Active (8 100base-TX Ports are in linkup state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		193		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		638		mA
Total Power Consumption for All Ports	-		1274.9		mW
10Base-T Active (8 10base-T Ports are in linkup state)					
Power Current for VDDH	I_{DVDDIO} , I_{AVDDH}, I_{SVDDH}		283		mA
Power Current for VDDL	I_{DVDDL} , I_{AVDDL}, I_{SVDDL}		453		mA
Total Power Consumption for All Ports	-		1386.9		mW

9.6. Clock Characteristics

Table 28. XTALI Characteristics

Parameter	Min	Typ	Max	Units
Frequency of XTALI	-	25	-	MHz
Frequency Tolerance of XTALI	-50		+50	ppm
Duty Cycle of XTALI	40		60	%
Rise Time of XTALI			12.5	ns
Fall Time of XTALI			12.5	ns
Jitter of XTALI			200	ps

Note: PLL generated clocks are not recommended as input to XTALI since they can have excessive jitter. Zero delay buffers are also not recommended for the reason.

9.7. Reset Characteristics

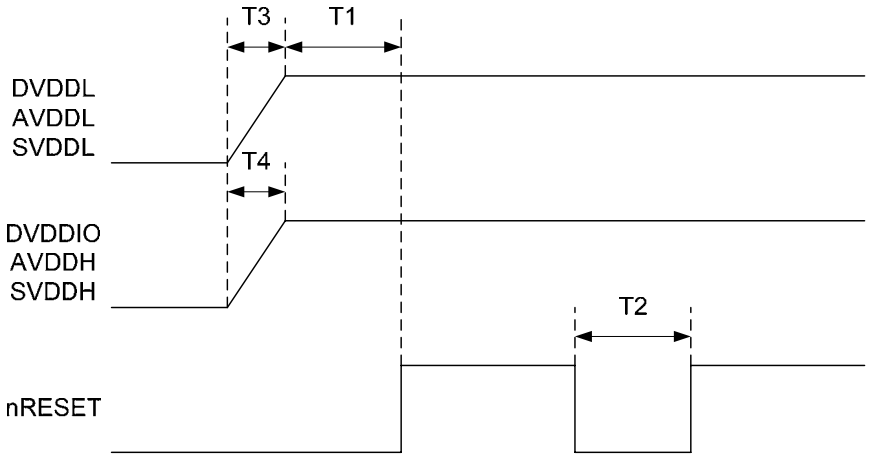


Figure 12. Reset Characteristics

Table 29. Reset Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	Reset Delay Time	10	-	-	ms
T2	Reset Low Time	10	-	-	ms
T3	VDDL Power Rise Settling Time	1	-	-	ms
T4	VDDH Power Rise Settling Time	1	-	-	ms

9.8. MDC/MDIO Interface Characteristics

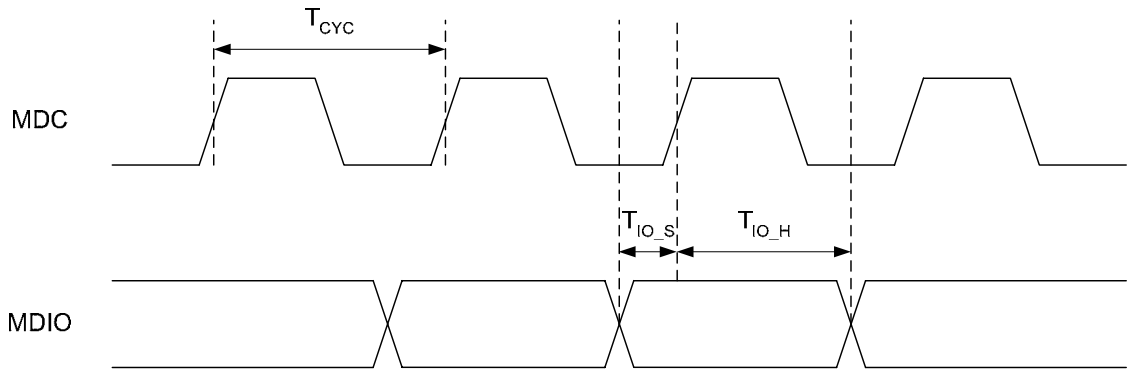


Figure 13. MDC/MDIO Interface Write Timing

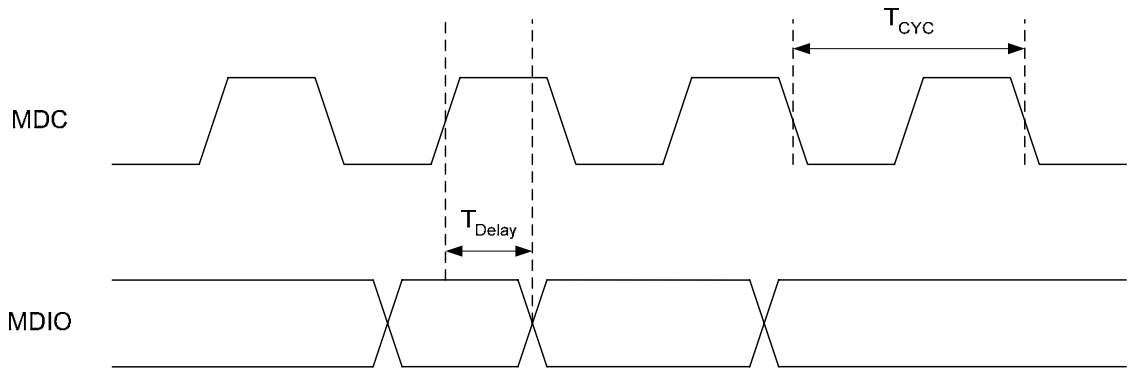


Figure 14. MDC/MDIO Interface Read Timing

Table 30. MDC/MDIO Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
T_{CYC}	MDC Clock Input Cycle	80	-	-	ns
T_{IO_S}	MDIO to MDC Rising Input Setup Time	10	-	-	ns
T_{IO_H}	MDIO to MDC Rising Input Hold Time	10	-	-	ns
T_{Delay}	MDC to MDIO Rising Output Delay				ns

9.9. RSGMII-Plus Characteristics

9.9.1. RSGMII-Plus Differential Transmitter Characteristics

Table 31. RSGMII-Plus Differential Transmitter Characteristics

Symbol	Description	Min	Typ	Max	Units	Note
UI	Unit Interval	199.94	200	200.06	ps	200 +/- 300ppm
T_X1	Eye Mask		-	0.2	UI	-
T_X1	Eye Mask		-	0.4	UI	-
T_Y1	Eye Mask	150			mV	-
T_Y2	Eye Mask			650	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	600	800	1300	mV	-
V_{TX-EYE}	Minimum TX Eye Width	0.6			UI	-
$V_{TX-JITTER}$	Output Jitter			0.35	UI	-
$V_{TX-RISE}$	Output Rise Time	0.15			UI	-
$V_{TX-FALL}$	Output Fall Time	0.15			UI	-
R_{TX}	Differential Resistance	80	100	120	Ohm	-
C_{TX}	AC Coupling Capacitor	80	100	200	nF	-
L_{TX}	Transmit Length in PCB			10	Inch	-

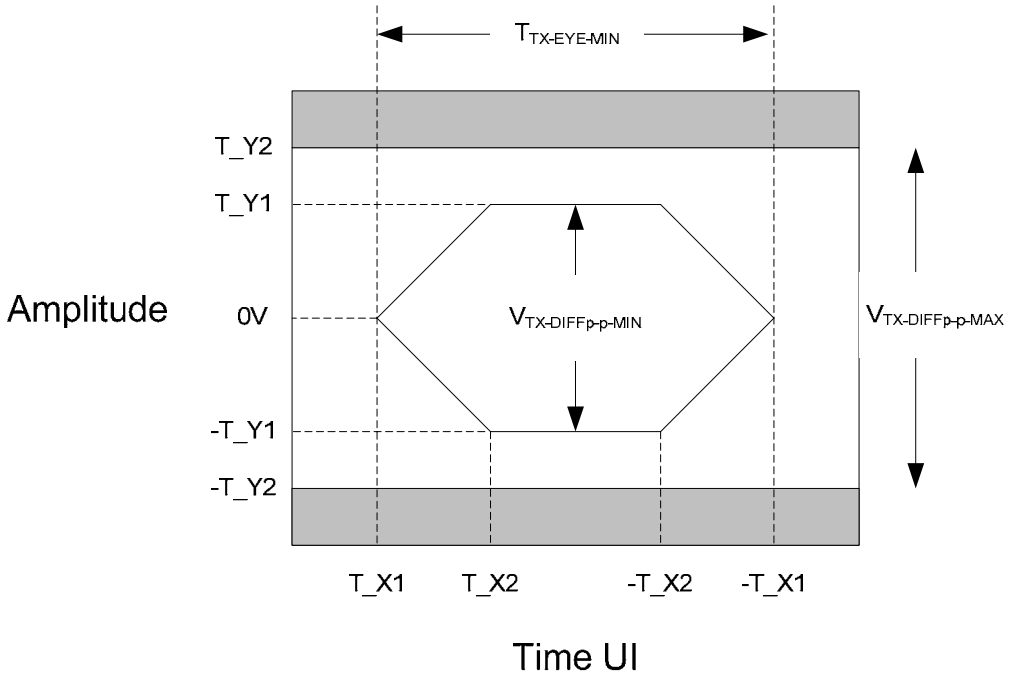


Figure 15. RSGMII-Plus Differential Transmitter Eye Diagram

9.9.2. RSGMII-Plus Differential Receiver Characteristics

Table 32. RSGMII-Plus Differential Receiver Characteristics

Symbol	Description	Min	Typ	Max	Units	Note
UI	Unit Interval	199.94	200	200.06	ps	200 +/- 300ppm
R_X1	Eye Mask		-	0.3	UI	-
R_Y1	Eye Mask	100			mV	-
R_Y2	Eye Mask			650	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200		1300	mV	-
V_{RX-EYE}	Minimum TX Eye Width	0.4			UI	-
$V_{TX-JITTER}$	Input Jitter Tolerance			0.6	UI	-
R_{TX}	Differential Resistance	80	100	120	Ohm	-

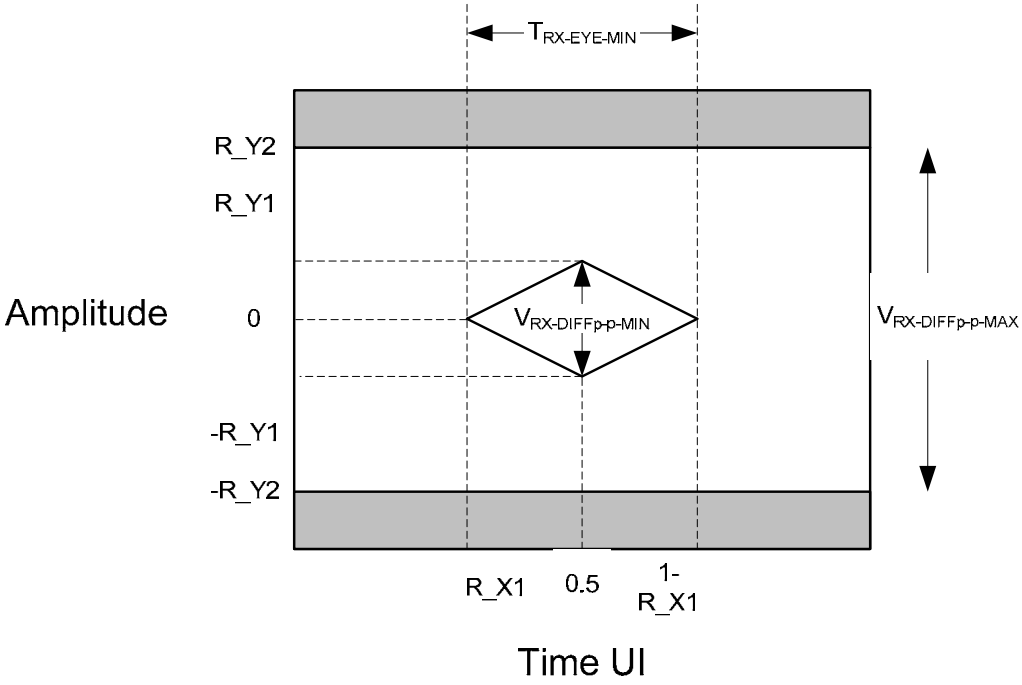


Figure 16. RSGMII-Plus Differential Receiver Eye Diagram

9.10. QSGMII Characteristics

9.10.1. QSGMII Differential Transmitter Characteristics

Table 33. QSGMII Differential Transmitter Characteristics

Symbol	Description	Min	Typ	Max	Units	Note
UI	Unit Interval	199.94	200	200.06	ps	200 +/- 300ppm
T_X1	Eye Mask		-	0.2	UI	-
T_X1	Eye Mask		-	0.4	UI	-
T_Y1	Eye Mask	150			mV	-
T_Y2	Eye Mask			650	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	600	800	1300	mV	-
V_{TX-EYE}	Minimum TX Eye Width	0.6			UI	-
$V_{TX-JITTER}$	Output Jitter			0.35	UI	-
$V_{TX-RISE}$	Output Rise Time	0.15			UI	-
$V_{TX-FALL}$	Output Fall Time	0.15			UI	-
R_{TX}	Differential Resistance	80	100	120	Ohm	-
C_{TX}	AC Coupling Capacitor	80	100	200	nF	-
L_{TX}	Transmit Length in PCB			10	Inch	-

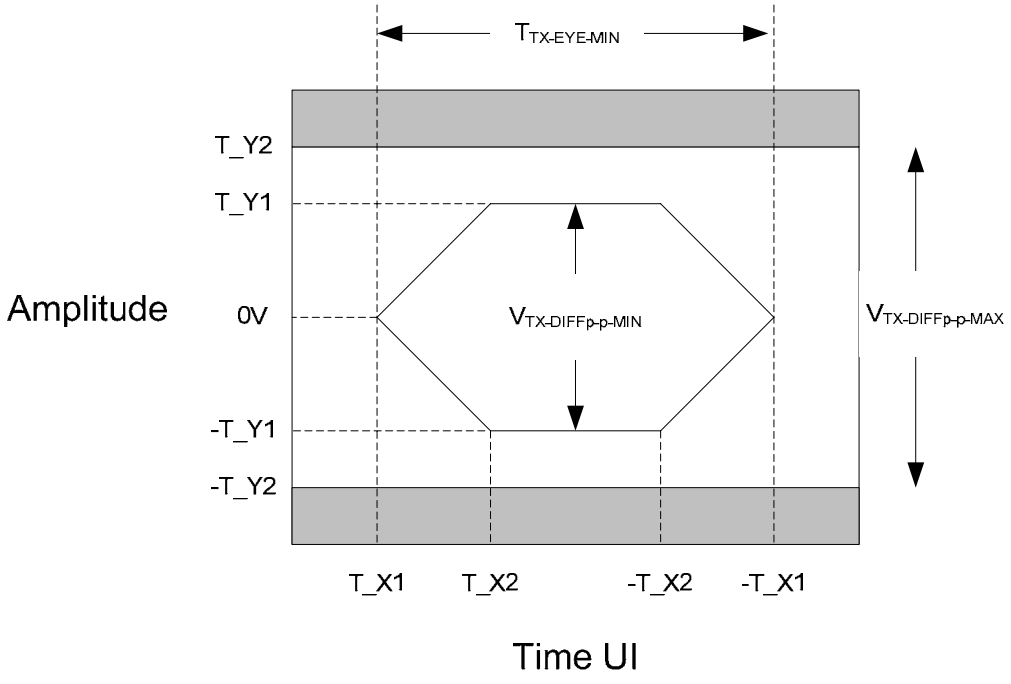


Figure 17. RQGMII Differential Transmitter Eye Diagram

9.10.2. QSGMII Differential Receiver Characteristics

Table 34. QSGMII Differential Receiver Characteristics

Symbol	Description	Min	Typ	Max	Units	Note
UI	Unit Interval	199.94	200	200.06	ps	200 +/- 300ppm
R_X1	Eye Mask		-	0.3	UI	-
R_Y1	Eye Mask	100			mV	-
R_Y2	Eye Mask			650	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200		1300	mV	-
V_{RX-EYE}	Minimum TX Eye Width	0.4			UI	-
$V_{TX-JITTER}$	Input Jitter Tolerance			0.6	UI	-
R_{TX}	Differential Resistance	80	100	120	Ohm	-

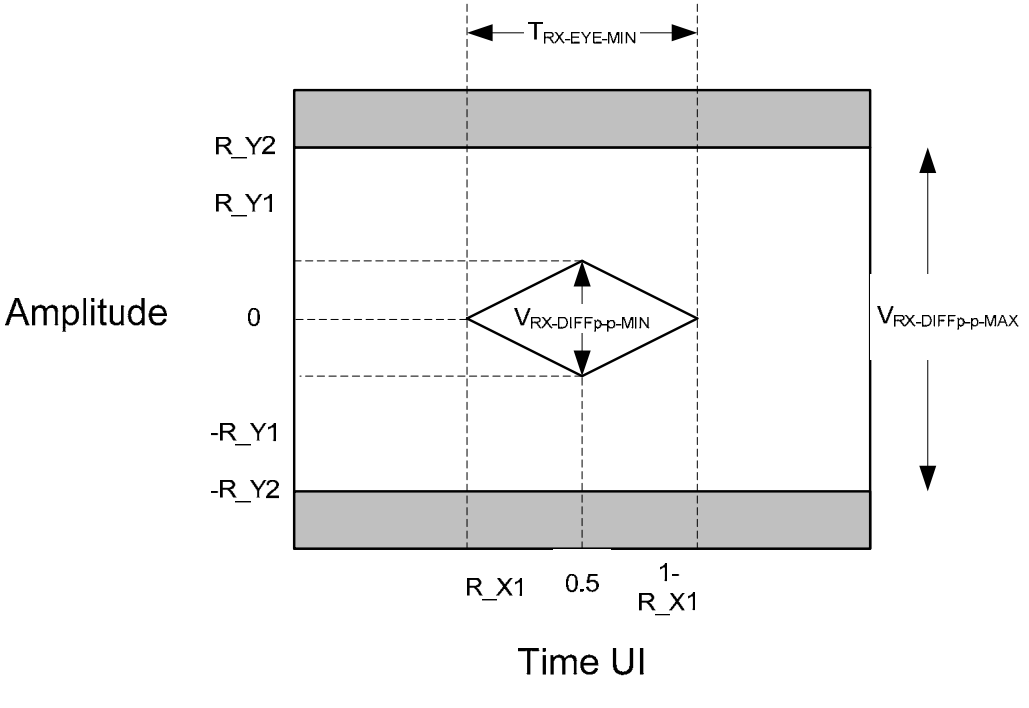


Figure 18. QSGMII Differential Receiver Eye Diagram

9.11. LED Characteristics

9.11.1. Serial LED Timing

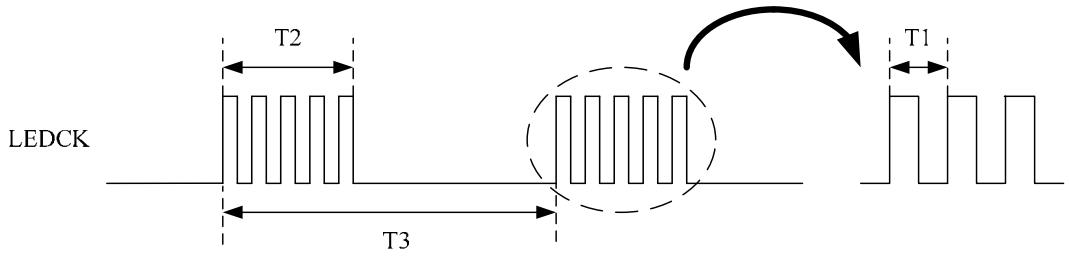


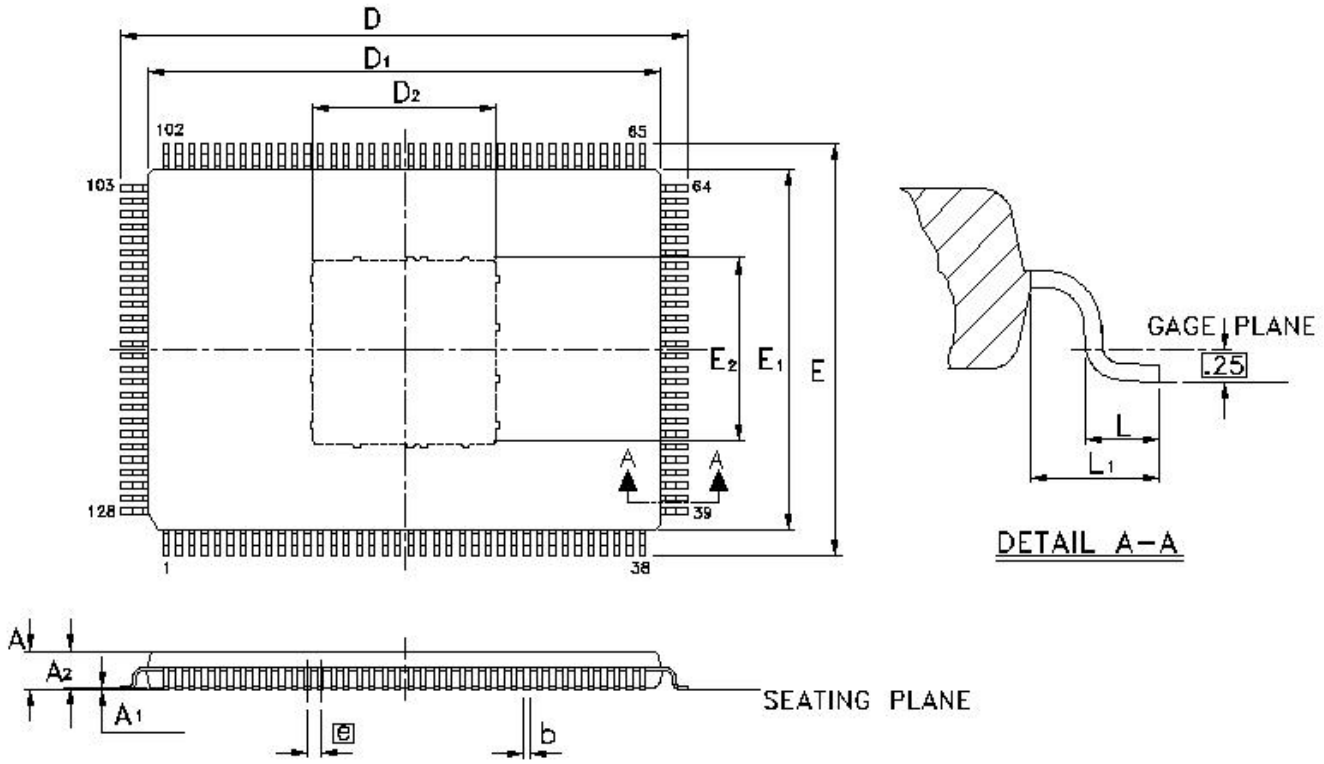
Figure 19. Serial LED Timing

Table 35. Serial LED Timing

Symbol	Description	Min	Typ	Max	Units
T1	Serial LED Clock Cycle Time	-	192	-	ns
T2	Serial LED Clock On/Off Duration	-		-	us
T3	Serial LED Burst Cycle Time	-	32	-	ms

10. Mechanical Dimensions

10.1. LQFP-128 E-PAD Package



10.2. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.2	0.27	0.007	0.009	0.011
D	22.00BSC			0.866BSC		
D_1	20.00BSC			0.787BSC		
D_2 / E_2	5.6	6.60	7.50	0.220	0.260	0.295
E	16.00BSC			0.630BSC		
E_1	14.00BSC			0.551BSC		
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm).
2. REFERENCE DOCUMENTL：JEDEC MS-26.

11. Ordering Information

Table 36. Ordering Information

Part Number	Package	Status
RTL8218B-CG	LQFP-128 EPAD Green Package	

Note: See page 6 package identification.

Figure 20. RTL8218B Package Identification

Marking Location	Description	Status
RTL8218B	Model Name	
LLLLLLL	Lot Number	
G	Green Package	
XXX	Date Code	

Note: package identification.

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