74LS375
Latch

Quad Bistable Latch
Product Specification

Logic Products

FEATURES

- **Quad transparent latch**
- **Complementary outputs**

DESCRIPTION

The '375 has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one set-up time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched output remains stable as long as the enable is LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS375	12ns	6.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS375N
Plastic SO-16	N74LS375D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$D_0 - D_3$	Inputs	1LSul
E_{0-1}, E_{2-3}	Inputs	4LSul
All	Outputs	10LSul

NOTE:
Where a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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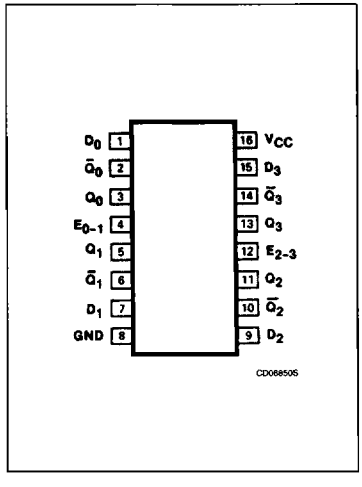
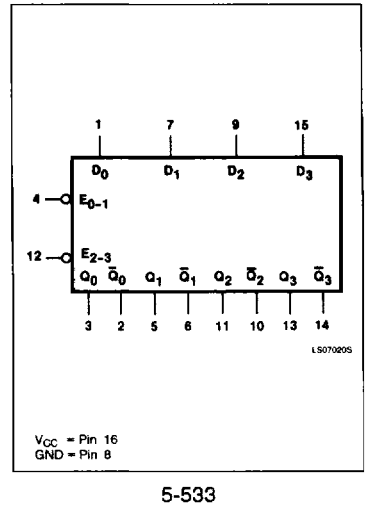
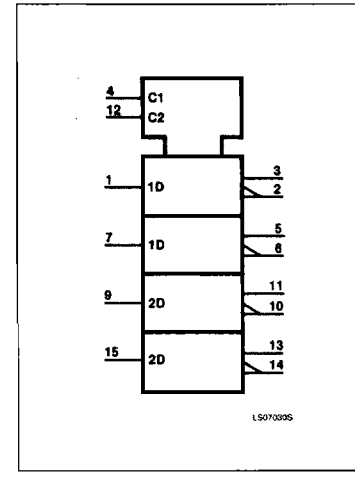
PIN CONFIGURATION



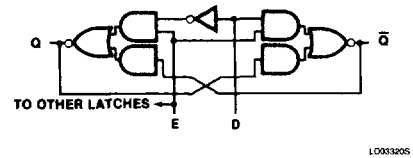
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (Each Latch)



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	$\overline{Q}$
Data Enabled	H H	L H	L H	H L
Data Latched	L	X	q	$\overline{q}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care.
q = Lower case letters indicate the state of referenced output one set-up time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output voltage			−400	µA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74LS375			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.35	0.5	V
			I_{OL} = 4mA		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	D_0-D_3 inputs			0.1	mA
			E_{0-1},E_{2-3} Inputs			0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	D_0-D_3 inputs			20	μA
			E_{0-1},E_{2-3} Inputs			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	D_0-D_3 inputs			−0.4	mA
			E_{0-1}, E_{2-3} inputs			−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			6.3	12	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} MAX +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Test I_{CC} with all inputs grounded and all outputs open.

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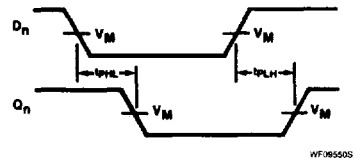
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		27 17	ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		20 15	ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		27 25	ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		30 15	ns

AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

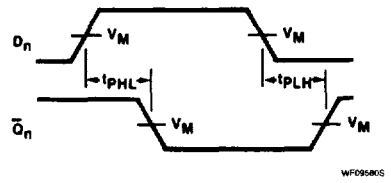
PARAMETER		TEST CONDITIONS	74LS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 3	20		ns
t_S	Setup time, Data to Enable	Waveform 4	20		ns
t_h	Hold time, Data to Enable	Waveform 4	0		ns

AC WAVEFORMS



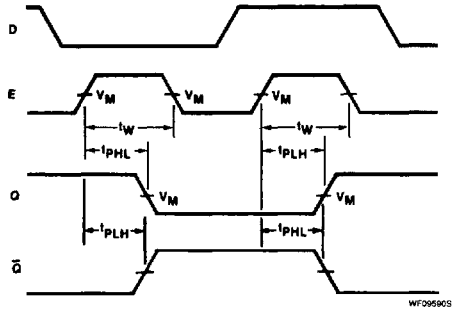
V_M = 1.35 for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 1. Propagation Delay Data To Q Outputs



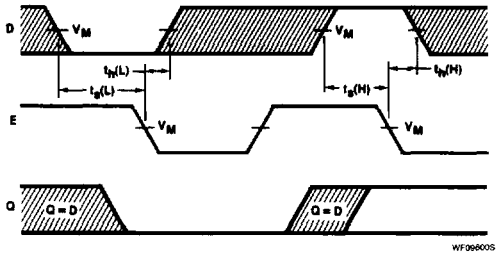
V_M = 1.35 for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 2. Propagation Delay Data To $\overline{Q}$ Outputs



V_M = 1.35 for 74 and 74S; V_M = 1.3V for 74LS.

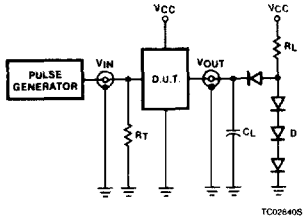
Waveform 3. Latch Enable To Output Delays And Latch Enable Pulse Width



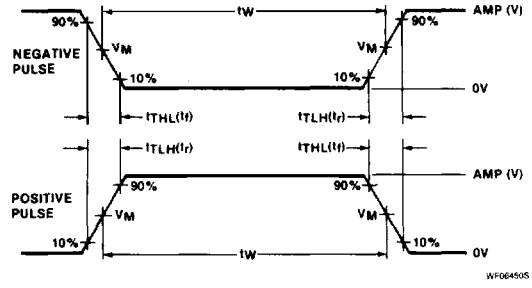
V_M = 1.35 for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Data Set-up And Hold Times

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns