FUJITSU

CMOS SINGLE CHIP 4-BIT MICROCOMPUTER WITH A/D CONVERTER AND VFD

MB88510B SERIES

TM334-A871: January 1987

CMOS SINGLE CHIP 4-BIT MICROCOMPUTER WITH A/D CONVERTER AND VFD DRIVER PORT

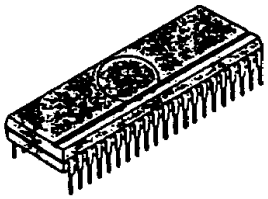
The Fujitsu MB88510B series CMOS single-chip 4-bit microcomputer family is a up grade version of the conventional MB88500 series. Its architecture and instruction set are super set of the MB88500 series, add on the A/D converter and VFD driver port.

The MB88510B series consists of the MB88514B, MB88515B, MB88516B, and MB88517B. This series contain max. 8K by 8-bit mask ROM (program memory), a 256 by 4-bit static RAM (data memory), max. 54 I/O lines (including a serial port), max. 8-bit resolution 8 channel A/D converter, max. 25 VFD driver port an 8-bit timer/counter, and a clock generator. They are fabricated by the silicon-gate CMOS process, packaged in a 64 pin shrink DIP or 42-pin plastic standard DIP. They operate with a +5 V power supply and a 6 MHz clock with a prescaler (minimum instruction execution time is 2.0µs) over the temperature range of -40 °C to +85 °C.

CMOS technology allows the device to operate with low power dissipation (6 mA max. at 1 MHz), and further the standby function enables data retention with lower current (15 µA max. at V_{CC} = 6 V).

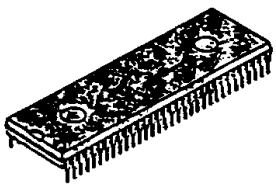
For user's development of the MB88510B series based system, Fujitsu provides the MB88400/500 cross-assembler and host-emulator which run on the CP/M-86 or PC-DOS machines (cross-assembler also run on the Intellec series III MDS), and the MB2115 series evaluation board system, and the MB88518B for MB88514B/MB88515B/MB88516B, MB88PG517B for MB88517B piggyback EPROM evaluation devices which have external 8K x 8-bit EPROM (MBM27C64). These development tools enables users to minimize their development time and cost.

MB88514B-P-SH
MB88515B-P-SH
MB88516B-P-SH



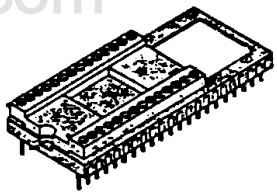
64-PIN PLASTIC SHRINK DIP
(DIP-64P-M01)

MB88517B-P



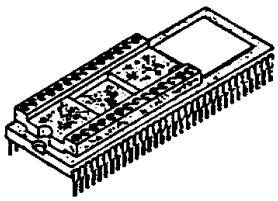
42-PIN PLASTIC STANDARD DIP
(DIP-42P-M01)

MB88518B-C



64-PIN CERAMIC SHRINK MODULE
(MDP-64C-P01)

MB88PG517B-C



42-PIN CERAMIC MODULE
(MDP-42C-P04)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- CMOS Single-chip 4-bit Microcomputer

- Program Memory:
  - o MB88514B : 6 K x 8-bit mask ROM
  - o MB88515B : 8 K x 8-bit mask ROM
  - o MB88516B, MB88517B: 4 K x 8-bit mask ROM

- Data Memory:
  - o 256 x 4-bit static RAM

- Max. 54 I/O Lines:
  - o MB88514B, MB88515B:
    - -R-Port: Four 4-bit parallel I/O, 16 individual input/output ports
    - -E-Port: Nine 4-bit and a 2-bit parallel output, six 4-bit parallel input, 38 individual output. Following E-Port have another functions:
      - E0 -E24 : P-Channel high voltage(-35V) parallel output for VFD direct drive
      - E28-E35 : Analog inputs
      - E24-E27, E36, : Serial I/O interrupt input, timer/counter input, timing output, standby release input

  - o MB88516B:
    - -R-Port: Three 4-bit and a 1-bit parallel I/O, 13 individual input/output ports
    - -E-Port: Six 4-bit and a 2-bit parallel output, three 4-bit and a 2-bit parallel input, 14 individual output: Following E-Port have another functions:
      - E0-E7, E12-E14: P-Channel high voltage(-35V) parallel output for VFD direct drive
      - E28-E35 : Analog inputs
      - E24-E27, E36, : Serial I/O interrupt input, timer/counter input, timing output, standby release input

  - o MB88517B:
    - -R-Port: Three 4-bit and a 1-bit parallel I/O, 13 individual input/output ports
    - -E-Port: Four 4-bit, a 3-bit, and a 2-bit parallel output, a 4-bit, a 3-bit, and a 2-bit parallel input, 38 individual output. Following E-Port have another functions:
      - E0-E7, E12-E18: P-Channel high voltage(-35V) parallel output for VFD direct drive
      - E28-E31 : Analog inputs
      - E17, E26, E27,: R15, R11 : Serial I/O interrupt input, timer/counter input, timing output, standby release input

- Four Selectable Output Port Types for E- and R-Ports with Mask Option, Every 4-bit Port:
  - o Standard open-drain
  - o Standard pullup
  - o High-current open-drain
  - o High-current pullup

- 8-bit Programmable Successive Approximation Type A/D Converter with Sample-Hold Circuit:
  - o MB88514B, MB88515B, MB88516B: 8 channel
  - o MB88517B : 4 channel

FEATURES (Continued)

- Mask Option Two Selectable 8 Analog Inputs (MB88514B, MB88515B):
  - o 4 high impedance analog/digital inputs and 4 standard analog inputs/ digital I/O
  - o 8 standard analog inputs/digital I/O

- 8-bit Programmable Timer/Counter with Auto-Loading function/Two Clock Modes:
  - o Internal clock (Timer)
  - o External clock (Counter)

- Software Selectable Serial I/O with 4-/8-bit Serial Buffer/Three Clock Modes:
  - o Internal clock
  - o External clock
  - o Software clock

- On-chip Clock Generator with 2 Mask Options:
  - o External crystal/ceramic resonator or external clock drive
  - o External RC-network or external clock drive

- Mask Option Divide-by-two Clock Prescaler for Expanding Clock Range

- Single Level four Prior Source Maskable Interrupt:
  - o External
  - o Clock
  - o Timer/counter overflow
  - o Serial buffer full/empty

- 8-nesting Levels for Subroutine Calls

- Instruction Set : Upward compatible with the MB88500 series
  - o Number of instructions : 81 MB88514B/5B, 79:MB88516B/7B
  - o Instruction length/cycle: 1, 2, or 3 byte(s)/1 , 2, or 3 cycle
  - o Execution time : 2.0 µs min. at 3 MHz clock without prescaler (or 6MHz clock with prescaler)

- On-chip Power-on Reset Circuit

- Mask-option Standby Function:
  - o No standby function
  - o Software-initiation standby function

- Two Mask option Output States During Standby:
  - o Hold
  - o High impedance

- Two Software Selectable Oscillator States During Standby:
  - o Idle
  - o Stop

- Mask Option Standby-off Reset

- Mask Option Watch-dog Timer Function

FEATURES (Continued)

- Low Power Dissipation:
  - o 6 mA at V_{CC} = 5.5 V at fc = 1 MHz max. (Active mode)
  - o15 µA at V_{CC} = 6.0 V at fc = 0 MHz max. (Standby mode)

- Power Supply
  - o 4.5V to 5.5V (Active mode)
  - o 3.5V to 6.0V (Standby mode)

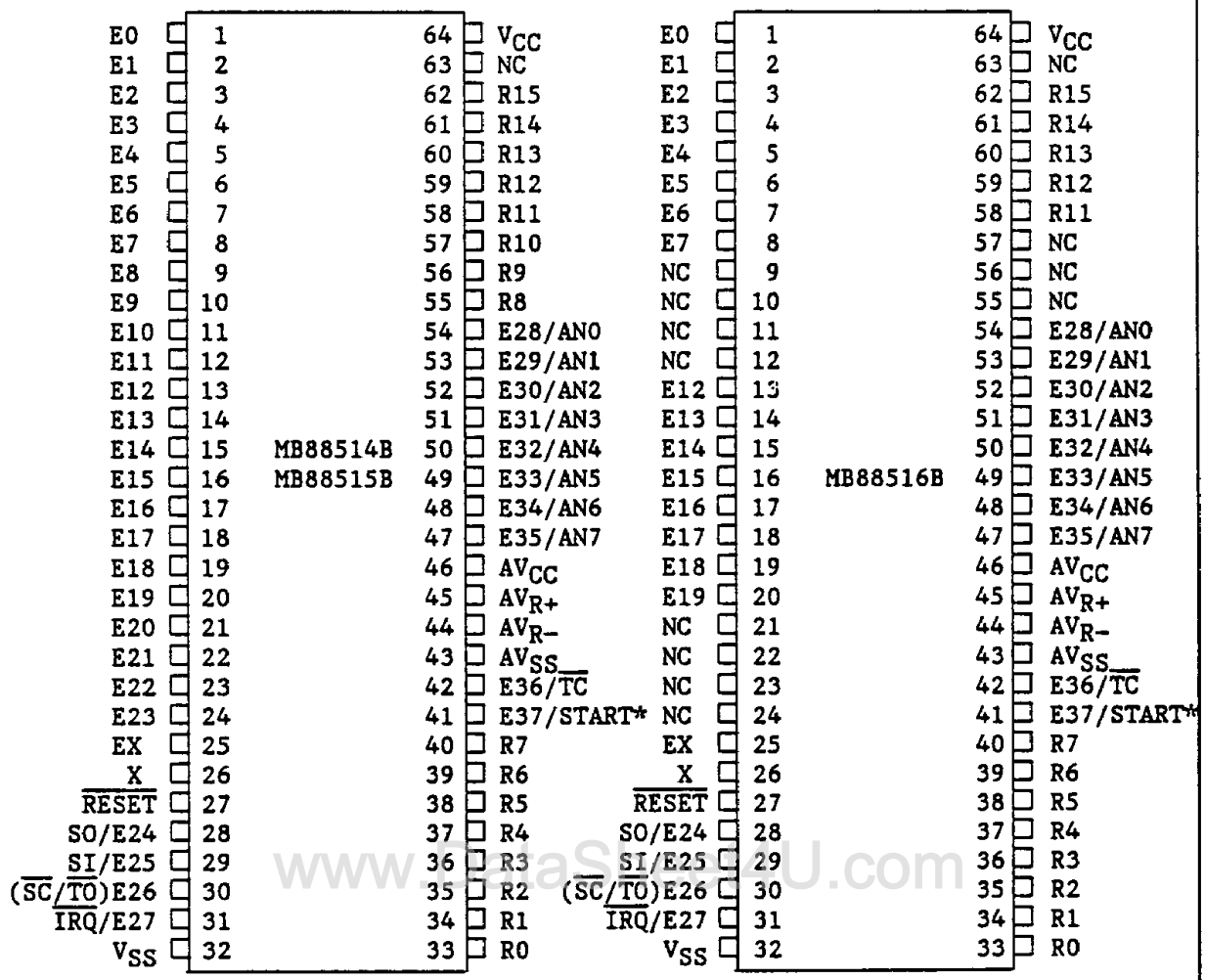
- Wide operation temperature range: T_A= -40 °C to +85 °C

- Silicon Gate CMOS Technology

- Two Package Options:
  - o 64-pin plastic shrink DIP: MB88514B, MB88515B, and MB88516B (Suffix -PSH)
  - o 42-pin plastic standard DIP: MB88517B (Suffix -P)

- Powerful Development Support:
  - o Intellec Series III MDS cross-assembler (SM05215-A010)
  - o CP/M-86 or PC-DOS cross-assembler (SM07415-A012/SMXXXXX-XXXX)
  - o CP/M-86 or PC-DOS host emulator software for monitoring evaluation board and symbolic debugging (SM07415-G022/XXXXXXX-XXXX)
  - o MB2115 series evaluation board (-01, -02, -04, 34, -96, and -92 for MB88514B/5B/6B, MB2115-01, -02, -04, and -38 for MB88517B) for software debugging
  - o MB88518B for MB88514B/5B/6B and MB88PG517B for MB88517B CMOS piggyback EPROM evaluation devices

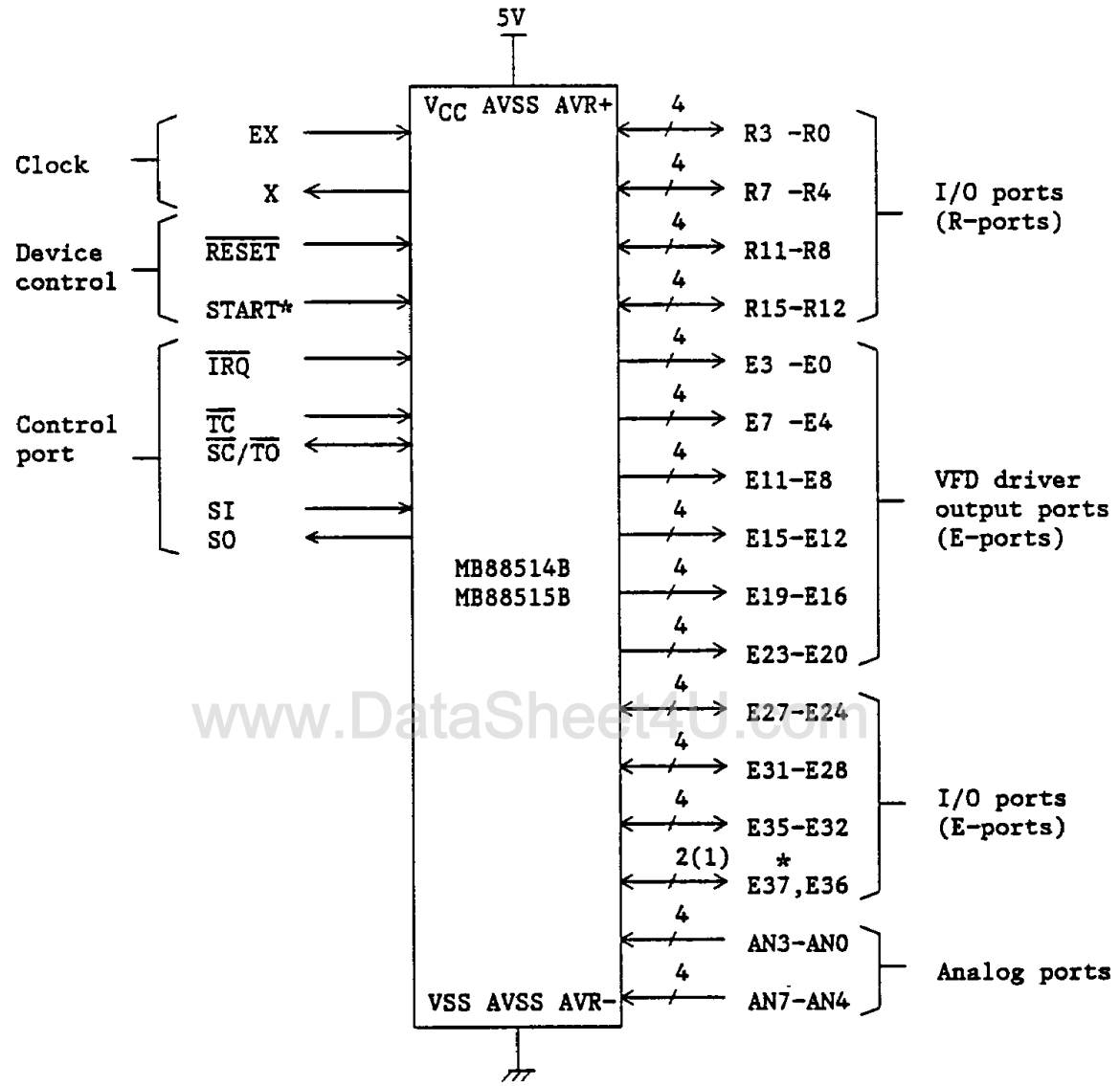
Fig. 1: PIN ASSIGNMENT



* Either E37 or START is selected using mask option.

** Either E18 or START is selected using mask option.

Fig. 2: MB88514B AND MB88515B LOGIC SYMBOL



* If selected standby by mask option, pin 41 is START pin. If not, pin 41 is E37 pin.

Fig. 3: MB88514B AND MB88515B LOGIC SYMBOL

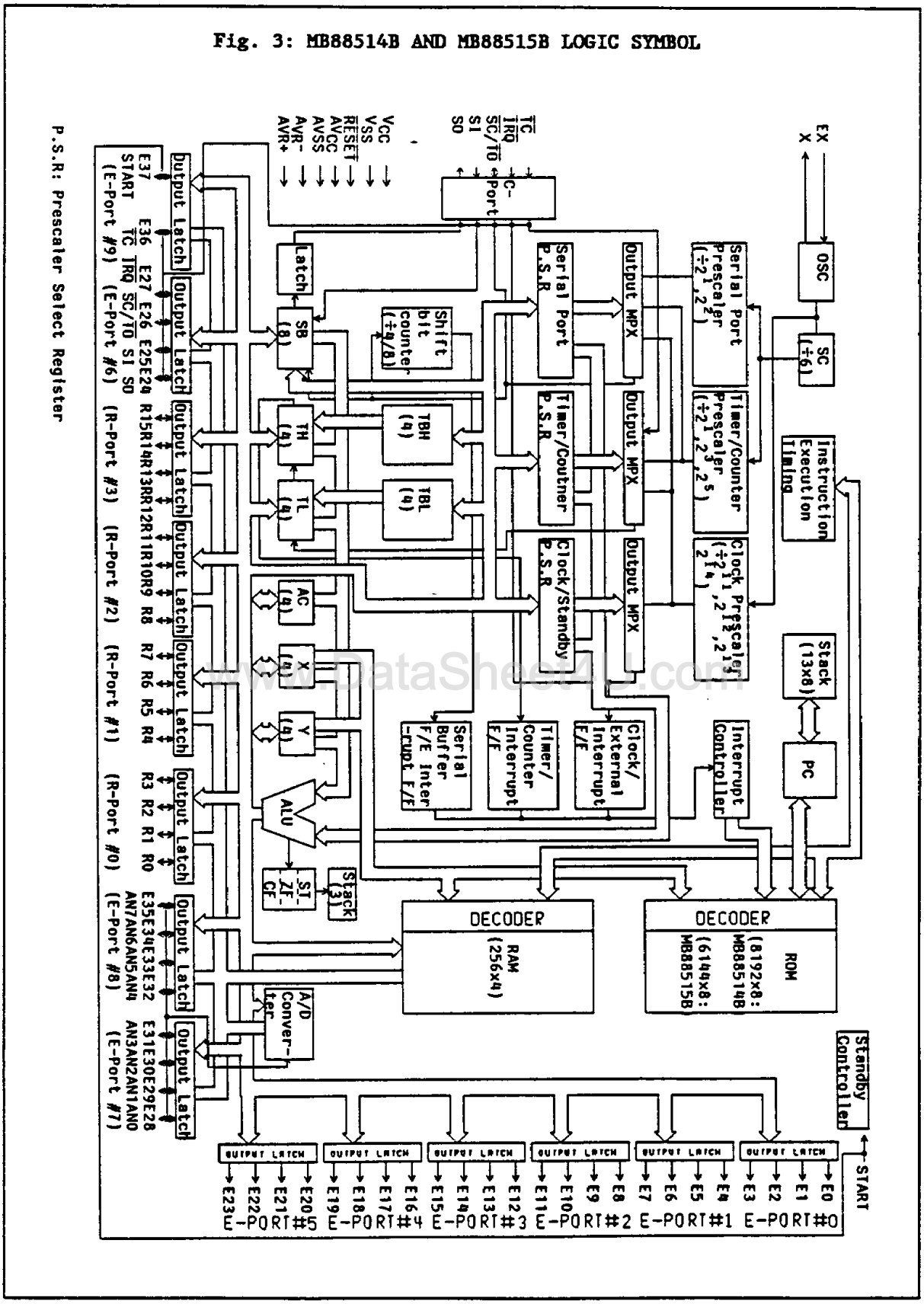
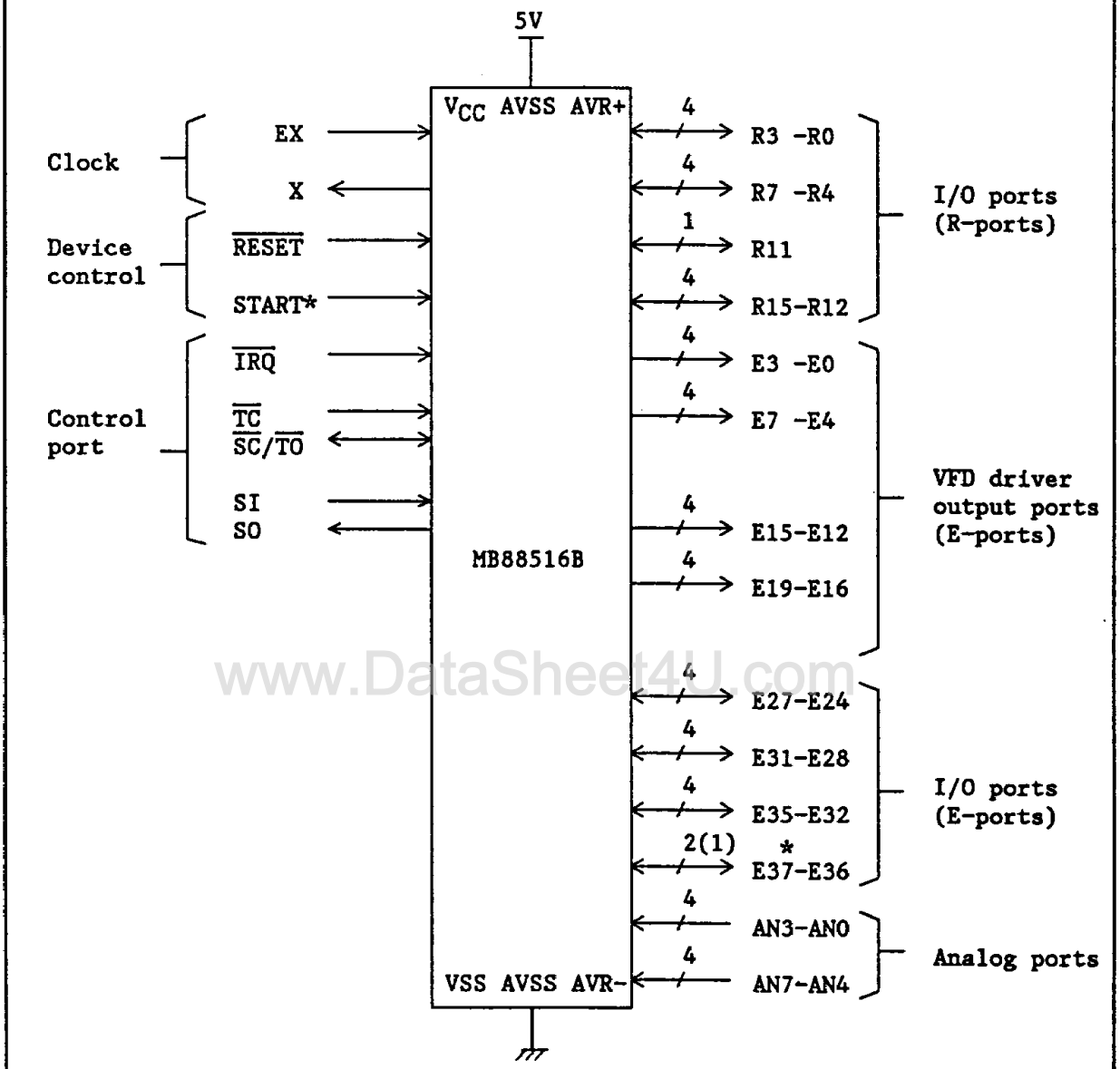


Fig. 4: MB88516B LOGIC SYMBOL



* If selected standby by mask option, pin 41 is START pin. If not, pin 41 is E37 pin.

Fig. 5: MB88516B LOGIC SYMBOL

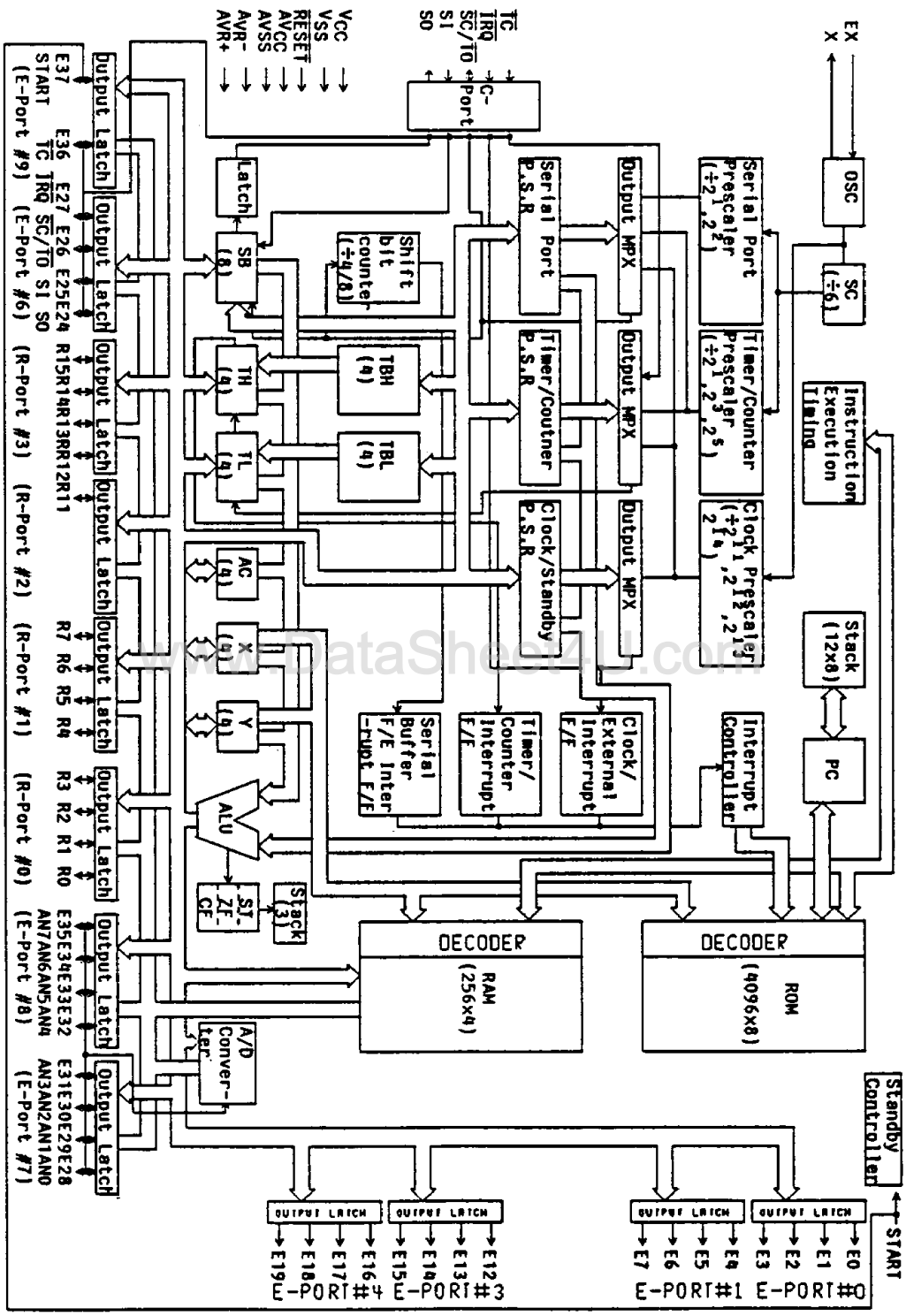
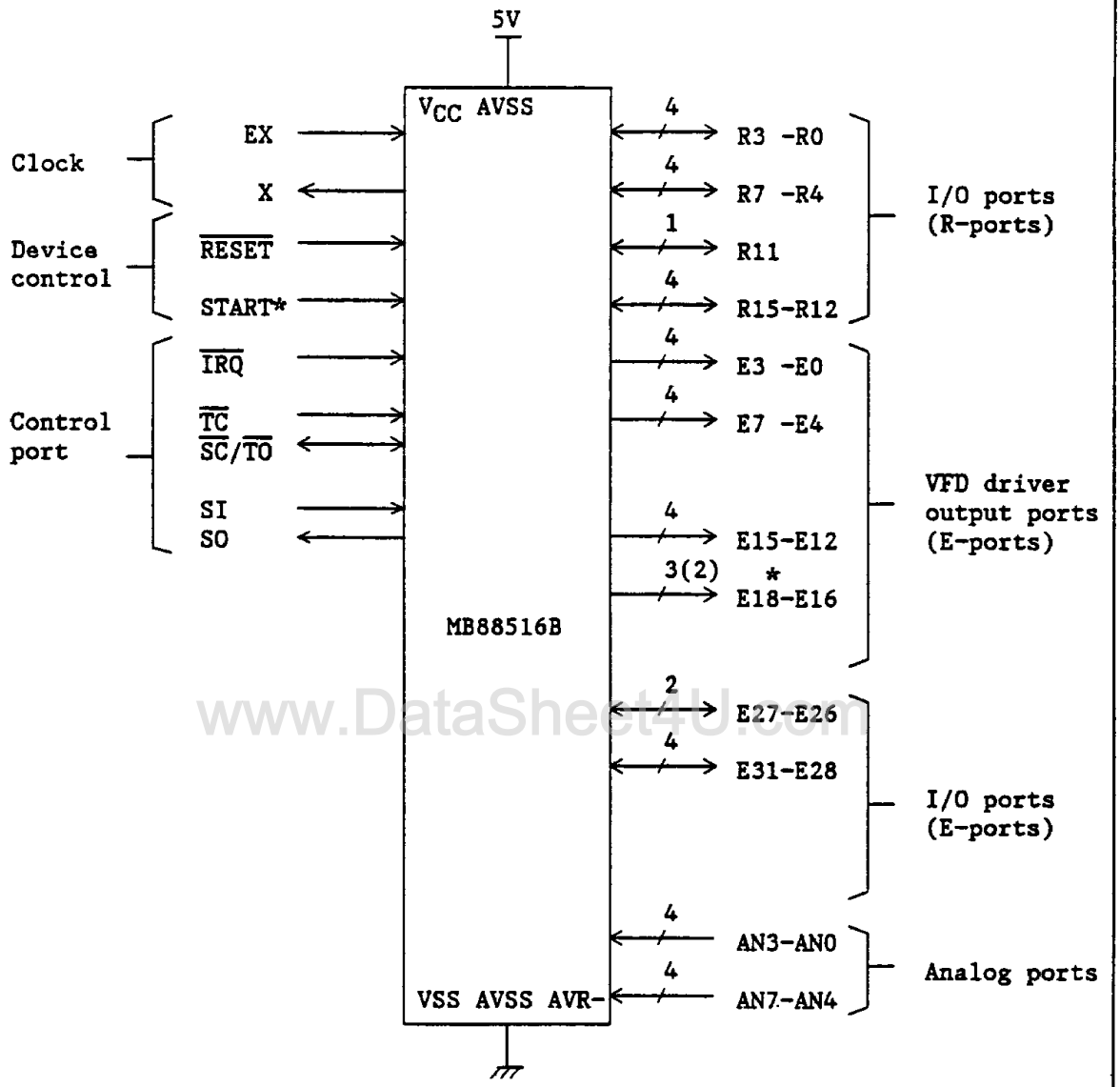
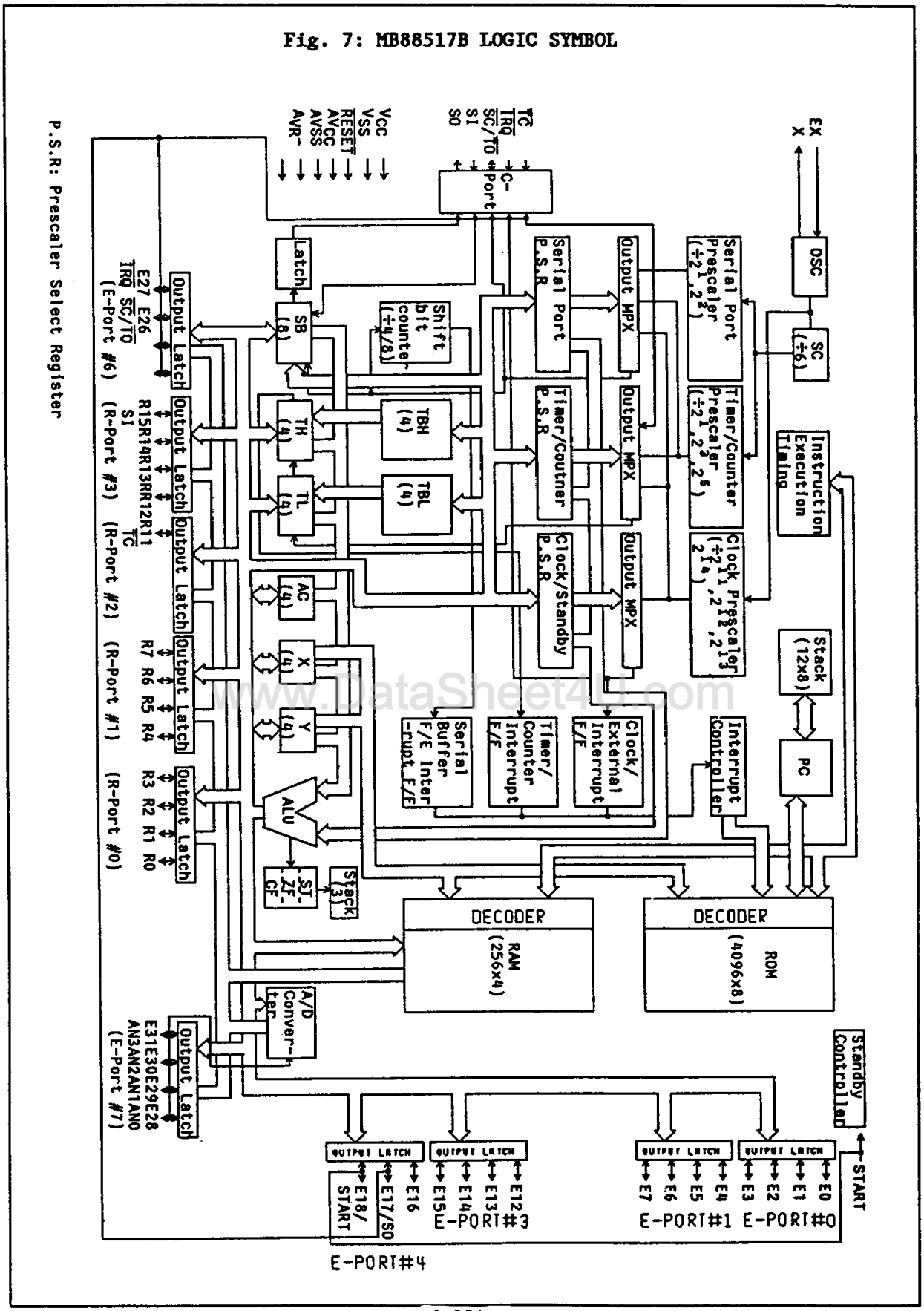


Fig. 6: MB88517B LOGIC SYMBOL



* If selected standby by mask option, pin 15 is START pin. If not, pin 15 is E18 pin.

Fig. 7: MB88517B LOGIC SYMBOL



PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB88510B Series.

Table 1: PIN DESCRIPTION

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
• Power Supply					
V_{CC}	64	64	42	–	+5V DC power supply pin.
V_{SS}	32	32	21	–	Ground pin.
• Clock					
EX	25	25	16	I	**Oscillator Input:** Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation types can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ceramic oscillator is selected, and a hysteresis input when the RC-network oscillator is selected.
X	26	26	17	O	**Oscillator Output:** Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillator types can be selected using mask option. When an external oscillator is used, the X pin should be left open.
• Device Control					
$\overline{RESET}$	27	27	18	I	**Reset:** This pin function as an external reset input or power-on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedely stops the MCU's operation, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{RESET}$ pulse must be low for at least two instruction cycles while the oscillator is stably running after power-on. This pin is a hysteresis input with an internal pullup resistor. An external capacitor from the $\overline{RESET}$ pin to the VSS pin (and the internal pull-up resistor),

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
• Device Control (Continued)					
$\overline{\text{RESET}}$	27	27	18	I	whose time constant should be greater than the reset time required (12 clock periods) composes the external reset circuit.
				I/O	Power on reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the VCC voltage after power on outputs a low level on the RESET pin, and them automatically returns high 2^{18} clock periods after the oscillator starts by power on.
					This pin is a hysteresis input with an internal pullup resistor.
START	41	41	15	I	**Start**: A standby release input to the internal standby control and status registers that control and monitor the on-chip standby control circuit. A high level on the START pin during the standby mode sets the standby release flag (STF) in the standby status register, resets the standby enable flag (STBE) in the standby control register, and triggers the standby release sequence to return the MCU to the active mode. Before the START pulse is applied, the VCC voltage must return to the active operation range when the battery backup is used. Also, the START pin must be low before the standby mode is initiated.
					The START pin state (logical level) is reflected in the standby release input (START) flag (STIF) in the stand-by status register, regardless of during the standby mode or active mode, and besides even when the standby function is not implemented using mask option. Therefore, the START pin state can be sensed by reading the standby status register using IN instruction (with Y=8).
					This pin is a hysteresis input with an internal pull-down resistor.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
• C-Port					
$\overline{IRQ}$	31	31	20	I	**Interrupt Request**: A maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of the $\overline{IRQ}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register regardless of enabling or disabling the external interrupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{IRQ}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{IRQ}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pullup resistor.
$\overline{TC}$	42	42	37	I	**Timer/Counter**: An external count clock input to the on-chip 8-bit timer/counter. The falling edge of the $\overline{TC}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming the timer/counter prescaler select register using OUT instruction (with Y = B). Also, the TC pin state (logical level), which is reflected in the timer/counter input flag (TCIF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (counter mode, is testable by reading the prescaler select register using IN instruction (with Y = B). (When $\overline{TC}$ = L, TCIF = 1; otherwise TCIF = 0.) This pin is inactive as a count clock input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pullup resistor.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
• C-Port (Continued)					
$\overline{SC}/\overline{TO}$	30	30	19	I/O	**Shift Clock/Timing Output**: One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), or synchronous timing output ($\overline{TO}$) is enabled using EN instruction.
				I	$\overline{SC}$:1)Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is not selected or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input. 2)Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization.
				O	$\overline{TO}$:Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output. This pin is a hysteresis input with an internal pullup resistor
SI	29	29	41	I	**Serial Data Input**: Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also,

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
• C-Port (Continued)					
SI	29	29	41	I	the SI pin state (logical level) is reflected in the serial data input flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instruction (with Y = A).
SO	28	28	14	O	**Serial Data Output**: Data output with latch of the on-chip serial port. The falling edge of the external (SC) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appears on the SO pin. This pin is a CMOS pullup output, and is set high by reset.
• I/O Port					
R3 -R0, R7 -R4, R11-R8, R15-R12	36-33, 40-37, 58-55, 62-59	36-33, 40-37, 58, 62-59	25-22, 29-26, 37, 41-38	I/O	**R-Port**: This port functions as four 4-bit parallel input (non-latched)/output (latched) ports, or 16 individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit port is named R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R15-R12), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of R-Ports #0 to #3 by OUT instruction. 4-bit data on the addressed port is input into the accumulator by IN instruction, and further in the R-Port #3 by INK instruction. (Before IN instruction, the port to be addressed must be set up to "1" state (input) mode).) Individual I/O: Each line from R15 to R0 is indirectly addressed by the Y-register (Bit #). The addressed line is individually set/reset by SETR/RSTR instruction, and especially each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. The addressed line is individually testable by TSTR instruction, and each line of R-Port #2 (R11-R8) is directly testable in particular by TSTD

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
• I/O Ports (continued)					
R3 -R0, R7 -R4, R11-R8, R15-R12	36-33, 40-37, 58-55, 62-59	36-33, 40-37, 58, 62-59	25-22, 29-26, 37, 41-38	I/O	instruction. (Before the TSTR and TSTD instructions, the line to be addressed must be set up to "1" (input mode).) Refer to Table 4 User mask options for available making option.
E3 -E0 E7 -E4 E11-E8 E15-E12 E19-E16 E23-E20 E24	4 -1 8 -5 12-9 16-13 20-17 24-21 28	4 -1 8 -5 - 16-13 20-17 - 28	4 -1 8 -5 - 12-9 15-13 - -	O	E-ports: This port function as six 4-bit and a 1-bit parallel output latched ports. These output ports are high-voltage open open-drain (-35V) P-channel open-drain outputs for VFD. Parallel output: Each 4-bit port is named E-Port #0 (E3-E0), E-Port #1 (E7-E4), .. E-Port #5 (E23-R20), and E-Port # 6 (E24) and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of E-Ports #0 to #6 by OUTX instruction, and further in the E-Port #0 by OUTP instruction. Individual output: A data of the accumulator is output to the each line from E24 to E0 by ANDX, ORX, and OUTX instruction. Refer to Table 4 User mask options for available making option.
E27-E25 E31-E28 E35-E32 E37-E36	31-29, 51-54, 47-50, 41,42	31-29, 51-54, 47-50, 41,42	20,19, 33-36 - -	I/O	E-ports: This port function as two 4-bit, a 3-bit, and a 2-bit parallel input (non-latched)/output (latched) ports, or 13 individual input (non-latched)/output (latched) output lines, depending on instruction. Parallel I/O: Each 4-bit port is named E-Port #6 (E27-E25), E-Port #7 (E31-E28), E-Port #8 (E35-R32), and E-Port #9 (E37-R36), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of E-Ports #6 to #9 by OUTX instruction. 4-bit data on the addressed port is input into the accumulator by INX instruction. (Before INX instruction, the port to be addressed must be set up "1" state (input) mode.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB88514B MB88515B	Pin No. MB88516B	Pin No. MB88517B	Type	Name & Function
E27-E25 E31-E28 E35-E32 E37-E36	31-29, 51-54, 47-50, 41,42	31-29, 51-54, 47-50, 41,42	20,19, 33-36 - -	I/O	Individual I/O: A state of the each line from E24 to E0 is input to the accumulator by ANDX, ORX, and INX instruction. A data of the accumulator is output to the each line by ANDX, ORX, and OUTX instruction. Refer to Table 4 User mask options for available making option.
NC	63	9,10,11, 12,21-24 55-57,63	-	-	Non Connection pin
• A/D Converter					
AV_{CC}	46	46	32	-	A/D converter supply voltage.
AV_{SS}	43	43	30	-	A/D converter ground pin.
A_{VR-}, A_{VR+}	44 45	44 45	31 -	-	A/D converter reference voltage.
AN3-AN0 AN7-AN4	51-54 47-50	51-54 47-50	31-28 -	I	8-bit Resolution A/D converter input: Analog input pin selectable from among the A3 to A0 by OUT (Y=D) instruction. Analog data which inputed from selected pin is A/D converted by OUT (Y=9) instruction, and input to internal memory as 5-bit digital data. Low of the digital data, one bit into the accumulator by IN (Y=E) instruction, and high of the digital data the four bit into the accumulator by IN (Y=F) instruction. This analog input is common to E-ports. In standby mode, this function doesn't worked, and A/D converted data is not hold.

DIFFERENCES BETWEEN MB88500 SERIES AND MB88510B SERIES

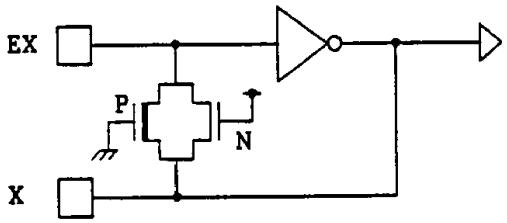
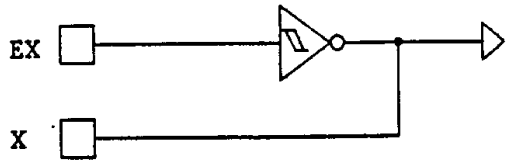
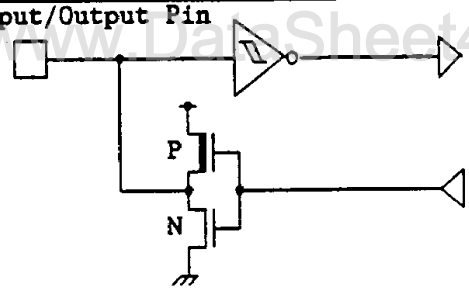
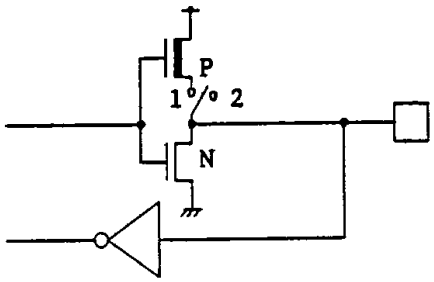
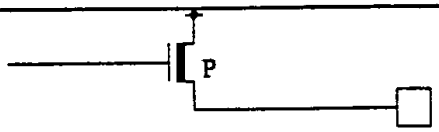
Table 2: DIFFERENCES BETWEEN MB88501 AND MB88510B SERIES

Item \ Device	MB88501	MB88510B series
ROM Size	· 4K x 8 bits	· Max. 8K x 8 bits
RAM Size	· 192 x 4 bits	· 256 x 4 bits
Min. Instruction Execution Time	· 2.86 µs use 4.19 MHz with prescaler	· 2.0 µs use 3.0 MHz with prescaler
I/O Port	36	Max. 54
VFD Driver Port	No	Max. 24
PLA	· No · Yes (Mask option)	· No
Serial Buffer	· 4 bit	· 4-/8-bit software selectable
A/D Converter	No	· 8 bit resolution, max. 8 channel.
Low-voltage Reset Function	· No · Yes (-10°C to +70°C) (Mask option:Standard version)	· No
Instruction No.	75	Max. 81
Package	· 42-pin standard DIP · 42-pin shrink DIP · 48-pin flat package	· 64-pin shrink DIP · 42-pin standard DIP
Members	· MB88501-P/-PSH/-PF A-version are available for each part above.	· MB88514B-P-SH · MB88515B-P-SH · MB88516B-P-SH · MB88517B-P

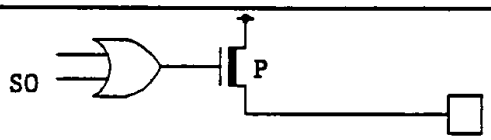
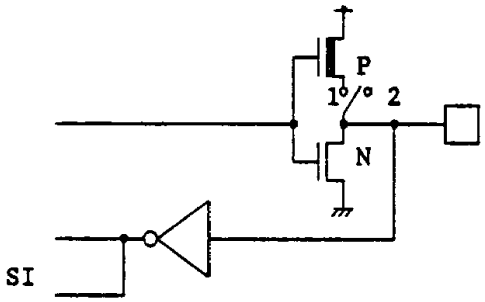
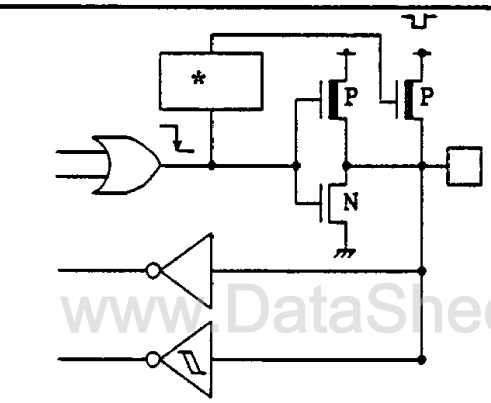
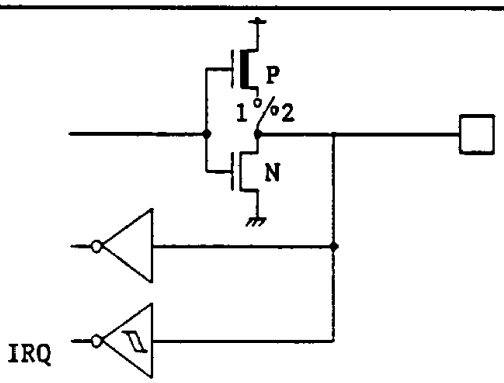
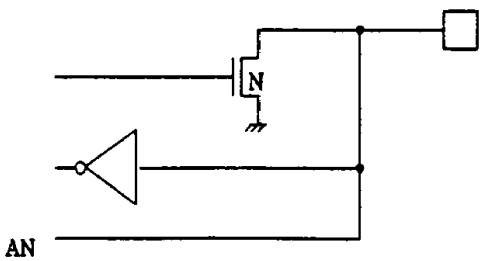
INPUT/OUTPUT CIRCUITS

All input only pins are internally pulled up, and all output only and input/output pins except E- and R-Ports have push-pull output buffer (standard pullup). E- and R-Ports can have push-pull (standard or high-current pullup) or open-drain (standard or high-current) buffer using mask option.

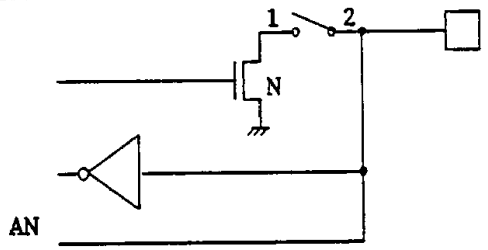
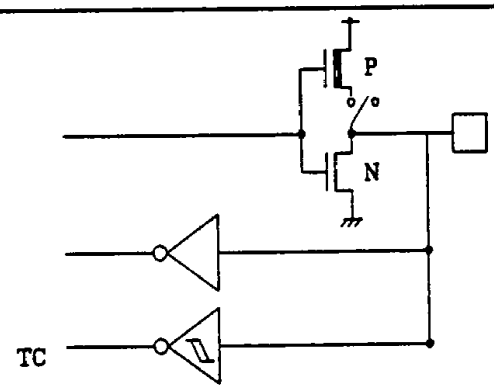
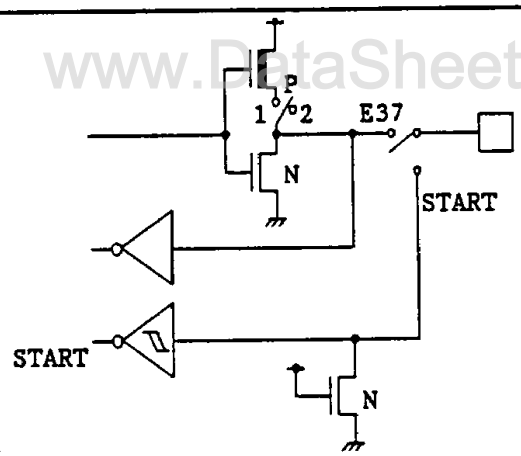
Table 3: INPUT/OUTPUT CIRCUITS

Pin	Circuit	Note
EX, X	• Crystal/Ceramic OSC or External Clock* 	• Non-hysteresis inverter • Feedback resistor: Approx. 2 MΩ typ. (at V_{CC}=5V) * When only external clock drive is used, we recommend RC-network OSC.
	• RC-Network OSC or External Clock* 	• Hysteresis inverter • Without feedback resistor * When only external clock drive is used, we recommend RC-network OSC.
$\overline{\text{RESET}}$	• Input/Output Pin 	• Output pullup resistor (P-ch. Tr.): Approx. 300kΩ typ. (at VCC=5V)
MB88514B/5B R0-R15 MB88516B: R0-R7, R11-R15 MB88517B: R0-R7, R12-R15		• Output port option 1: Standard/high current pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ 2: Standard/high-current open-drain without P-ch. pull-up resistor
MB88514B/5B E0-E23 MB88516B: E0-E7, E12-E19 MB 88517B E0-E7, E12-E16		• P-ch. high-voltage open-drain output

Input/Outoput (Continued)

Pin	Circuit	Remarks
MB88514B/ 5B/6B: E24/SO MB88517B: E17/SO		• P-ch. high-voltage open-drain output
MB88514B/ 5B/6B: E25/SI MB88517B: R15/SI		• Output port option 1: Standard/high current pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ 2: Standard/high-current open-drain without P-ch. pull-up resistor
E26($\overline{SC}$/$\overline{TO}$)		• With pull-up resistor P-ch. Tr. approx. 10kΩ * This additional circuit makes the load MOS FET turn on, at the timing when high level is output on the $\overline{TO}$ line, so that the $\overline{TO}$ line can goes high immediately.
E27/$\overline{IRQ}$		• Output port option 1: Standard/high current pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ 2: Standard/high-current open-drain without P-ch. pull-up resistor
MB88514B/ 5B/7B: E28/AN0- E31/AN3 MB88516B: E28/AN0- E35/AN0		• Open-drain output

Input/Output Circuit (Continued)

Pin	Circuit	Remarks
MB88514B/5B E32/AN4-E32-AN7		• Analog input circuit option: 1: Standard analog input 2: High impeadance analog input
MB88514B/5B/6B: E36/$\overline{TC}$ MB88517B: R11/$\overline{TC}$		• Output port option 1: Standard pull-up: pull-up resistor: P-ch. Tr, approx.10kΩ 2: Standard open-drain, high current open-drain without P-ch. pull-up resistor
MB88514B/5B/6B: E37/START MB88517B: E18/START		E37(E18): • Output port option 1: Standard/high current pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ 2: Standard/high-current open-drain without P-ch. pull-up resistor START: With N-ch. pull-down register approx. 300kΩ

USER MASK OPTIONS

The MB88510B series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock	CLK	No	0	f_C=0.5 MHz to 3 MHz:
		Yes	1	f_C=1 MHz to 6 MHz:
Oscillator Type	OSC	Crystal/ceramic OSC or external clock*	0	* When only external clock drive is used, we recommend RC-network oscillator.
		RC-network OSC or external clock*	1	We recommend no clock prescaler.
Output Port Type	PORT	Standard open-drain	L	
		Standard pull-up	M	
		High-current open-drain	K	
		High-current pull-up	T	
Standby Function	STBY	No	0	MB88514B/5B/6B: Pin 41 is applied to E37. MB88517B Pin 15 is applied to E18.
		Yes (Software initiation)	1	MB88514B/5B/6B: Pin 41 is applied to START. MB88517B Pin 15 is applied to START.
Output Port State During Standby	STATE	Hold	0	Output port state option selected must be the same for all E- and R-Ports.
		High-Z	1	
Standby off Reset Function	SOR	No	0	
		Yes	1	
Watch-dog Timer Function	WDR	No	0	
		Yes	1	
Analog Input (AN4-AN7)Port Type (MB88514B/5B)	ANIN	High impedance analog input	0	E28/AN0 to E31/AN3 is standard analog input.
		Standard analog input	1	

NOTES ON OPERATION

- **Prevention Latch-up**

  Latch-up may occur in CMOS devices when a voltage higher than V_{CC} or lower than V_{SS} is applied to any input or output pin, or when a voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins. If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

- **Treatment of Unused Pins**

  Unused input pins should be pulled up or down with external resistors or they may cause some malfunction. (However, the X pin should be open when an external clock oscillator is used.)

- **A/D converter supply**

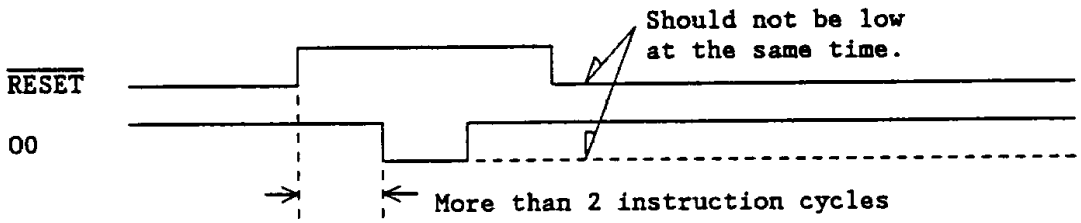
  When A/D converter function doesn't used, AVCC and AVSS should be connect the supply and ground.

- **Special Function of R12 Pin**

  The R12 pin has another function as a test terminal, in addition to its normal function R-Port. If the R12 pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the R12 pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

  Especially when the open-drain is selected for the output port option, the R12 pin should be externally pulled up because such open-drain outputs are subject to noise disturbance if left floating.

  At least 2 instruction cycles are required to change R12 pin from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



- **External Capacitors for Crystal Oscillation**

  Figs. 11, 19, and 27 gives an aim of an area where the on-chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

  The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use crystal with a frequency higher than required oscillation frequency, together with the on-chip divided-by-two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

NOTES ON OPERATION

- **Supply Voltage**

Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:

(1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.

(2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88510B series instruction set includes 81 (79) instructions, 78% of which are single-byte and single-cycle, 19% two-byte two-cycle, 1% two byte three-cycle, and 2% three-byte and three-cycle. The MB88510B series instruction sets is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

* MB88514B/5B: 81 instruction
MB88516B/7B: 79 instruction

Tables 5 and 6 summarize the MB88510B series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	TATH	05	·	·	·	1/1	TH←(AC)
	TATL	06	·	·	·	1/1	TL←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	↕	·	·	1/1	4-bit mode: AC←(SB_L), 8-bit mode: AC←(SB_L), X←(SB_H)
	TTHA	15	↕	·	·	1/1	AC←(TH)
	TTLA	16	↕	·	·	1/1	AC←(TL)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)⇌(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)⇌{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)⇌{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ⇌{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LXID	3D90-3D9F*	↕	·	·	2/2	X←imm; imm=0 to 15
	LRXA imm	3D20-3D3F*	·	·	·	2/3	X ←{ROM(imm | X | Y)}d, d=7-4 AC←{ROM(imm | X | Y)}d, d=3-0 imm=0 to 31
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	3D80-3D8F	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	·	·	↓Z	1/1	imm-(Y) ; imm=0 to 15

Table 5: INSTRUCTION SET SUMMARY (Continued)

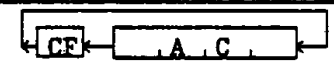
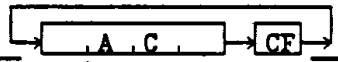
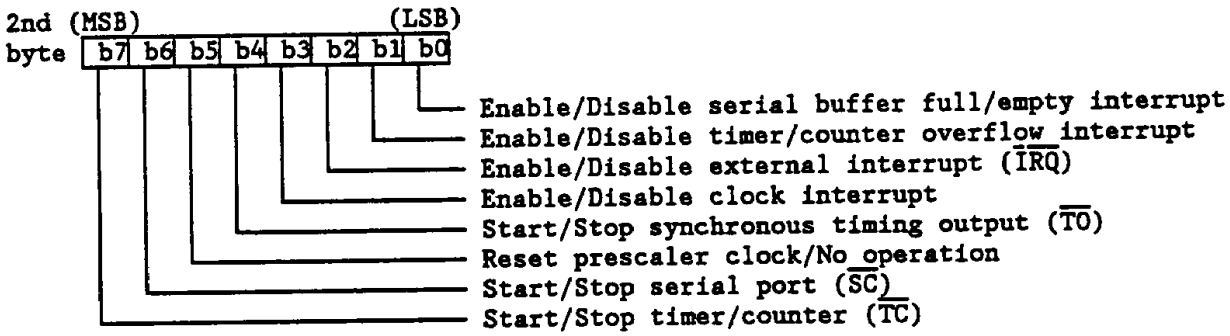
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)
	ICA	3D81	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICX	3DAC	·	·	↓C	2/2	X←(X)+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipula- tion	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	RBA bp	3DA4 3DA7 *	·	·	·	2/2	(AC)bp←0 ; bp=0 to 3
	SBA bp	3DA0 3DA3 *	·	·	·	2/2	(AC)bp←1 ; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
	RST	3DAD	·	·	·	2/2	System initialization
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #) AC←(REG)Y; Y=9 to 15
	INK	12	↕	·	·	1/1	AC←(R15-R12)
	INX	3DAA	·	·	·	2/2	AC←E(Y) ; Y=6 to 9
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R);Y=9 to 15
	OUTP	02	·	·	·	1/1	E3-E0←(AC)
	OUTX	3DAB	·	·	·	2/2	E(Y)←(AC); Y=0 to 9
	ANDX	3DA8	·	·	·	2/2	E←(AC)∩(E)Y ; Y=0 to 9
	ORX	3DA9	·	·	·	2/2	E←(AC)∪(E)Y ; Y=0 to 9
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of Port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of Port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-6FFF*	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 4095. ST=0, Not Subroutine Call.
	CALX addr *4	3D4000-3D5FFF*	·	·	·	3/3	If ST=1, Subroutine Call for addr; addr=0 to 8192. ST=0, Not Subroutine Call.

Table 5: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Branch	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPXY addr	3D00-3D1F*	·	·	·	2/2	Branch always to addr on page #n;
	JPL addr	7000-7FFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 4095. ST=0, No Branch.
	JPLX addr *4	3DC000-3DCFFF*	·	·	·	3/3	If ST=1, Branch to addr; addr=0 to 8192. ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return From Interrupt Routine
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulation	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



*4: MB88514B/5B only

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
-	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
‾ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviation	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
E	E-Port (#0: E3-E0, #1: E7-E4, ... #2: E35-E32, #9: E37-E36)
(R)Y; Y=n	E-Port #n specified by Y-register (Y=0 to 9)
IF	Interrupt flag
imm	Immediate data
IRQ	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODES SUMMARY

L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	NOT USED	OUTP	OUT	TAY	TATH	TATL	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	* EXT	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

NOTE: : 1-byte/1-cycle instruction : 2-bytes/2-cycles instruction

* See the next page

Table 6: INSTRUCTION CODES SUMMARY (Continued)
Extended instruction

3DL / 3DH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1																
2	LRXA imm															
3																
4	CALX *															
5																
6	NOT USED															
7																
8		(ICA)	AI imm													(DCA)
9	LXID imm															
A	SBA bp				RBA bp				ANDX	ORX	INX	OUTX	ICX	RST	NOT USED	
B	NOT USED															
C	JPLX *															
D																
E																
F																

* MB88514B/5B only

Note: : 3 byte/3 cycle instruction

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

The MB88510B series consists of the MB88514B, MB88515B, MB88516B, and MB88517B. The MB88518B are available as piggyback EPROM evaluation devices for MB88514B/5B/6B. MB88PG517B is for the MB88517B. Refer to Table 7.

Table 7: MB88510B SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88514B-PSH MB88515B-PSH	MB88516B-PSH	MB88517B-PSH	MB88518B-C-SH-101/102	MB88PG518B-C-101/102
ROM Size	6Kx8 bits:4B 8Kx8 bits:5B (On-chip mask ROM)	8K x 8 bits (On-chip mask ROM)	4K x 8 bits (On-chip mask ROM)	8K x 8 bits (External EPROM)	
RAM Size (Directly addressed locations)	256 x 4 bits (0-7)				
I/O Port:	54	43	34	54	34
-Input only port	0	0	0	0	0
-Output only port	25	17	15	25	15
-I/O port	29	26	19	29	19
-Control port	5 (Including serial I/O)				
VFD Port	24	17	15	24	15
-Segment	18	10	8	18	8
-Digit	6	7	7	6	7
Output Port Type	· STD P/U · STD O/D · H/C P/U · H/C O/D (Mask option)			· H/C P/U (101) · H/C O/D (102)	· STD O/D (101) · STD P/U (102)
A/D Converter -Resolution -Channel -Analog input level	8-bits 8-channels Standard/High		8-bits 4 cahnnels	8-bits 8-cahnnels Standard	8-bits 4-channels
Stack Depth (Nesting level)	8 levels				
Timer/Counter: -Buffer size -Clock source	Yes 8 bits Internal/External				
Serial I/O: -Buffer size -Clock source -Output latch	Yes 4/8 bits Internal/External Yes				
Clock Generator: -Oscillator type -Clock Frequency (With prescaler)	Yes · Crystal/External · RC-Network/External (Mask option) 0.5 MHz-3 MHz (1 MHz-6 MHz)			Yes · Crystal/External (Fixed) - 1 MHz-6 MHz	
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)			Yes (Fixed)	
Interrupt Function -Nesting level -Interrupt sources	Yes Single level 4 sources				

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

Table 7: MB88500H SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS (Countinued)

	MB88514B-PSH MB88515B-PSH	MB88516B-PSH	MB88517B-PSH	MB88518B-C-SH-101/102	MB88PG518B-C-101/102
Standby Function: -Initiation method -Oscillator state during standby -Output state during standby -Standby off reset function	· Yes/No (Mask option) · Software · Idle/Stop (Software selectable) · Hold/High-Z (Mask option) · Yes/No (Mask option)			· Yes · Software · Idle/Stop (Software selectable) · Hold :102 · High-Z:101 · No	No - - - -
Watch Dog Timer Function	Yes/No (Mask option)			· No (Fixed)	
Number of Instructions	81	79		81	
Instruction Length/Cycle	1/1, 2/2, 2/3 or 3/3	1/1, 2/2, or 2/3		1/1, 2/2, 2/3, or 3/3	
Min. Instruction Execution Time	1.5 µs at 8 MHz (With prescaler)				
Power Supply: -Active -Standby	+5V · 4.5V to 5.5V · 3.5V to 6.0V				-
Operating Temp. Range:	-40°C to +85°C				
Process	CMOS				
Package	SH-DIP-64P		DIP-42P	SH-MDIP-64P	MDIP-42P
Development Tools: -Hardware -Software 	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-34 : DUE board (MB88514B/5B/6B) MB2115-96 : Port adapter (MB88514B/5B/6B) MB2115-92 : SDIP 64-pin cable (MB88517B) MB2115-38 : DUE board (MB88517B) SM05215-A010: Intellec series III MDS cross-assembler SM07415-A012: CP/M-86 cross-assembler SMXXXXX-XXXX: PC-DOS cross-assembler SM07415-G022: CP/M-86 host emulator SMXXXXX-XXXX: PC-DOS host emulator				

Note STD: Standard
H/C: High-current
P/U: Pull-up
O/D: Open-drain

MB88514B/5B ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS** (MB88514B/5B)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	Sholud not exceed VCC
	AV_{R-}	V_{SS}-0.3		V_{SS}+7.0	V	
	AV_{R+}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed AV_{CC}+0.3V
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
		V_{CC}-40		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V E0 to E24
Output Low Current	I_{OL}			15	mA	
Total Output Low Current	ΣI_{OL}			80	mA	
Output High Current	I_{OH1}			-25	mA	E0 to E5, E24
	I_{OH2}			-15	mA	E6 to E23
Total Output High Current	ΣI_{OH}			-80	mA	E0 to E24
Power Dissipation	P_D			650	mW	
Operating Ambient Temperature	T_A	-40		+85	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS** (MB88514B/5B)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	4.5		5.5	V	Should not exceed VCC
	AV_{R+}	AV_{R-}		AV_{CC}	V	
	AV_{R-}	0		AV_{R+}	V	
Input High Voltage	V_{IH}	$0.7 \cdot V_{CC}$		$V_{CC}+0.3$	V	R-,E-ports,SI,EX(Crystal/ceramic resonator)
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$	V	START, (RC-network) $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$, $\overline{RESET}$
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.3 \cdot V_{CC}$	V	R-,E-ports,SI,EX(Crystal/ceramic resonator)
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	START, EX(RC-network) $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$, $\overline{RESET}$
Operating Ambient Temperature	T_A	−40		+85	°C	

2

- **DC CHARACTERISTICS** (MB88514B/5B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value Min.	Value Typ.	Value Max.	Unit
Output High Voltage	V_{OH}	E-, R-Ports (High-current/ standard pull-up)	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	E-, R-Ports (All outputs options), $\overline{RESET}$	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		E-,R-Ports(High-current open-drain/pull-up)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input Leakage Current	I_{IL}	E-, R-Ports (High-current/ standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		$\overline{EX}$, $\overline{RESET}$	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
	IIH	EX, START	V_{CC}=5.5V V_{IH}=5.5V			60	μA
Output Current	I_{OH1}	E0 to E5, E24	V_{CC}=4.5V to 5.5V V_{OH}=V_{CC}-2.5V	-15			mA
	I_{OH2}	E6 to E23		-5			mA
Open-Drain Output Leakage Current	I_{LOL1}	E0 to E5, E24	V_{CC}=5.5V V_{OL}=V_{CC}-35V (P-ch. Tr. off)			-20	μA
	I_{LOL2}	E6 to E23				-10	μA
	I_{LEAK}	E-,R-Ports(High-current/standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V (N-ch. Tr off)		0.1	10	μA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	E-, R-Ports	V_{CC}=6.0V(Standby) V_{IN}=0V to 6.0V			±25	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=1MHz(Operation) All outputs open		3	6	mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=5.0V(Typ.) V_{CC}=6.0V(Max.) fc=0(Standby) All outputs open		3	15	μA
Input Capacitance	C_{IN}	All pins except V_{CC}, V_{SS}	fc=1MHz		10	20	pF

- **AC CHARACTERISTICS** (MB88514B/5B)

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/ Port	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic, RC-network OSC or external clock drive Figs. 8 and 9	1	3	MHz	Without prescaler
				2	6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 8 and 9	0.33	1	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open) Figs. 8 and 9	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figs. 8 and 9	5	200	ns	

Fig. 8: CLOCK TIMING

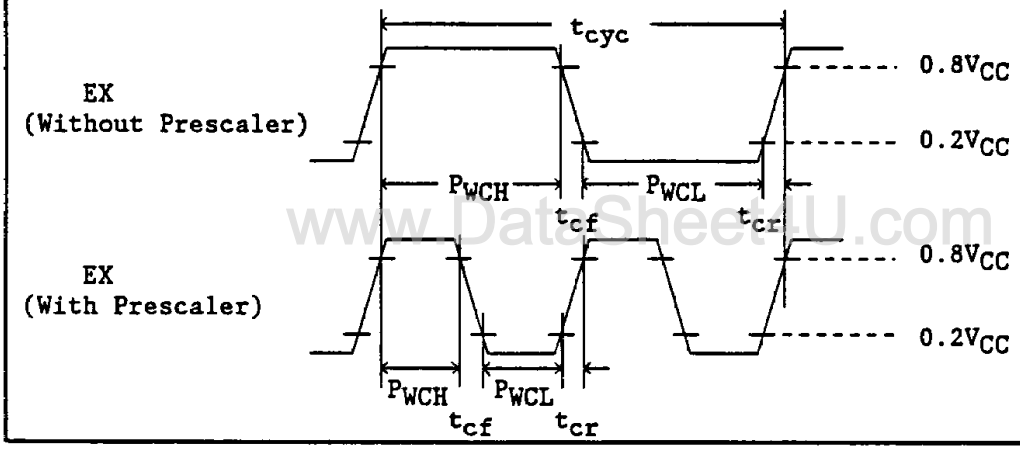
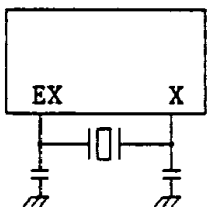
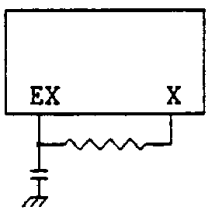


Fig. 9: CLOCK CIRCUIT CONFIGURATIONS

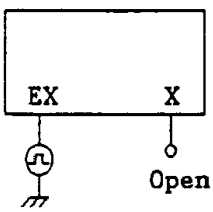
(1) Crystal/Ceramic Oscillation



(2) RC-Network * Oscillation

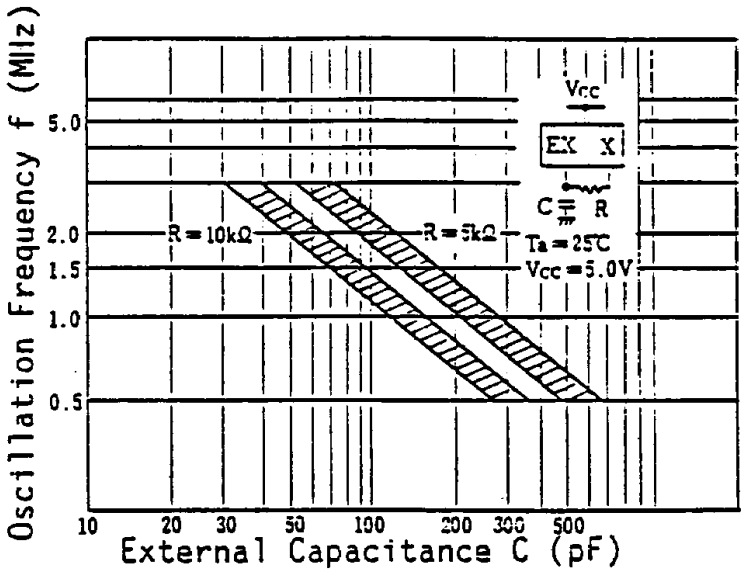


(3) External Clock Drive



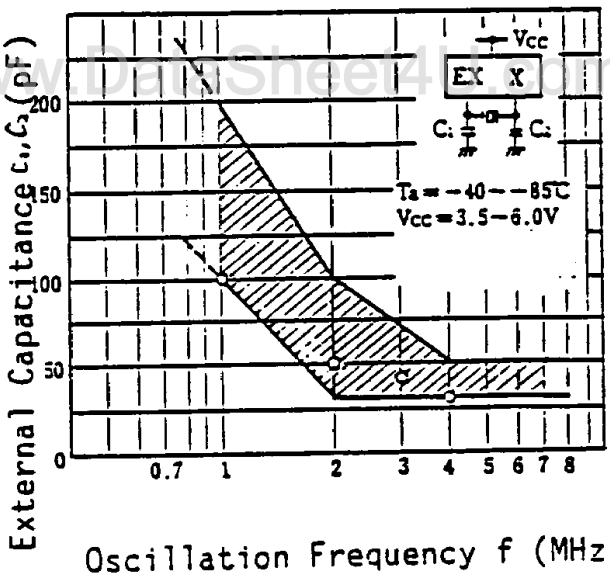
* When the RC-network oscillation is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-40°C to +85°C
4) f_C does not exceed 3MHz (Max. setting clock frequency is about 2.4MHz at V_{CC}=5V and T_A=25°C.)

Fig. 10: RC-Network Oscillation Characteristics (Example)



Note:
When the RC-network oscillations is used, the following conditions must be met: 1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-40°C to 85°C 4) f_C does not exceed 2.4 MHz.

Fig. 11: Crystal Oscillation Characteristics (Example)



Note:
1) The cross-hatched portion shows an area where the on-chip oscillator has stable oscillation characteristics and short oscillation stabilization time when an average crystal resonator is used. This chart gives an aim value of the external capacitor to realize a desired oscillation frequency. When an exact oscillation frequency is needed, a capacitor value should be determined, adjusting to individual crystal resonator characteristics.
2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend to use high-frequency crystal resonator with on-chip 1/2 prescaler.

- **OUTPUT TIMING** (MB88514B/5B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
E-, R-ports Delay Time	t_{PDH}	E25-E37, R0-R15	With pull-up resistor approx. at 10kΩ Fig. 12		1000	ns
	t_{PDL}				350	
E-Port(High-Voltage Open-Drain) Delay Time	t_{EDH}	E0-E24	With pull-down resistor approx. at 10kΩ Fig. 12		350	ns
	t_{EDL}				1000	
Serial Port Delay Time	t_{SDH}	SO	Fig. 12		1000	ns
	T_{SDL}				350	

Note:
1. Except E-port output loading values are 50pF + 1TTL. See figure below.
2. E-Port output load values are 50pF.

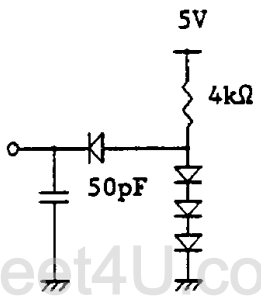
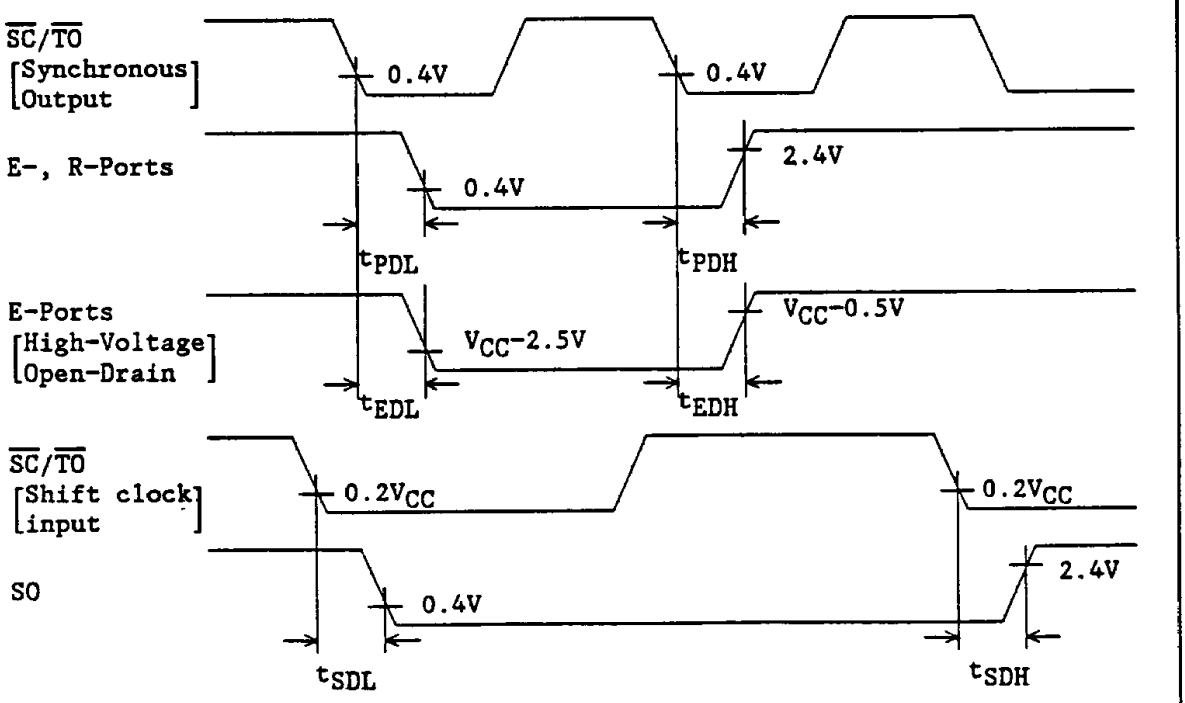


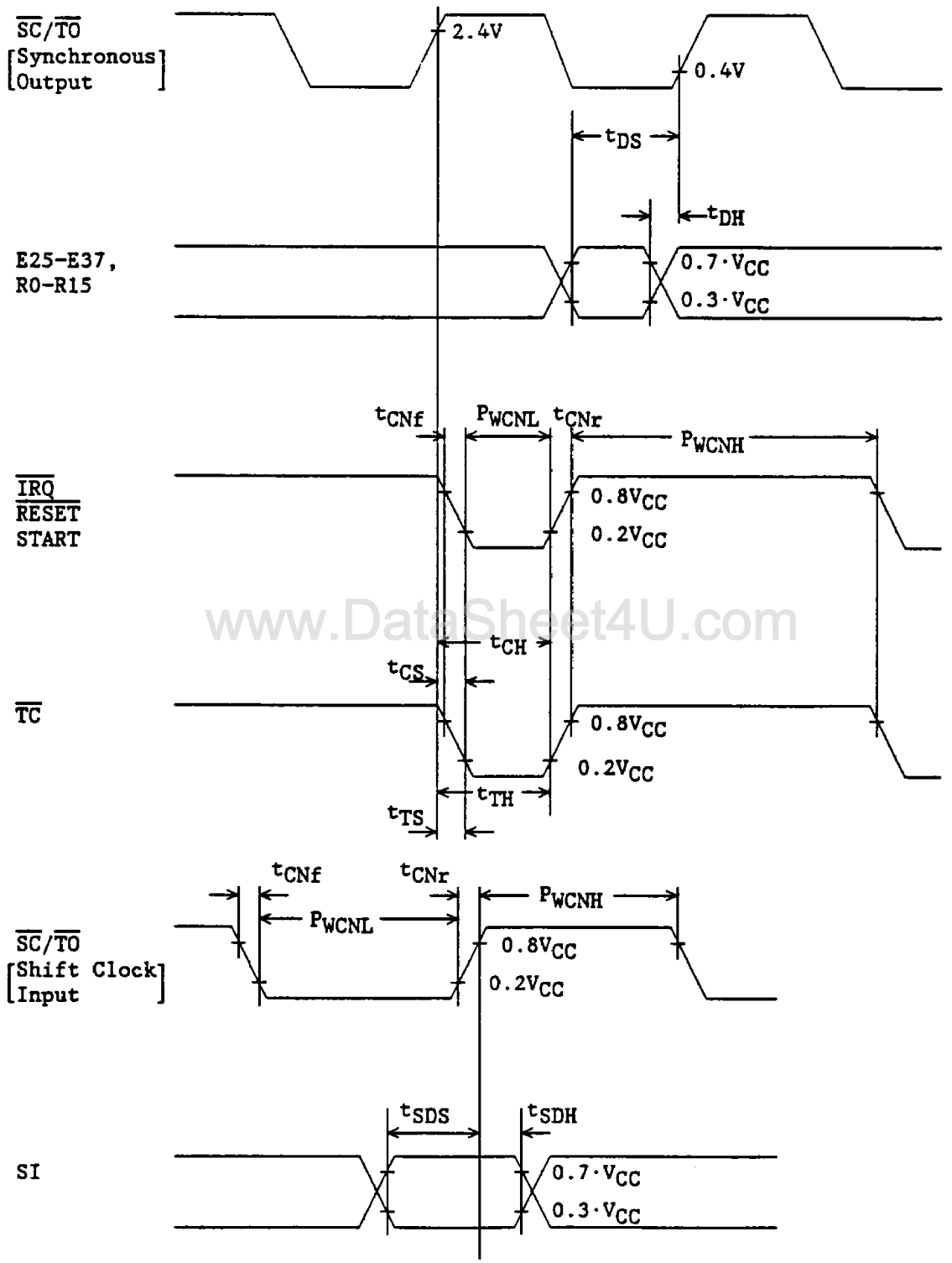
Fig. 12: OUTPUT CLOCK TIMING



INPUT TIMING (MB88514B/5B)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	E25-E37 R-Port	Fig. 13	$t_{cyc}+1000$		ns
Input Data Hold Time	t_{DH}				$t_{cyc}-50$	
SI Input Setup Time	t_{SDS}	SI	Fig. 13	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 13		$2t_{cyc}-200$	ns
		$\overline{IRQ}$			$2t_{cyc}-200$	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 13	$8t_{cyc}+50$		ns
		$\overline{IRQ}$		$2t_{cyc}+50$		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 13		$2t_{cyc}-200$	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 13	$2t_{cyc}+50$		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 13	$6t_{cyc}+250$		ns
		$\overline{IRQ}$, $\overline{TC}$		$6t_{cyc}+250$		
		$\overline{RESET}$		$12t_{cyc}+250$		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 13	$12t_{cyc}+250$		ns
		$\overline{RESET}$, $\overline{TC}$, $\overline{IRQ}$		$6t_{cyc}+250$		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{SC}/\overline{TO}$, $\overline{IRQ}$ $\overline{RESET}$, $\overline{TC}$	Fig. 13	Should be less than 200ns		

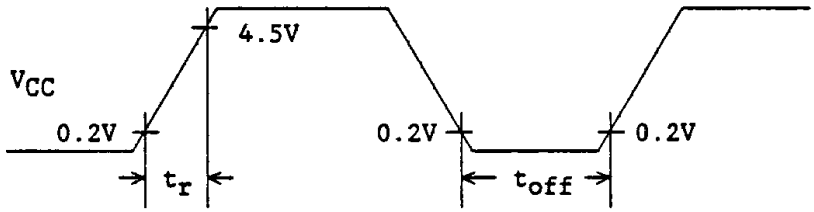
Fig. 13: INPUT TIMING



• **POWER-ON RESET(MB88514B/5B)**

Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 14	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 14	1		ms	Required for accurate circuit operation repeatability

Fig. 14: POWER-ON RESET TIMING



Note:
Power supply should be raised smoothly.

- **A/D CONVERTER CHARACTERISTICS** (MB88514B/5B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value			Unit	Conditions
			Min.	Typ.	Max.		
Resolution					8	Bit	
Linearity Error					±1.0	LSB	AV_{R+}=5.0V AV_{R-}=0V
Differential Linearity Error					±0.9	LSB	
Zero Transition Voltage	V_{OT}		-20	+10	+40	mV	
Full-Scale Transition Voltage	V_{FST}		+4910	+4970	+5030	mV	
Conversion Time			47.5 *1		144*2	µs	144 x t_{CYC}
Analog Port Input Current	I_{AIN}	AN0-7			5	µA	Standard analog input
		AN4-7			1	µA	High impedance analog inputs
Analog Input Voltage		AN0-7	AV_{R-}		AV_{R+}	V	
Reference Voltage		AV_{R+}	AV_{R-}		AV_{CC}	V	$\frac{AV_{R+}+AV_{R-}}{2} \leq 0.6AV_{CC}$
		AV_{R-}	0	0	AV_{R+}	V	
Supply Current	I_A	AV_{CC}		1.5		mA	AV_{CC}=5.0V
	IA_H	AV_{CC}			5	µA	AV_{CC}=6.0V(Standby)
Reference Voltage Supply Current	I_R	AV_{R+}		170		µA	AV_{R-}=0V AV_{R+}=5.0V

Notes:
1. Error between analog inputs is within 1/2 LSB when AV_{R+}-AV_{R-}=5.0V
2. Full-scale and offset can be adjust by an appropriate setting of AV_{R+} and AV_{R-}.
3. Error becomes relatively larger as $|AV_{R+}-AV_{R-}|$ becomes smaller.

*1 fc=6.0 MHz (with prescaler)
*2 fc=1.0 MHz (without prescaler)

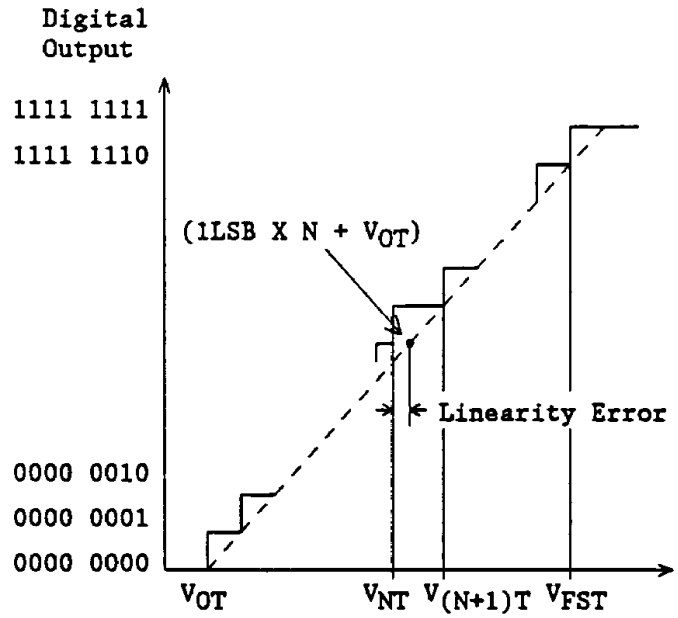
- Resolution
  The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^8=256 parts.)

- Linearity Error
  The difference between the line connecting the device zero transition point ("0000 0000" ⟷ "0000 0001") with the full scale transition point ("1111 1111" ⟷ "1111 1110"), the actual conversion characteristics.

- Differential Linearity Error
  The difference from ideal input voltage required to change the output voltage code by 1LSB.

• **A/D CONVERTER CHARACTERISTICS** (Continues)

Fig. 15: A/D TRANSFER CHARACTERISTICS



$$1LSB = \frac{V_{FST} - V_{OT}}{254}$$

$$\text{Linearity Error} = \frac{V_{NT} - (1LSB \times N + V_{OT})}{1LSB} \quad (LSB)$$

$$\text{Differential Linearity Error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \quad (LSB)$$

MB88516B ELECTRICAL CHARACTERISTICS

• **ABSOLUTE MAXIMUM RATINGS** (MB88516B)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed VCC
	AV_{R-}	V_{SS}-0.3		V_{SS}+7.0	V	
	AV_{R+}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed AV_{CC}+0.3V
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
		V_{CC}-40		V_{SS}+7.0	V	should not exceed V_{CC}+0.3V, E0-E7, E12-E19,E24
Output Low Current	I_{OL}			15	mA	
Total Output Low Current	ΣI_{OL}			75	mA	
Output High Current	I_{OH1}			-30	mA	E0-E5, E24
	I_{OH2}			-15	mA	E6, E7, E12-E19
Total Output High Current	ΣI_{OH}			-100	mA	E0-E7, E12-E19, E24
Power Dissipation	P_D			650	mW	
Operating Ambient Temperature	T_A	-40		+85	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS** (MB88516B)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Guaranteed range
		3.5		6.0	V	Standby range
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	4.5		5.5	V	Should not exceed VCC
	AV_{R+}	AV_{R-}		AV_{CC}	V	
	AV_{R-}	0		AV_{R+}	V	
Input High Voltage	V_{IH}	$0.7 \cdot V_{CC}$		$V_{CC}+0.3$	V	R-,E-ports,SI,EX(Crysral/ ceramic resonator)
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$	V	$\overline{EX}$(RC-network), $\overline{START}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}$/$\overline{TO}$, $\overline{RESET}$
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.3 \cdot V_{CC}$	V	R-,E-ports,SI,EX(Crysral/ ceramic resonator)
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	$\overline{EX}$(RC-network), $\overline{START}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}$/$\overline{TO}$, $\overline{RESET}$
Operating Ambient Temperature	T_A	-40		+85	°C	

- **DC CHARACTERISTICS** (MB88516B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value Min.	Value Typ.	Value Max.	Unit
Output High Voltage	V_{OH}	E-, R-Ports (High-current/ standard pull-up)	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	E-, R-Ports (All outputs options), $\overline{RESET}$	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		E-,R-Ports(High-current open-drain/pull-up)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input Leakage Current	I_{IL}	E-, R-Ports (High-current/ standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		$\overline{EX}$, $\overline{RESET}$	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
	IIH	EX, START	V_{CC}=5.5V V_{IH}=5.5V			60	μA
Output Current	I_{OH1}	E0-E5, E24	V_{CC}=4.5V to 5.5V V_{OH}=V_{CC}-2.5V	-15			mA
	I_{OH2}	E6, E7, E12-E19		-5			mA
Open-Drain Output Leakage Current	I_{LOL1}	E0-E5, E24	V_{CC}=5.5V V_{OL}=V_{CC}-35V (P-ch. Tr. off)			-20	μA
	I_{LOL2}	E6, E7, E12-E19				-10	μA
	I_{LEAK}	E-,R-Ports(High-current/standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V (N-ch. Tr off)		0.1	10	μA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	E-, R-Ports	V_{CC}=6.0V(Standby) V_{IN}=0V to 6.0V			±25	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=1MHz(Operation) All outputs open		3	6	mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=5.0V(Typ.) V_{CC}=6.0V(Max.) fc=0(Standby) All outputs open		3	15	μA
Input Capacitance	C_{IN}	All pins except V_{CC}, V_{SS}	fc=1MHz		10	20	pF

- **AC CHARACTERISTICS** (MB88516B)

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/ Port	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic, RC-network OSC or external clock drive Figs. 16 and 17	1	3	MHz	Without prescaler
				2	6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 16 and 17	0.33	1	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open) Figs. 16 and 17	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figs. 16 and 17	5	200	ns	

Fig. 16: CLOCK TIMING

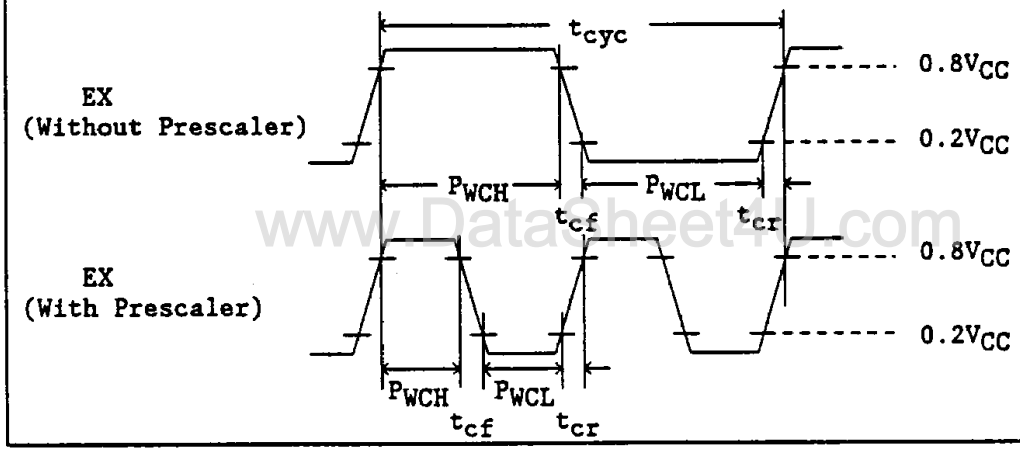
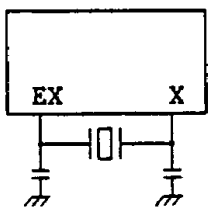
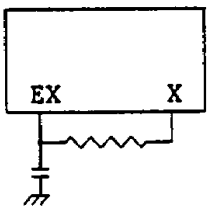


Fig. 17: CLOCK CIRCUIT CONFIGURATIONS

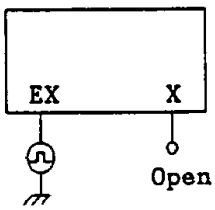
(1) Crystal/Ceramic Oscillation



(2) RC-Network * Oscillation

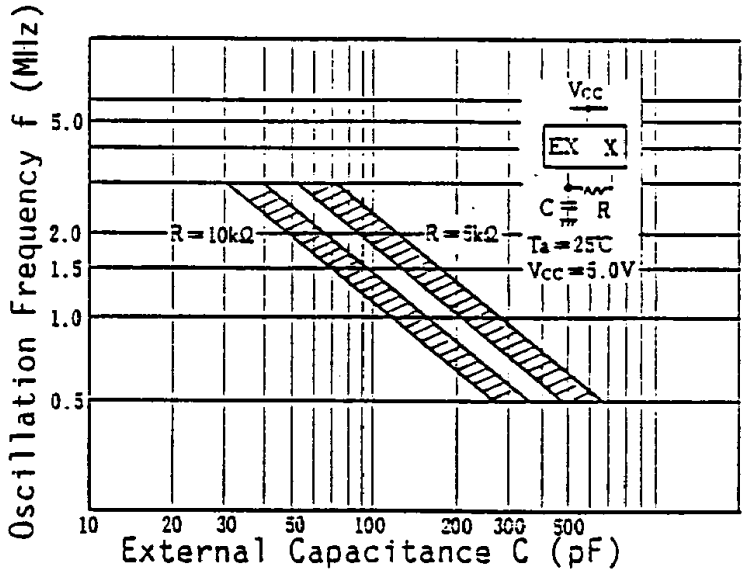


(3) External Clock Drive



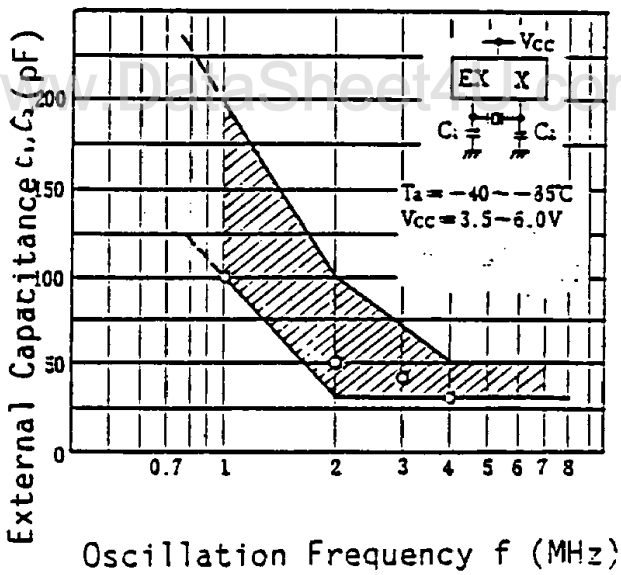
* When the RC-network oscillation is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-40°C to +85°C
4) f_C does not exceed 3MHz (Max. setting clock frequency is about 2.4MHz at V_{CC}=5V and T_A=25°C.)

Fig. 18: RC-Network Oscillation Characteristics (Example)



Note:
When the RC-network oscillations is used, the following conditions must be met: 1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-40°C to 85°C 4) f_C does not exceed 2.4 MHz.

Fig. 19: Crystal Oscillation Characteristics (Example)



Note:
1) The cross-hatched portion shows an area where the on-chip oscillator has stable oscillation characteristics and short oscillation stabilization time when an average crystal resonator is used. This chart gives an aim value of the external capacitor to realize a desired oscillation frequency. When an exact oscillation frequency is needed, a capacitor value should be determined, adjusting to individual crystal resonator characteristics.
2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend to use high-frequency crystal resonator with on-chip 1/2 prescaler.

- **OUTPUT TIMING** (MB88516B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
E-, R-ports Delay Time	t_{PDH}	E25-E37, R0-R7, R11-R15	With pull-up resistor approx. at 10kΩ Fig. 20		1000	ns
	t_{PDL}				350	
E-Port(High-Voltage Open-Drain) Delay Time	t_{EDH}	E0-E7, E12-E19, E24	With pull-down resistor approx. at 10kΩ Fig. 20		350	ns
	t_{EDL}				1000	
Serial Port Delay Time	t_{SDH}	SO	Fig. 20		1000	ns
	T_{SDL}				350	

Note:
1. Except E-port output loading values are 50pF + 1TTL. See figure below.
2. E-Port output load values are 50pF.

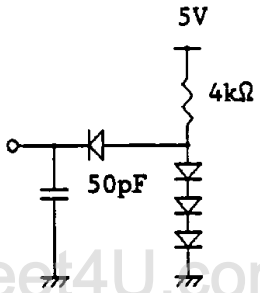
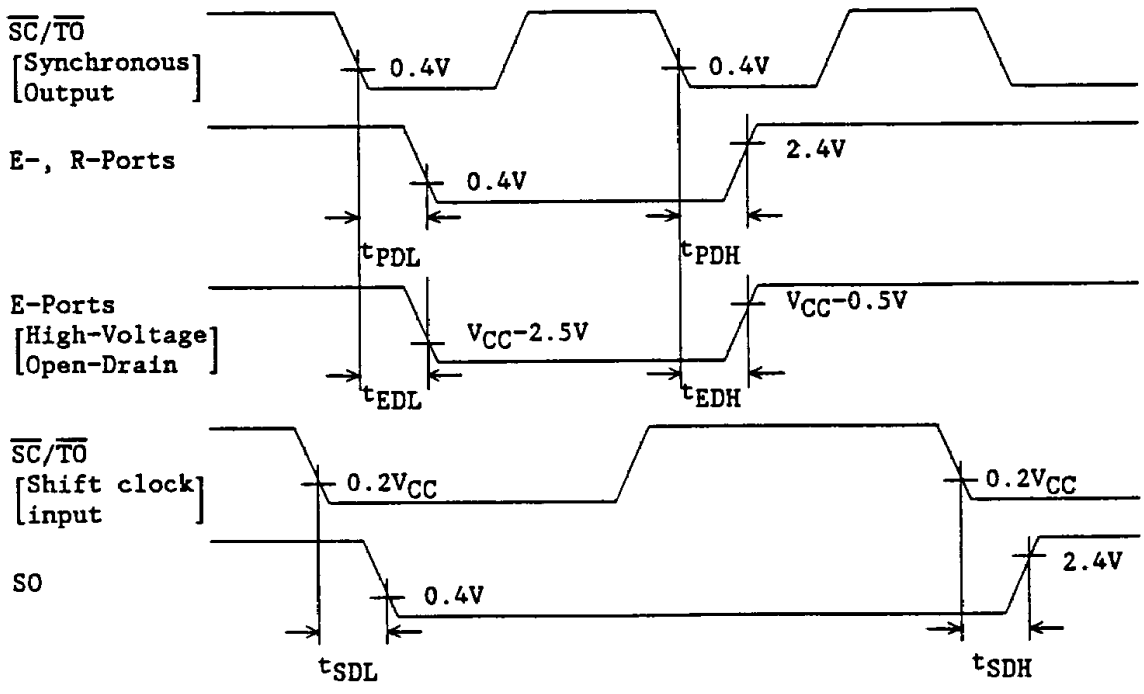


Fig. 20: OUTPUT CLOCK TIMING

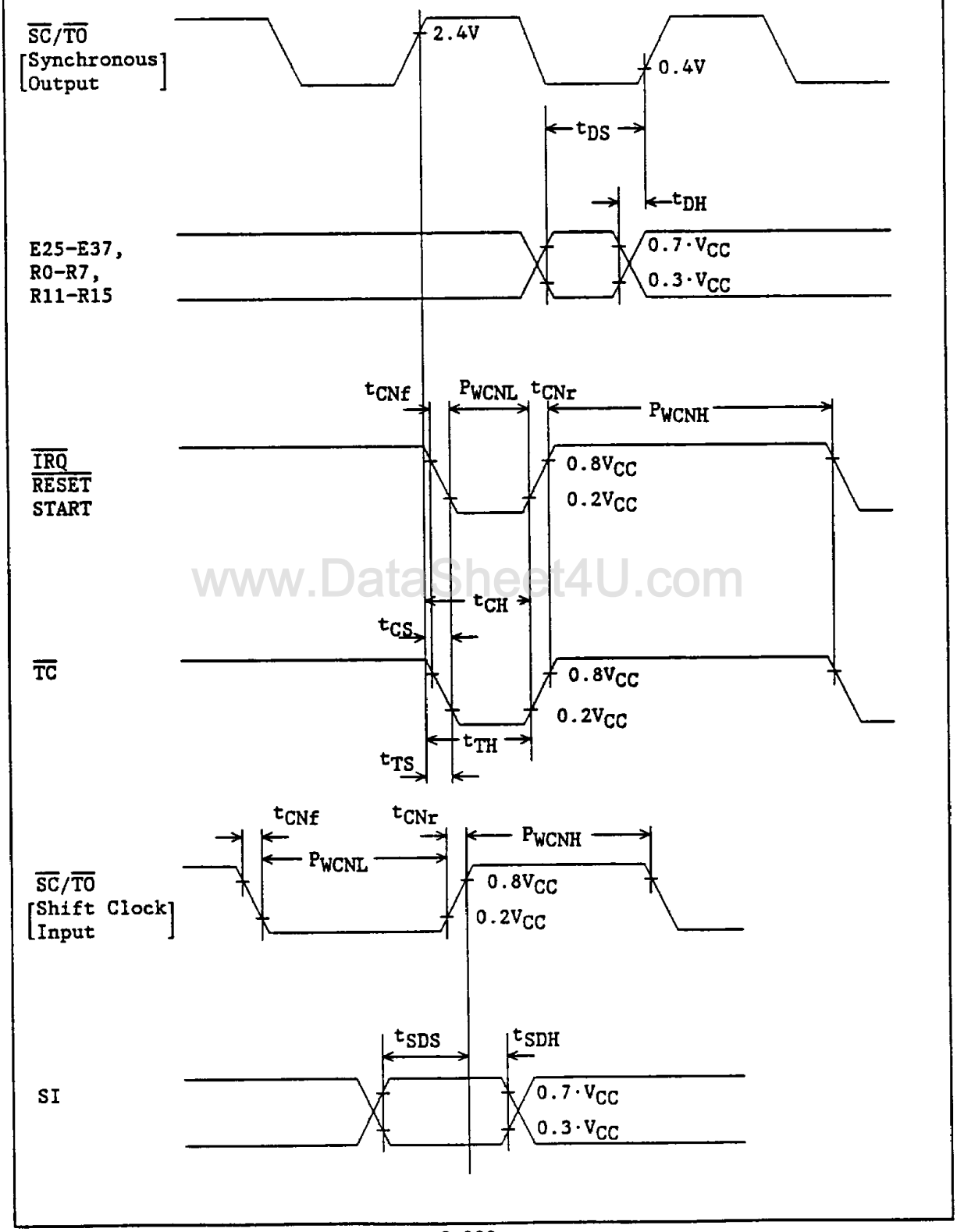


INPUT TIMING (MB88516B)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	E25-E37, R0-R7, R11-R15	Fig. 21	t_{cyc}+1000		ns
Input Data Hold Time	t_{DH}				t_{cyc}-50	
SI Input Setup Time	t_{SDS}	SI	Fig. 21	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 21		$2t_{cyc}$-200	ns
		$\overline{IRQ}$			$2t_{cyc}$-200	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 21	$8t_{cyc}$+50		ns
		$\overline{IRQ}$		$2t_{cyc}$+50		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 21		$2t_{cyc}$-200	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 21	$2t_{cyc}$+50		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 21	$6t_{cyc}$+250		ns
		$\overline{IRQ}$, $\overline{TC}$		$6t_{cyc}$+250		
		$\overline{RESET}$		$12t_{cyc}$+250		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 21	$12t_{cyc}$+250		ns
		$\overline{RESET}$, $\overline{TC}$, $\overline{IRQ}$		$6t_{cyc}$+250		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{SC}/\overline{TO}$, $\overline{IRQ}$ $\overline{RESET}$, $\overline{TC}$	Fig. 21	Should be less than 200ns		

2

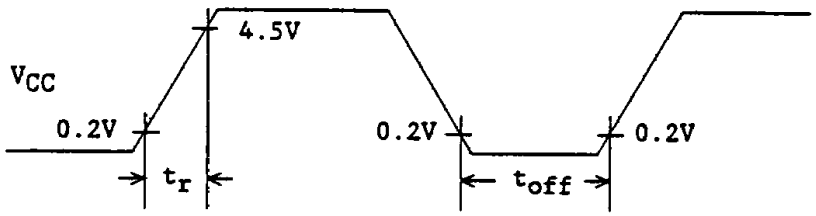
Fig. 21: INPUT TIMING



• POWER-ON RESET(MB88516B)

Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 22	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 22	1		ms	Required for accurate circuit operation repeatability

Fig. 22: POWER-ON RESET TIMING



Note:
Power supply should be raised smoothly.

2

- **A/D CONVERTER CHARACTERISTICS** (MB88516B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value			Unit	Conditions
			Min.	Typ.	Max.		
Resolution					8	Bit	
Linearity Error					±1.0	LSB	AV_{R+}=5.0V, AV_{R-}=0V
Differential Linearity Error					±0.9	LSB	
Zero Transition Voltage	V_{OT}		-20	+10	+40	mV	
Full-Scale Transition Voltage	V_{FST}		+4910	+4970	+5030	mV	
Conversion Time			47.5 *1		144*2	µs	144 x t_{CYC}
Analog Port Input Current	I_{AIN}	AN0-7			1	µA	
Analog Input Voltage		AN0-7	AV_{R-}		AV_{R+}	V	
Reference Voltage		AV_{R+}	AV_{R-}		AV_{CC}	V	$\frac{AV_{R+}+AV_{R-}}{2} \leq 0.6AV_{CC}$
		AV_{R-}	0	0	AV_{R+}	V	
Supply Current	I_A	AV_{CC}		1.5		mA	AV_{CC}=5.0V, A/D converter mode
	I_{AH}	AV_{CC}			5	µA	AV_{CC}=6.0V, Stadnby or A/D stop mode
Reference Voltage Supply Current	I_R	AV_{R+}		170		µA	AV_{R-}=0V, AV_{R+}=5.0V

Notes:
1. Error between analog inputs is within 1/2 LSB when $AV_{R+}-AV_{R-}$=5.0V
2. Full-scale and offset can be adjust by an appropriate setting of AV_{R+} and AV_{R-}.
3. Error becomes relatively larger as $|AV_{R+}-AV_{R-}|$ becomes smaller.

*1 fc=6.0 MHz (with prescaler)
*2 fc=1.0 MHz (without prescaler)

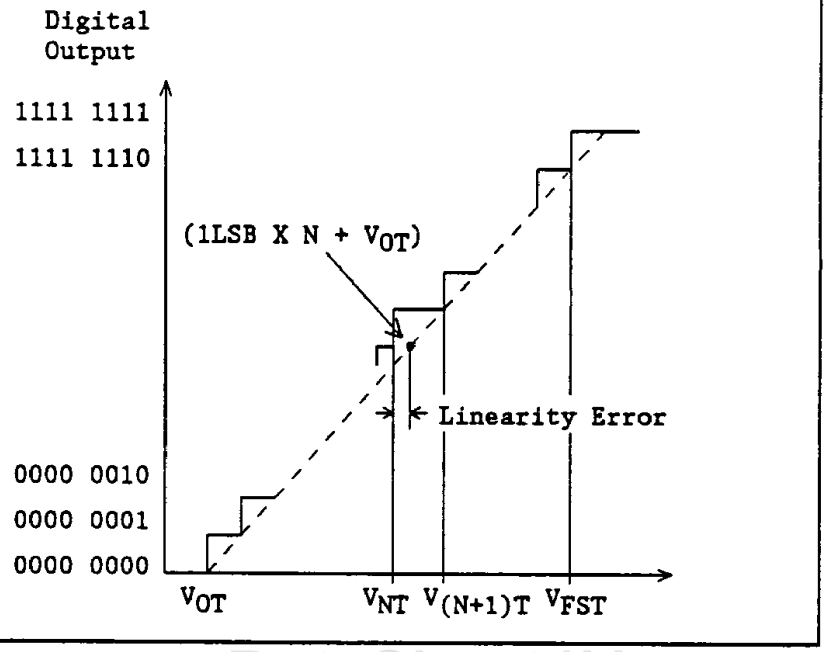
- Resolution
  The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^8=256 parts.)

- Linearity Error
  The difference between the line connecting the device zero transition point ("0000 0000" ⟷ "0000 0001") with the full scale transition point ("1111 1111" ⟷ "1111 1110"), the actual conversion characteristics.

- Differential Linearity Error
  The difference from ideal input voltage required to change the output voltage code by 1LSB.

• A/D CONVERTER CHARACTERISTICS (Continues)

Fig. 23: A/D TRANSFER CHARACTERISTICS



$$1LSB = \frac{V_{FST} - V_{OT}}{254}$$

$$\text{Linearity Error} = \frac{V_{NT} - (1LSB \times N + V_{OT})}{1LSB} \quad (LSB)$$

$$\text{Differential Linearity Error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \quad (LSB)$$

MB88517B ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS** (MB88517B)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed VCC
	AV_{R-}	V_{SS}-0.3		V_{SS}+7.0	V	
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
		V_{CC}-40		V_{SS}+7.0	V	should not exceed V_{CC}+0.3V, E0-E7, E12-E18 *1
Output Low Current	I_{OL}			15	mA	
Total Output Low Current	ΣI_{OL}			75	mA	
Output High Current	I_{OH1}			-25	mA	E0-E5
	I_{OH2}			-15	mA	E6, E7, E12-E18*1
Total Output High Current	ΣI_{OH}			-80	mA	E0-E7, E12-E18*1
Power Dissipation	P_D			650	mW	
Operating Ambient Temperature	T_A	-40		+85	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

*1: Only E18 selected high-voltage port by mask option.

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS** (MB88517B)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Guaranteed range
		3.5		6.0	V	Standby range
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	4.5		5.5	V	Should not exceed VCC
	AV_{R-}	0		$0.2AV_{CC}$	V	
Input High Voltage	V_{IH}	$0.7 \cdot V_{CC}$		$V_{CC}+0.3$	V	R-,E-ports,SI,EX(Crysral/ ceramic resonator)
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$	V	$\overline{EX}$(RC-network), $\overline{START}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}$/TO, $\overline{RESET}$
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.3 \cdot V_{CC}$	V	R-,E-ports,SI,EX(Crysral/ ceramic resonator)
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	$\overline{EX}$(RC-network), $\overline{START}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}$/TO, $\overline{RESET}$
Operating Ambient Temperature	T_A	-40		+85	°C	

2

- **DC CHARACTERISTICS** (MB88517B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value Min.	Value Typ.	Value Max.	Unit
Output High Voltage	V_{OH}	E-, R-Ports (High-current/ standard pull-up)	V_{CC}=4.5V I_{OH}=-200µA	2.4			V
			V_{CC}=4.5V I_{OH}=-10µA	4.0			V
Output Low Voltage	V_{OL}	E-, R-Ports (All outputs options), $\overline{RESET}$	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		E-,R-Ports(High-current open-drain/pull-up)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input Leakage Current	I_{IL}	E-, R-Ports (High-current/ standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		$\overline{EX}$, $\overline{RESET}$	V_{CC}=5.5V V_{IL}=0.4V			-60	µA
	IIH	EX, START	V_{CC}=5.5V V_{IH}=5.5V			60	µA
Output Current	I_{OH1}	E0-E5	V_{CC}=4.5V to 5.5V V_{OH}=V_{CC}-2.5V	-15			mA
	I_{OH2}	E6, E7, E12-E18 *1		-5			mA
Open-Drain Output Leakage Current	I_{LOL1}	E0-E5	V_{CC}=5.5V V_{OL}=V_{CC}-35V (P-ch. Tr. off)			-20	µA
	I_{LOL2}	E6, E7, E12-E18 *1				-10	µA
	I_{LEAK}	E-,R-Ports(High-current/standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V (N-ch. Tr off)		0.1	10	µA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	E-, R-Ports	V_{CC}=6.0V(Standby) V_{IN}=0V to 6.0V			±25	µA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=1MHz(Operation) All outputs open		3	6	mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=5.0V(Typ.) V_{CC}=6.0V(Max.) fc=0(Standby) All outputs open		3	15	µA
Input Capacitance	C_{IN}	All pins except V_{CC}, V_{SS}	fc=1MHz		10	20	pF

*1: Only E18 is selected high-voltage port by mask option.

- **AC CHARACTERISTICS** (MB88517B)

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/ Port	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic, RC-network OSC or external clock drive Figs. 24 and 25	1	3	MHz	Without prescaler
				2	6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 24 and 25	0.33	1	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open) Figs. 24 and 25	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figs. 24 and 25	5	200	ns	

Fig. 24: CLOCK TIMING

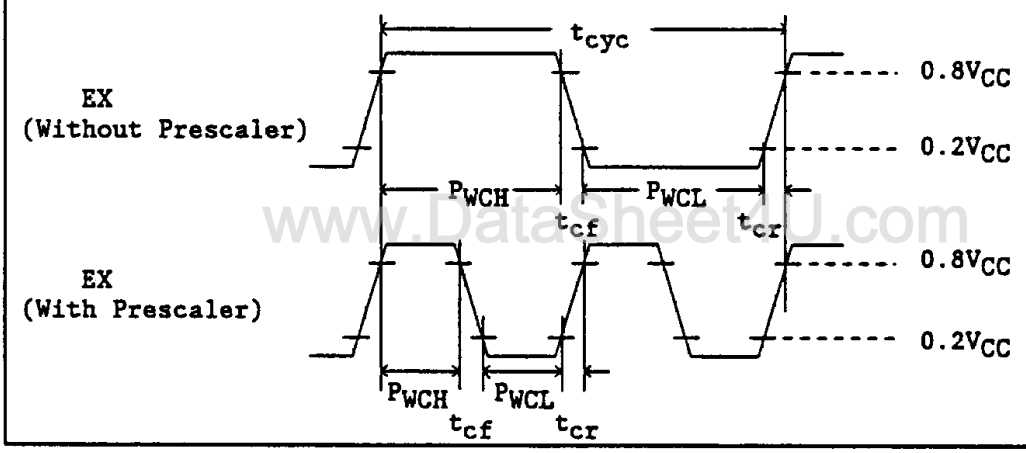
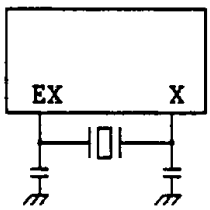
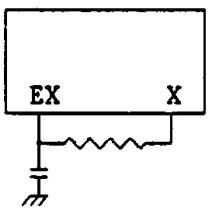


Fig. 25: CLOCK CIRCUIT CONFIGURATIONS

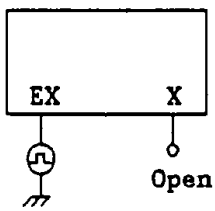
(1) Crystal/Ceramic Oscillation



(2) RC-Network * Oscillation

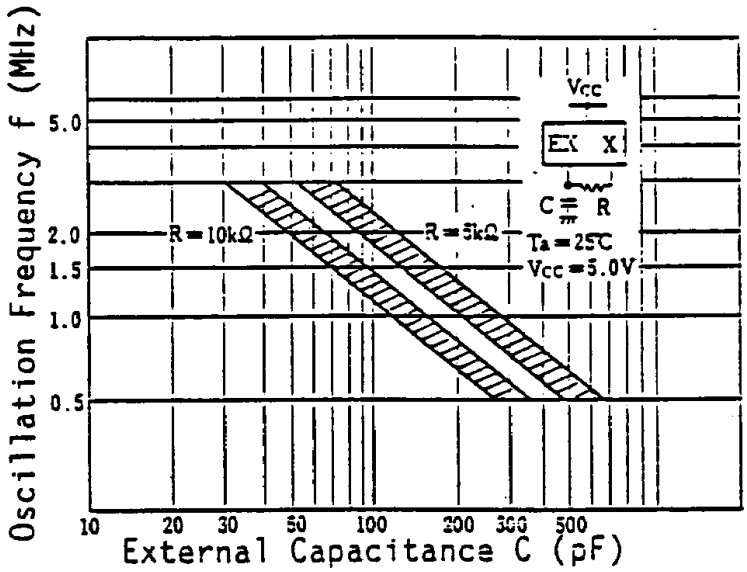


(3) External Clock Drive



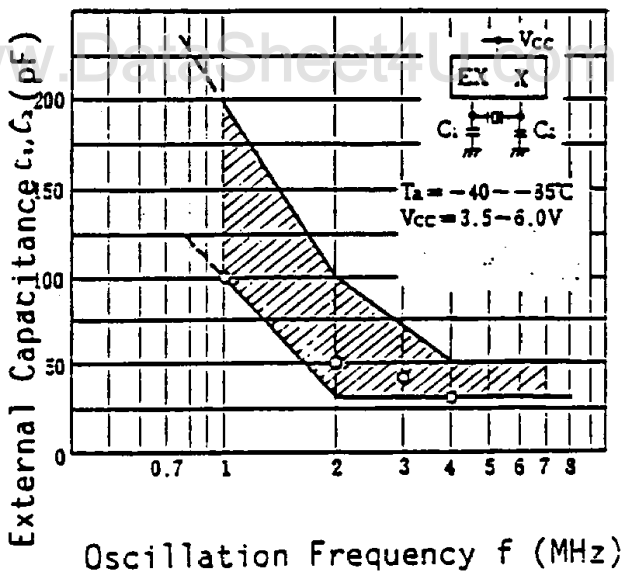
* When the RC network oscillation is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-40°C to +85°C
4) f_C does not exceed 3MHz (Max. setting clock frequency is about 2.4MHz at V_{CC}=5V and T_A=25°C.)

Fig. 26: RC-Network Oscillation Characteristics (Example)



Note:
When the RC-network oscillations is used, the following conditions must be met: 1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-40°C to 85°C 4) f_C does not exceed 2.4 MHz.

Fig. 27: Crystal Oscillation Characteristics (Example)



Note:
1) The cross-hatched portion shows an area where the on-chip oscillator has stable oscillation characteristics and short oscillation stabilization time when an average crystal resonator is used. This chart gives an aim value of the external capacitor to realize a desired oscillation frequency. When an exact oscillation frequency is needed, a capacitor value should be determined, adjusting to individual crystal resonator characteristics.
2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend to use high-frequency crystal resonator with on-chip 1/2 prescaler.

- **OUTPUT TIMING** (MB88517B)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
E-, R-ports Delay Time	t_{PDH}	E18*1, E26-E31, R0-R7, R11-R15	With pull-up resistor approx. at 10kΩ Fig. 28		1000	ns
	t_{PDL}				350	
E-Port(High-Voltage Open-Drain) Delay Time	t_{EDH}	E0-E7, E12-E18*1	With pull-down resistor approx. at 10kΩ Fig. 28		350	ns
	t_{EDL}				1000	
Serial Port Delay Time	t_{SDH}	SO	Fig. 28		1000	ns
	T_{SDL}				350	

Note:
*1. Only E18 is selected high-voltage port by mask option.
*2. Except E-port output loading values are 50pF + 1TTL. See figure below.
*3. E-Port output load values are 50pF.

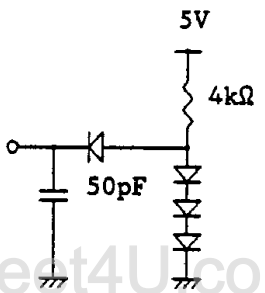
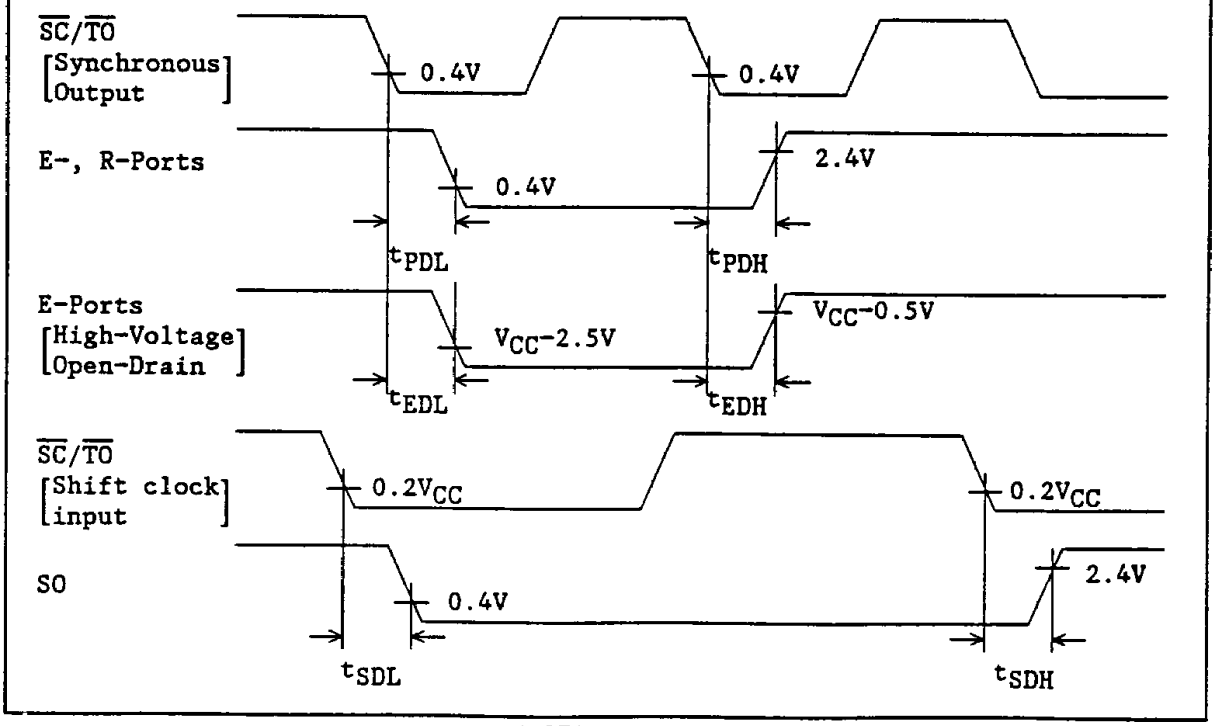


Fig. 28: OUTPUT CLOCK TIMING

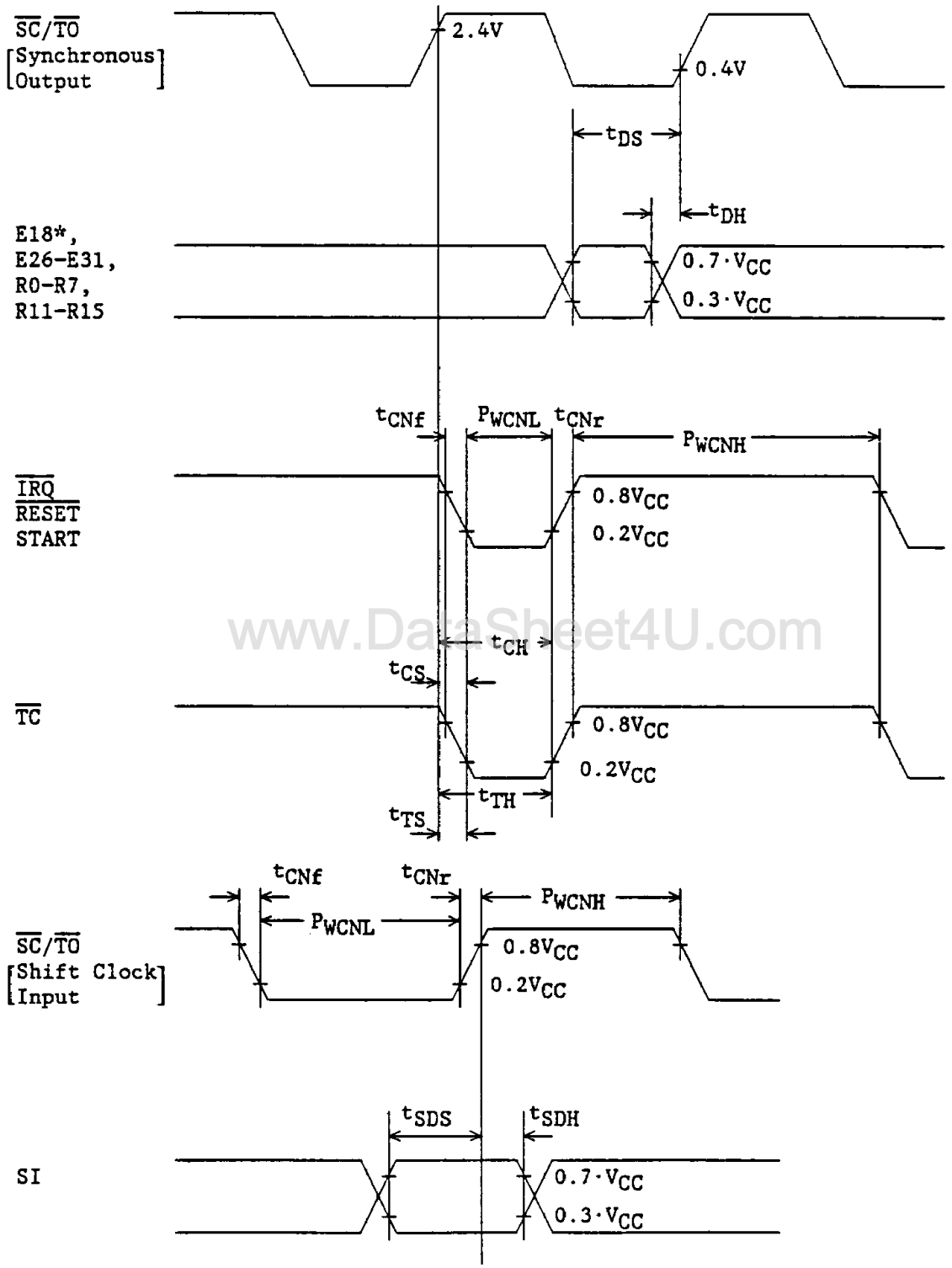


INPUT TIMING (MB88517B)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	E18*, E26-E31, R0-R7, R11-R15	Fig. 29	t_{cyc}+1000		ns
Input Data Hold Time	t_{DH}				t_{cyc}-50	
SI Input Setup Time	t_{SDS}	SI	Fig. 29	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 29		$2t_{cyc}$-200	ns
		$\overline{IRQ}$			$2t_{cyc}$-200	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 29	$8t_{cyc}$+50		ns
		$\overline{IRQ}$		$2t_{cyc}$+50		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 29		$2t_{cyc}$-200	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 29	$2t_{cyc}$+50		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 29	$6t_{cyc}$+250		ns
		$\overline{IRQ}$, $\overline{TC}$		$6t_{cyc}$+250		
		$\overline{RESET}$		$12t_{cyc}$+250		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 29	$12t_{cyc}$+250		ns
		$\overline{RESET}$, $\overline{TC}$, $\overline{IRQ}$		$6t_{cyc}$+250		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{SC}/\overline{TO}$, $\overline{IRQ}$ $\overline{RESET}$, $\overline{TC}$	Fig. 29	Should be less than 200ns		

*1 Only E18 is selected high-voltage port by mask option.

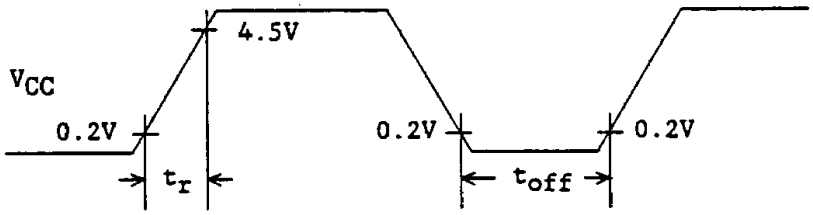
Fig. 29: INPUT TIMING



• **POWER-ON RESET(MB88517B)**

Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 29	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 29	1		ms	Required for accurate circuit operation repeatability

Fig. 29: POWER-ON RESET TIMING



Note:
Power supply should be raised smoothly.

• **A/D CONVERTER CHARACTERISTICS** (MB88517B)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Value			Unit	Conditions
			Min.	Typ.	Max.		
Resolution					8	Bit	
Linearity Error					±1.0	LSB	AV_{CC}=5.0V AV_{R-}=0V
Differential Linearity Error					±0.9	LSB	
Zero Transition Voltage	V_{OT}		-20	+10	+40	mV	
Full-Scale Transition Voltage	V_{FST}		+4910	+4970	+5030	mV	
Conversion Time			47.5 *1		144*2	µs	144 x t_{CYC}
Analog Port Input Current	I_{AIN}	AN0-3			1	µA	
Analog Input Voltage		AN0-3	AV_{R-}		AV_{CC}	V	
Reference Voltage		AV_{R-}	0	0	0.2AV_{CC}	V	
Supply Current	I_A	AV_{CC}		1.7		mA	AV_{CC}=5.0V, AV_{R-}=0V A/D converter mode
	I_{AH}	AV_{CC}			5	µA	AV_{CC}=AV_{R-}=6V Standby or A/D stop mode
Reference Voltage Supply Current	I_R	AV_{R+}			300	µA	AV_{CC}=6V AV_{R-}=0V

Notes:
1. Error between analog inputs is within 1/2 LSB when AV_{CC}-AV_{R-}=5.0V
2. Full-scale and offset can be adjust by an appropriate setting of AV_{CC} and AV_{R-}.
3. Error becomes relatively larger as $|AV_{CC}-AV_{R-}|$ becomes smaller.

*1 fc=6.0 MHz (with prescaler)
*2 fc=1.0 MHz (without prescaler)

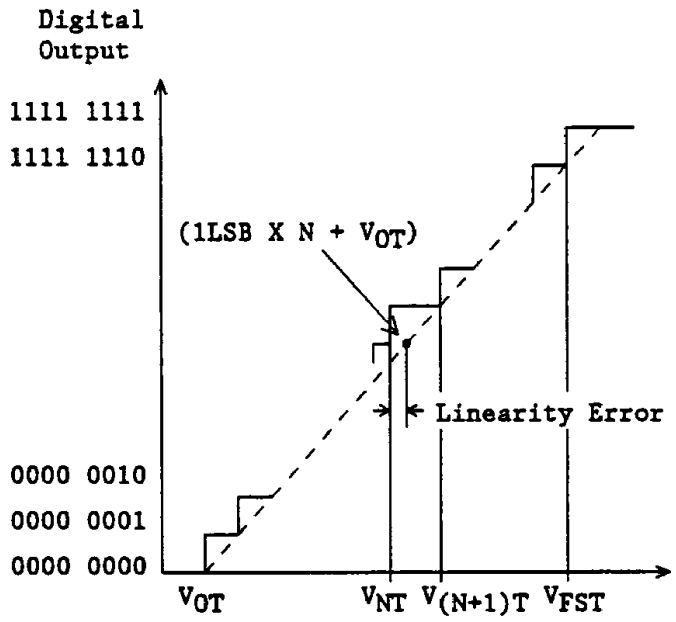
• Resolution
The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^8=256 parts.)

• Linearity Error
The difference between the line connecting the device zero transition point ("0000 0000" ⟷ "0000 0001") with the full scale transition point ("1111 1111" ⟷ "1111 1110"), the actual conversion characteristics.

• Differential Linearity Error
The difference from ideal input voltage required to change the output voltage code by 1LSB.

• **A/D CONVERTER CHARACTERISTICS** (Continues)

Fig. 31: A/D TRANSFER CHARACTERISTICS



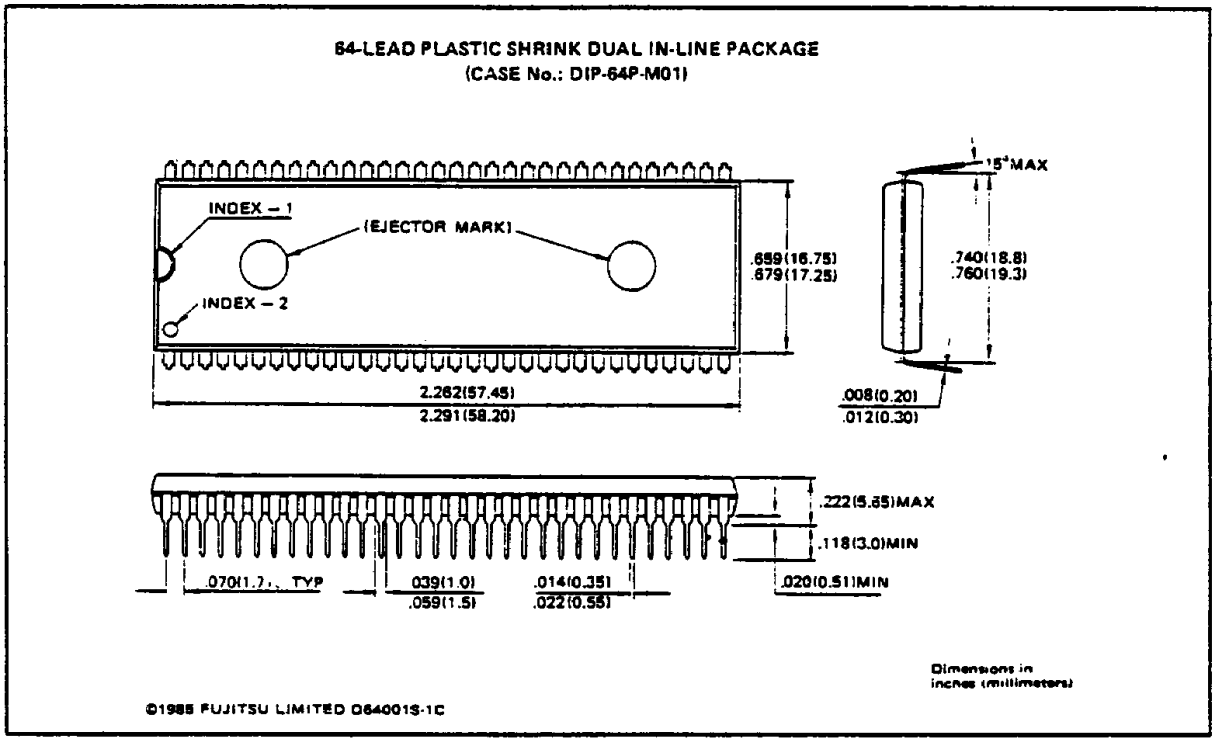
$$1LSB = \frac{V_{FST} - V_{OT}}{254}$$

$$\text{Linearity Error} = \frac{V_{NT} - (1LSB \times N + V_{OT})}{1LSB} \quad (LSB)$$

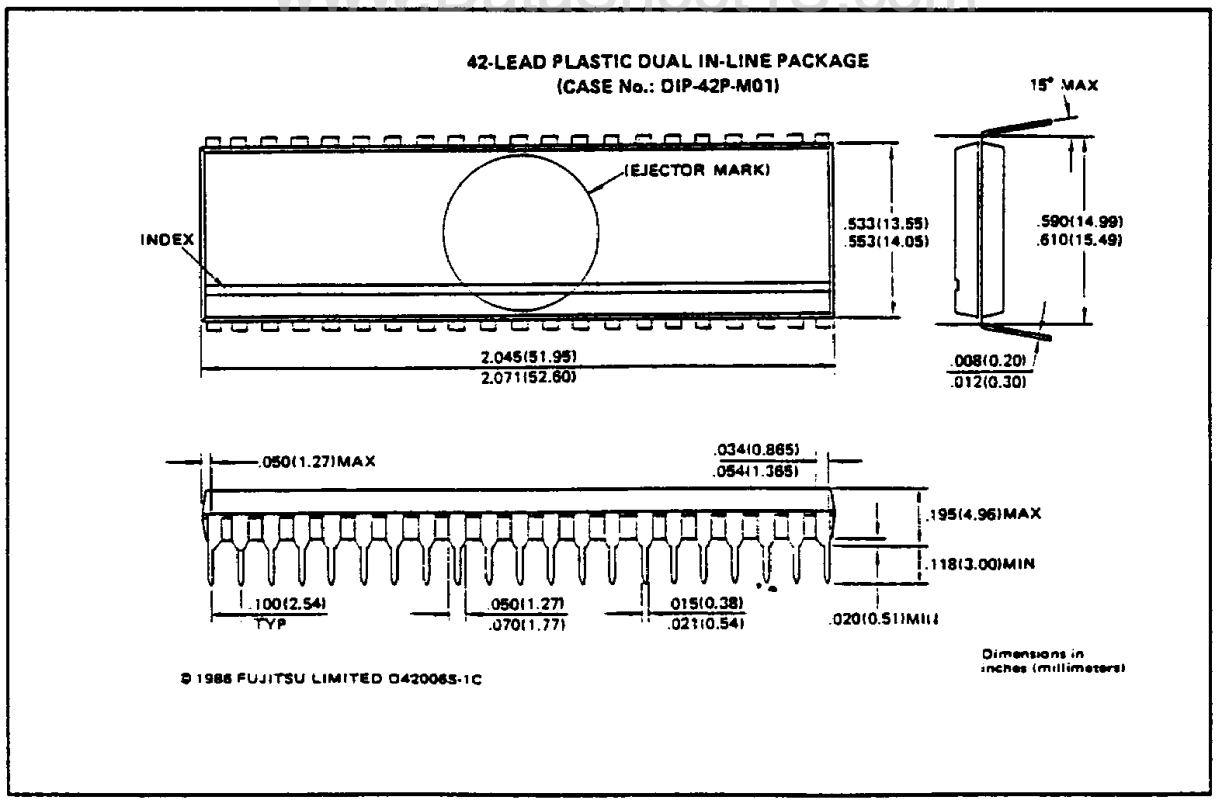
$$\text{Differential Linearity Error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \quad (LSB)$$

PACKAGE DIMENSION

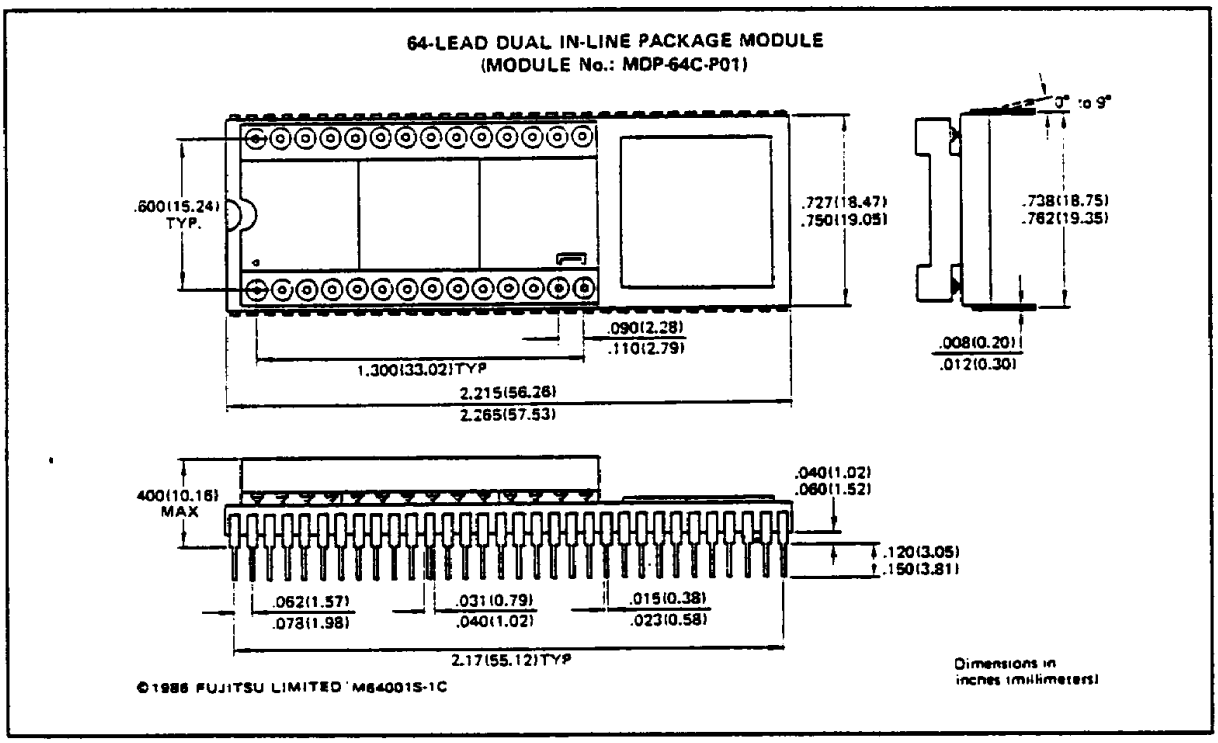
• MB88514B, MB88515B, and MB88516B: 64-PIN PLASTIC SHRINK DIP



• MB88517B: 42-PIN PLASTIC STANDARD DIP



• MB88518B: 64-PIN CERAMIC SHRINK MODULE



• MB88PG517B: 42-PIN CERAMIC MODULE