

Surface Mount Digital Step Attenuator

DAT-31A+ Series

50Ω 0 to 31 dB, 1.0 dB Step DC to 4.0 GHz

The Big Deal

- Wideband, operates up to 4 GHz
- Immune to latchup
- High IP3, 52 dBm



CASE STYLE: DG983-2

Product Overview

The DAT-31A+ series of 50Ω digital step attenuators provides adjustable attenuation from 0 to 31 dB in 1.0 dB steps. The control is a 5-bit serial/parallel interface, and the attenuators operate with either single positive or dual (positive and negative) supply voltage. DAT-31A+ series models are produced by a unique CMOS process on silicon, offering the performance of GaAs with the advantages of conventional CMOS devices.

Key Features

| Feature | Advantages |
|--|---|
| Wideband operation, specified from DC to 4.0 GHz | Can be used in multiple applications such as communications, satellite and defense, reducing part count. |
| Serial or parallel interface | Models available with serial or parallel interface mode to suit customer demand. |
| Good VSWR, 1.2:1 typ. | Eases interfacing with adjacent components and results in low amplitude ripple. |
| Single positive supply models: (Model suffixes: -SP+ and -PP+) +2.3 to +3.6V+ | Use of single positive supply simplifies power supply design. An internal negative voltage generator supplies the desired negative voltage. Single positive supply results in excellent spurious performance, -140 dBm typical. |
| Dual supply models: (Model suffixes: -SN+ and -PN+) +2.7 to +3.6V (Positive) and -3.6 to -3.2V (Negative) | Dual supply provides spurious-free operation. It also allows fast switching up to 1 MHz (vs. 25 kHz for single supply). |
| Useable over a wide range of supply voltages, +2.3/2.7 to 5.2V | Wide range of positive operating voltages allows the DAT-31A+ Series of models to be used in a wide range of applications. See Application Note AN-70-006 for operation above +3.6V |
| Footprint compatible to DAT-31-XX+ Series (XX=SN/SP/PN/PP) | Can fit into existing footprint and provide wideband performance, to 4 GHz instead of 2.4 GHz. |
| Safe attenuation transitions | The DAT-31A-XX+ series is designed to prevent any momentary positive 'spikes' in power during attenuation transitions |



Digital Step Attenuator

50Ω DC-4000 MHz

31 dB, 1.0 dB Step

5 Bit, Serial control interface, Single Supply Voltage

Product Features

- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Serial control interface
- Low Insertion Loss
- High IP3, +52 dBm Typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm

Typical Applications

- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

General Description

The DAT-31A-SP+ is a 50Ω digital step attenuator that provides adjustable attenuation of 0 to 31 dB in 1.0 dB steps. The control is a 5-bit serial interface, operating with a single (positive) supply voltage. DAT-31A-SP+ is produced by a unique CMOS process on silicon, offering the performance of GaAs with the advantages of conventional CMOS devices.



Generic photo used for illustration purposes only

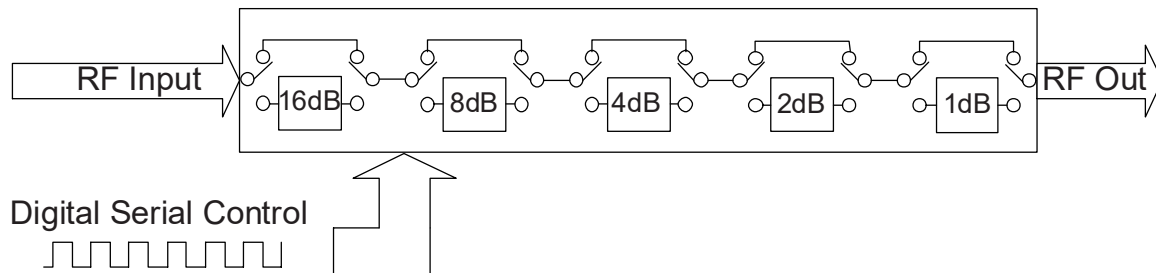
DAT-31A-SP+

CASE STYLE: DG983-2

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Simplified Schematic



RF Electrical Specifications^(Note1), DC-4000 MHz, T_{AMB}=25°C, V_{DD}=+3V

| Parameter | Freq. Range (GHz) | Min. | Typ. | Max. | Units |
|--|-------------------|------|------|------------|-------|
| Accuracy @ 1 dB Attenuation Setting | DC-1 | — | 0.02 | 0.1 | dB |
| | 1-2.4 | — | 0.05 | 0.15 | |
| | 2.4-4 | — | 0.1 | 0.25 | |
| Accuracy @ 2 dB Attenuation Setting | DC-1 | — | 0.05 | 0.15 | dB |
| | 1-2.4 | — | 0.15 | 0.25 | |
| | 2.4-4 | — | 0.15 | 0.35 | |
| Accuracy @ 4 dB Attenuation Setting | DC-1 | — | 0.07 | 0.2 | dB |
| | 1-2.4 | — | 0.15 | 0.25 | |
| | 2.4-4 | — | 0.23 | 0.5 | |
| Accuracy @ 8 dB Attenuation Setting | DC-1 | — | 0.03 | 0.2 | dB |
| | 1-2.4 | — | 0.15 | 0.5 | |
| | 2.4-4 | — | 0.6 | 0.8 | |
| Accuracy @ 16 dB Attenuation Setting | DC-1 | — | 0.1 | 0.3 | dB |
| | 1-2.4 | — | 0.15 | 0.7 | |
| | 2.4-4 | — | 1.1 | 1.45 | |
| Insertion Loss ^(note 2) @ all attenuator set to 0dB | DC-1 | — | 1.3 | 1.9 | dB |
| | 1-2.4 | — | 1.6 | 2.4 | |
| | 2.4-4 | — | 2.1 | 3.0 | |
| Input IP3 ^(note 3) (at Min. and Max. Attenuation) | DC-4 | — | +52 | — | dBm |
| Input Power @ 0.2dB Compression ^(Note 3) (at Min. and Max. Attenuation) | DC-4 | — | +24 | — | dBm |
| Input Operating Power | 10 kHz to 50 MHz | — | — | See Fig. 1 | dBm |
| | >50 MHz | — | — | +24 | |
| VSWR | DC-1 | — | 1.2 | 1.5 | :1 |
| | 1-2.4 | — | 1.2 | 1.6 | |
| | 2.4-4 | — | 1.4 | 1.9 | |

Notes:

1. Tested on Evaluation Board TB-334, See Figure 3.
2. Insertion loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @ 100MHz, 0.35dB @ 1000MHz, 0.60dB @ 2400MHz, 0.75dB @ 4000MHz).
3. Input IP3 and 1dB compression degrade below 1 MHz. Input power not to exceed max operating specification for continuous operation.

DC Electrical Specifications

| Parameter | Min. | Typ. | Max. | Units |
|----------------------------------|------|------|-------------------------|-------|
| V _{DD} , Supply Voltage | 2.3 | 3 | 3.6 ^(Note 4) | V |
| I _{DD} Supply Current | — | — | 200 | µA |
| Control Input Low | -0.3 | — | +0.6 | V |
| Control Input High | 1.17 | — | 3.6 | V |
| Control Current | — | — | 20 ^(Note 5) | µA |

4. For operation above +3.6V, see Application Note AN-70-006
5. Except, 30µA typ for C16 at +3.6V

Absolute Maximum Ratings^(Note6,7)

| Parameter | Ratings |
|------------------------------|-----------------------|
| Operating Temperature | -40°C to 105°C |
| Storage Temperature | -65°C to 150°C |
| V _{DD} | -0.3V Min., 5.5V Max. |
| Voltage on any control input | -0.3V Min., 3.6V Max. |
| Input Power | +30dBm |
| Thermal Resistance | 37°C/W |

6. Permanent damage may occur if any of these limits are exceeded.
7. Operation between max operating and absolute max input power will result in reduced reliability.

Switching Specifications

| Parameter | Min. | Typ. | Max. | Units |
|--|------|------|------|-------|
| Switching Speed, 50% Control to 0.5dB of Attenuation Value | — | 1.0 | — | µSec |
| Switching Control Frequency | — | — | 25 | kHz |

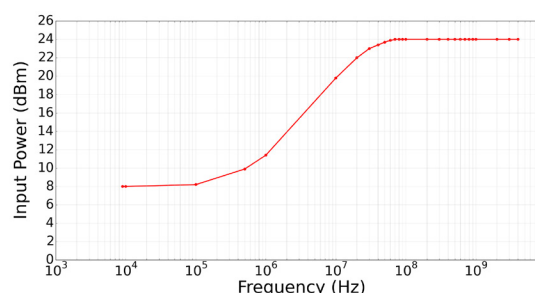
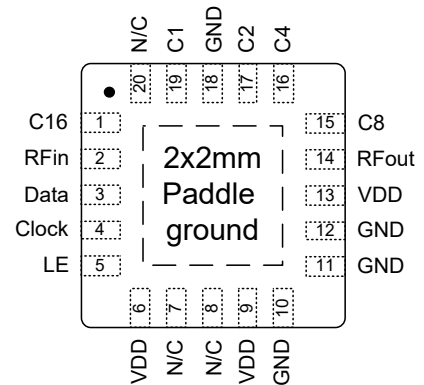


Figure 1. Max Input Operating Power vs Frequency

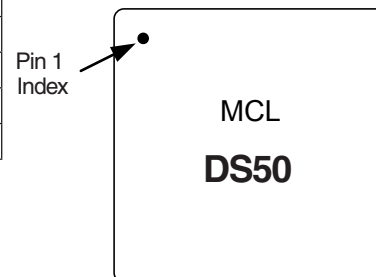
Pin Description

| Function | Pin Number | Description |
|-----------------|------------|---|
| C16 | 1 | Control for Attenuation bit, 16dB (Notes 3,4,6) |
| RF in | 2 | RF in port (Note 1) |
| Data | 3 | Serial Interface data input (Note 3) |
| Clock | 4 | Serial Interface clock input |
| LE | 5 | Latch Enable Input (Note 2) |
| V _{DD} | 6 | Positive Supply Voltage |
| N/C | 7 | Not connected |
| N/C | 8 | Not connected |
| V _{DD} | 9 | Positive Supply Voltage |
| GND | 10 | Ground connection |
| GND | 11 | Ground connection |
| GND | 12 | Ground connection (Note 7) |
| V _{DD} | 13 | Positive Supply Voltage (Note 8) |
| RF out | 14 | RF out port (Note 1) |
| C8 | 15 | Control for attenuation bit, 8 dB (Note 4) |
| C4 | 16 | Control for attenuation bit, 4 dB (Note 4) |
| C2 | 17 | Control for attenuation bit, 2 dB (Note 4) |
| GND | 18 | Ground Connection |
| C1 | 19 | Control for attenuation bit, 1 dB (Note 4) |
| N/C | 20 | Not Connected (Note 9) |
| GND | Paddle | Paddle ground (Note 5) |

Pin Configuration (Top View)



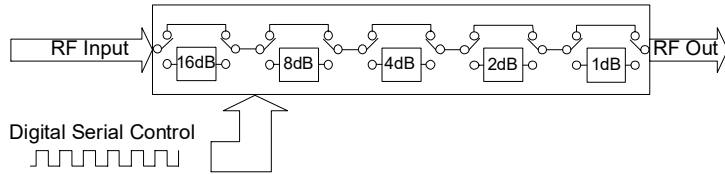
Device Marking



Notes:

- Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
- Latch Enable (LE) has an internal 2MΩ to internal positive supply voltage.
- Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
- Refer to Power-up Control Settings.
- The exposed solder pad on the bottom of the package (See Pin configuration) must be grounded for proper device operation.
- This pin has an internal 200 kΩ resistor to ground.
- Ground must be less than 80 mil (0.08") from pin 12 proper device operation.
- When VDD ≤ 3.6V this pin may be connected directly to VDD, when 3.6V < VDD ≤ 5.2V need to use a voltage divider to reduce voltage on this pin to a voltage in the range +1.17 to 3.6V. See Application note AN-70-006.
- Place a shunt 10kΩ resistor to ground.

Simplified Schematic



The DAT-31A-SP+ serial interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

| Table 1. Truth Table | | | | | |
|----------------------|-----|----|----|----|----|
| Attenuation State | C16 | C8 | C4 | C2 | C1 |
| Reference | 0 | 0 | 0 | 0 | 0 |
| 1 (dB) | 0 | 0 | 0 | 0 | 1 |
| 2 (dB) | 0 | 0 | 0 | 1 | 0 |
| 4 (dB) | 0 | 0 | 1 | 0 | 0 |
| 8 (dB) | 0 | 1 | 0 | 0 | 0 |
| 16 (dB) | 1 | 0 | 0 | 0 | 0 |
| 31 (dB) | 1 | 1 | 1 | 1 | 1 |

Note: Not all 32 possible combinations of C1 - C16 are shown in table

The serial interface is a 5-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by **Figure 2** (Serial Interface Timing Diagram) and **Table 2** (Serial Interface AC Characteristics).

Figure 2: Serial interface Timing Diagram

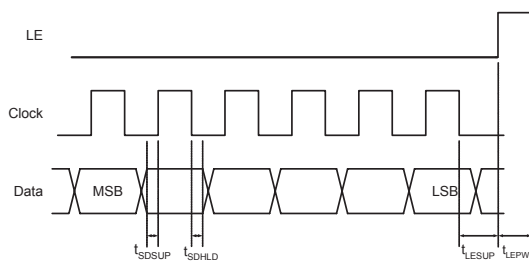


Table 2. Serial Interface AC Characteristics


| Symbol | Parameter | Min. | Max. | Units |
|-------------|--|------|------|-------|
| f_{clk} | Serial data clock frequency (Note 1) | | 10 | MHz |
| t_{clkH} | Serial clock HIGH time | 30 | | ns |
| t_{clkL} | Serial clock LOW time | 30 | | ns |
| t_{LESUP} | LE set-up time after last clock falling edge | 10 | | ns |
| t_{LEPW} | LE minimum pulse width | 30 | | ns |
| t_{SDSUP} | Serial data set-up time before clock rising edge | 10 | | ns |
| t_{SDHLD} | Serial data hold time after clock falling edge | 10 | | ns |

Note 1. f_{clk} verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify f_{clk} specification.


The DAT-31A-SP+, uses a common 5-bit serial word format, as shown in **Table 3: 5-Bit attenuator Serial Programming Register Map**.

The first bit, the MSB, corresponds to the 16 dB Step and the Bit B1 corresponds to the 1.0 dB step.

| Table 3. 5-Bit attenuator Serial Programming Register Map | | | | | |
|--|----|----|----|----|----|
| B5 | B4 | B3 | B2 | B1 | B0 |
| C16 | C8 | C4 | C2 | C1 | 0 |



MSB
(first in)



LSB
(last in)

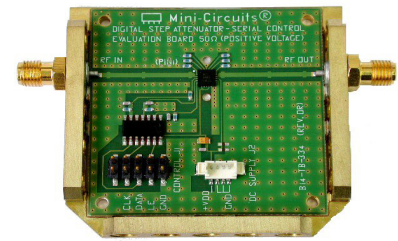
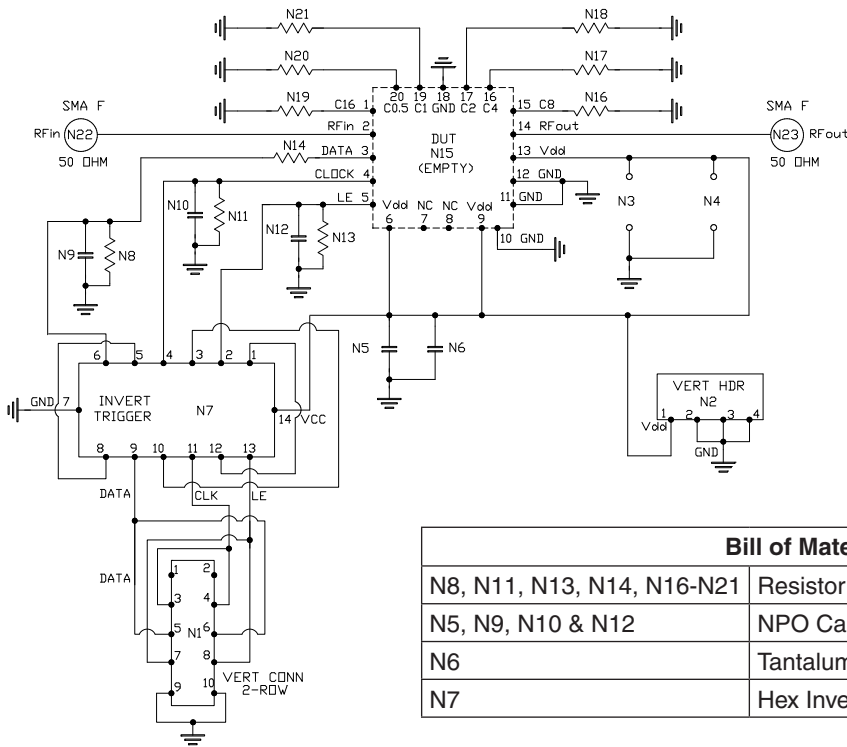
Note: The stop bit (B0) must always be low to prevent the attenuator from entering an unknown state.

Power-up Control Settings

The DAT-31A-SP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided.

When the attenuator powers up, the five control bits are set to whatever data is present on the five data inputs (C1 to C16).

This allows any one of the 32 attenuation settings to be specified as the power-up state.



TB-334

| Bill of Materials | |
|----------------------------|---------------------------------------|
| N8, N11, N13, N14, N16-N21 | Resistor 0603 10 KOhm +/- 1% |
| N5, N9, N10 & N12 | NPO Capacitor 0603 100pF +/- 5% |
| N6 | Tantalum Capacitor 0805 100nF +/- 10% |
| N7 | Hex Invert Schmitt Trigger MSL1 |

Notes

1. Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
2. Test Board TB-334 is designed for operation for VDD=2.3 to 3.6V. For operation over 3.6V to 5.2V, See Application Note AN-70-006
3. VDD=Vdd

Fig 3. Evaluation Board Schematic, TB-334, used for characterization (DUT not soldered on TB-334)

Test Equipment

- For Insertion Loss, Isolation and Return Loss:**
Agilent's E5071C Network Analyzer & E3631A Power Supply.
- For Compression:**
Agilent's N9020A Signal Analyzer, E8247C RF Generator, E3631A Power Supply & U2004A Power Sensor.
- For Input IP3:**
Agilent's N9020A Signal Analyzer, N5181A Signal Generators, E3631A Power Supply, U2004A Power Sensor.
- For Spurs:**
Agilent N5181A Signal Generator, E4440A Spectrum Analyzer.
- For Switching Time:**
Agilent's N5181A Signal Generator, 81110A Pulse Generator, 54832B Oscilloscope, E3631A Power Supply.
- For Max Control Frequency:**
Agilent's N5181A Signal Generator, N9020A Signal Analyzer, E3631A Power Supply, 81110A Pulse Generator.

Measurement Conditions

- For Insertion Loss, Isolation and Return Loss:**
VDD=+2.3/+3/+5.5V & Pin=0dBm
- For Compression:** Pin=0/+24dBm. VDD=+3V
- For Input IP3:** Pin=+10dBm/tone.
Tone spacing: 0.1 MHz to 1 MHz RF Freq and 1 MHz to 4200 MHz RF Freq, VDD=+3V
- For Spurs:** RF IN at 1000MHz and -20dBm. VDD=+3V
- For Switching Time:**
RF Freq=501MHz/0dBm, Pulse for LE=1Hz/0/+3.4V, Delay=500ms, Width=500ms. VDD=+3V
- For Max Control Frequency:**
RF Freq=501MHz, 0dBm. VDD=+3V

| Additional Detailed Technical Information | |
|---|--|
| <i>additional information is available on our dash board. To access this information click here</i> | |
| Performance Data | Data Table |
| | Swept Graphs |
| | S-Parameter (S2P Files) Data Set (.zip file) |
| Case Style | DG983-2 <i>Plastic package, exposed paddle, lead finish: NiPdAu</i> |
| Tape & Reel Standard quantities available on reel | F87 <i>7" reels with 20, 50, 100 or 200 devices</i> <i>13" reels with 3K devices</i> |
| Suggested Layout for PCB Design | PL-191 |
| Evaluation Board | TB-334 |
| Environmental Ratings | ENV33T1 |

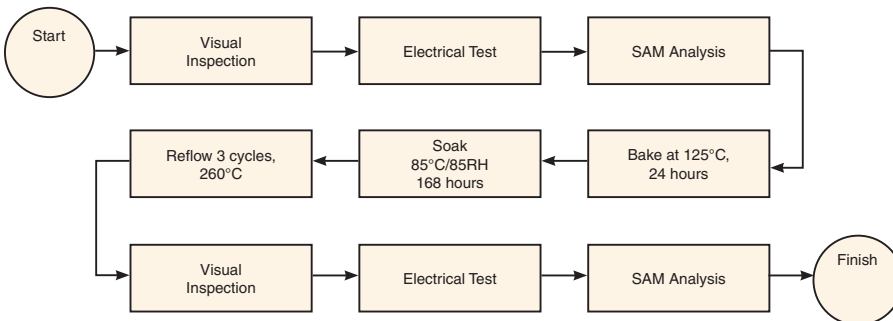
ESD Rating

Human Body Model (HBM): Class 1C (1000 to <2000V) in accordance with MIL-STD-883 method 3015

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



Additional Notes

- Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
- The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp