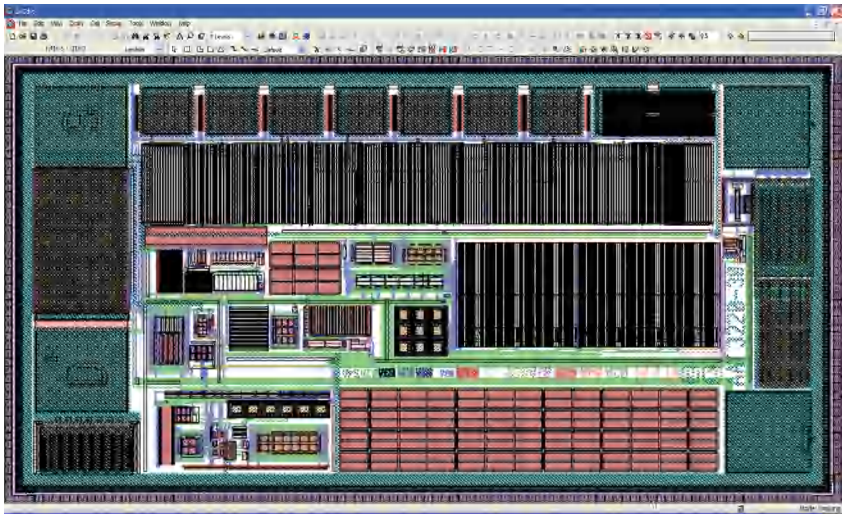
ANALOG/MIXED-SIGNAL (AMS)
DESIGN AND VERIFICATION

Tanner L-Edit IC

D A T A S H E E T



Tanner L-Edit IC chip view; the layout tool is a comprehensive analog/mixed-signal (AMS) IC physical design environment.

A Complete IC Physical Design Environment

Tanner L-Edit IC is an analog/mixed-signal (AMS) IC physical design environment that gives you all the features you need to quickly and efficiently finish the layout of your design, including:

- Schematic Driven Layout (SDL) capability that allows you to create layout that matches the schematic the first time
- Interactive DRC displays violations in real time while you edit your layout
- Node Highlighting for connectivity visualization
- Pad I/O cross reference for easy generation of bonding reports

L-Edit increases your productivity by reading and writing directly to an OpenAccess database, enabling you to share designs with third-party tools. Work in teams with multi-user support that can implicitly lock a cell when you start editing and then release it when the window is closed. Save time by using foundry-provided files directly, allowing you to avoid having to set up technology information manually. Maximize efficiency with L-Edit's physical design features, reduce your CAD manager's support burden, and get up and running easily with platform independence and flexible licensing.

Create Layout with Precision

L-Edit provides greater precision by enabling you to perform complex Boolean and derived layer operations with polygons of arbitrary shape and curvature. Perform AND, OR, XOR, Subtract, Grow, and Shrink on groups of objects. Display coordinate and distance values in any technology unit, and automatically add guard rings around any shape. Further increase your productivity by mapping multiple layout functions to a single keystroke.

FEATURES AND BENEFITS:

- Complete hierarchical physical layout including all-angle and curved polygons
- Fast rendering
- Reads and writes OpenAccess with multi-user support
- Schematic Driven Layout (SDL) that imports netlists and automatically generates parameterized cells and instances them into your design
- Import Cadence Virtuoso technology and display files
- Interactive (real-time) DRC displays violations as you edit
- Cross-probe between schematic, layout, and LVS report to highlight nets or devices
- Node highlighting for connectivity visualization
- Object snapping (gravity) for quick, accurate layout
- Increase routing productivity with automated instancing of parameterized cells, real-time net flylines, net completion tracking, geometry marking/highlighting/ by net and ECO tracking
- Pad I/O cross reference for easy generation of bonding reports
- Platform independence on Windows or Linux
- Ease of use: Intuitive and quick learning curve
- Unparalleled customer support
- Flexible licensing

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L-Edit additionally allows you to:

- Perform complete hierarchical physical layout with all-angle and curved polygons on an unlimited number of layers
- Use orthogonal, 45°, all-angle, and curved drawing modes
- View your design with the fastest rendering
- Use a command line interface for run-time automation

Speed Layout with SDL

- Read in a netlist and automatically generate parameterized cells and instance them into your design
- Display flylines to allow you to place your blocks to minimize routing congestion
- Mark existing geometry as part of a specific net allowing selection and rip-up of geometry (by net)
- Perform engineering change orders (ECO) and highlight differences in the netlists
- Use netlist files in T-Spice, HSPICE, PSpice, structural Verilog or CDL formats
- Check for connectivity issues using Tanner's SDL short and open Connectivity Checker
- Assemble your chip using the SDL auto router

L-Edit also supports parameterized cells called T-Cells. With T-Cells, create versatile source cells that consist of user-defined input parameters and layout-generating code. T-Cells extend traditional geometry cells to include the flexibility and automation of L-Edit's user-programmable interface (UPI).

L-Comp, a set of high-level composition functions, provides a simple toolkit for creating T-Cell code. Use L-Comp to efficiently create, place, and align cell instances in a design.

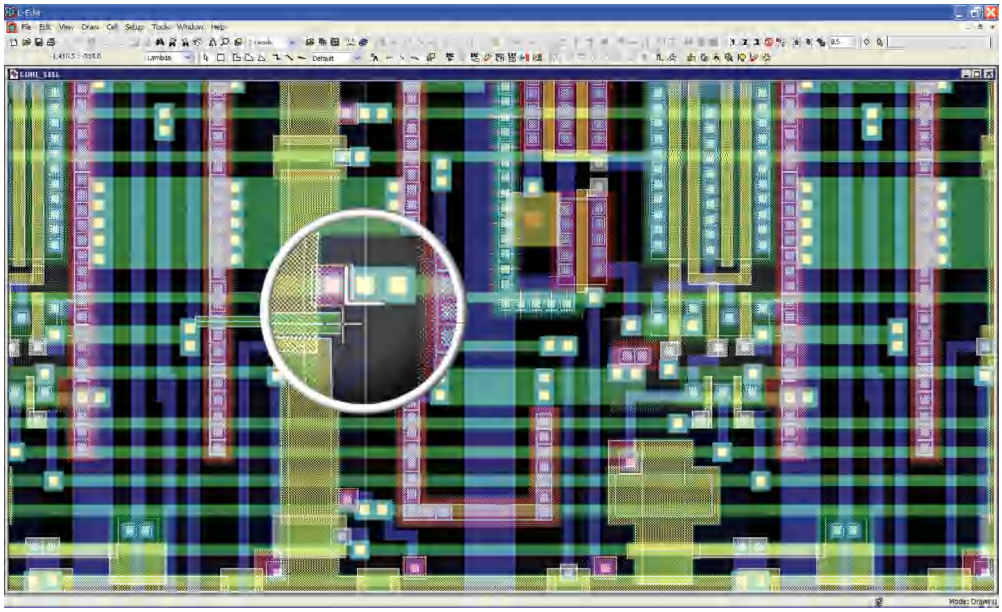
Navigate Efficiently

L-Edit provides a built-in Libraries Navigator that enables you to:

- Efficiently traverse design hierarchy with top-down and bottom-up hierarchical view, non-instanced cells view, or cells view sorted by modified date
- Drag and drop cells into layout from library files, other design files, or the current design database
- View layout details down to any level of the hierarchy
- Lock and unlock cells to protect the design from any changes
- Easily replace instances of one cell with another cell, at the current level or throughout the design
- Maximize IP reuse with L-Edit's multiple library support
- Cross-probe between schematic, layout, and LVS report to highlight nets or devices

Gain Complete Control Over Editing

L-Edit gives you the flexibility and control you need to master the editing process. You can dramatically streamline the process by editing the properties of multiple objects simultaneously. With L-Edit you can instantly push down the hierarchy to any object, making it easy to edit edges, corners, and arcs. You can quickly stretch or shrink multiple edges to make room for more layout.



Tanner L-Edit interactive DRC displays violations in real time while you edit your layout, helping you create compact, error-free layouts the first time.

Other features that help streamline editing include:

- Change the current drawing layer directly from the layout using the virtual layer palette
- Perform unlimited undo and redo operations
- Perform all-angle rotate, flip, merge, nibble, and slice operations
- Speed drawing and editing by snapping the cursor to object vertices, edges, midpoints, center points, intersections, and instances
- Perform one-click horizontal or vertical object alignment, equally space objects, or tile objects horizontally, vertically, or in a 2D array
- Specify a reference point for editing operations such as object rotation, flip, move, or instance placement using the base point feature
- Pad I/O cross reference for easy generation of bonding reports
- High-resolution plotter support with the same rendering scheme used in L-Edit, including legends, rulers, and headers
- Populate wafers with maximum number of die and label all dies on a wafer with WaferTools
- CurveTools add chamfers and fillets quickly to your layout. It adds fillets of equal width to wires and processes multiple edges as a single edge when working with curved objects that have been converted to all-angle objects
- LayerFill easily adds dummy fills to your layout to meet density requirements of deep submicron designs
- MaskBias performs easy mask resizing on a layer by layer basis

Work in a Versatile Environment

Save time and money with L-Edit's ease-of-use benefits:

- Delivers powerful features from an affordable, customizable, easy-to manage tool
- Offers a short learning curve
- Enables you to import and export GDS, OASIS© (from SEMI©), DXF, Gerber and CIF file formats
- Provides multi-language menus (English, Japanese, Simplified and Traditional Chinese, German, Italian, and Russian)
- Customize and filter the Layer Palette to show only layers used in the file, current cell, or cell and its hierarchy, allowing you to finish your layout faster
- Enables you to easily copy and paste layout into your documentation flow

Tanner L-Edit node highlighting offers connectivity visualization so you can quickly find/fix LVS problems.

Additional productivity features:

- Cross-section viewer
- Layout vs Layout comparison
- Area calculator
- PostScript mask export for high resolution transparency MEMS masks

Generate Layout for Parameterized Devices

Tanner DevGen (formerly HiPer DevGen) provides layout generators for most common devices. It is easy to configure for any process to help ensure DRC correct layout. Devices include MOSFET, resistor, capacitor, current mirror, and differential pair Generators. DevGen with SDL can recognize current mirror and differential pair configurations and generates consistent, high quality layout that is parasitic aware and guarantees the best matching. For specialized devices, use L-Edit's automatic layout to T-Cell generator to quickly complete your T-Cell library.

Create Automation Macros

L-Edit's powerful UPI allows you to create macros that automate layout manipulations, geometric synthesis, batch verification, and advanced analysis. You can further increase your productivity by mapping multiple layout functions to a single keystroke. UPI macros are written in TCL, C and C++ languages and can be executed with directly in L-Edit or compiled as a DLL.

Correct Layout as-you-go with Interactive DRC

L-Edit Interactive DRC displays violations in real time while you edit your layout, helping you create compact, error-free layouts the first time. Interactive DRC simultaneously checks for violations between objects in the same cell and down through the cell hierarchy. You can display the distance to the two closest edges while editing and have Interactive DRC prevent violations by not allowing you to draw or edit a shape that would cause a violation.

Streamline Verification with Node Highlighting

L-Edit Node Highlighting offers connectivity visualization so you can quickly find and fix LVS problems.

- Point to an object in the layout, regardless of hierarchy, and display all the geometry connected to it based on a set of connectivity rules
- Highlight discrepancies between the schematic netlist and the extracted netlist in the layout
- View multiple nodes in different colors
- Track down shorts and opens
- Improve design productivity significantly during LVS

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