TC40H374P/F

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H374 OCTAL D-TYPE FLIP-FLOP (3-STATE OUTPUT)

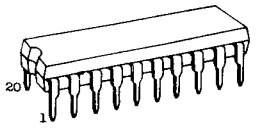
The TC40H374 is an octal D-type flip-flop having 3-state output control terminal.

When OUTPUT-CONTROL input is at "L" level, the data is transmitted to the output at the rising edge of CLOCK.

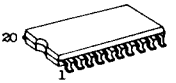
Further, when OUTPUT-CONTROL input is set to "H" level, high impedance is given to the output regardless of the other inputs.

Eight circuits have a common CLOCK and a common OUTPUT-CONTROL input.

The function and pin assignment of the TC40H374 are the same as those of the 74LS374.



DIP20(3D20A-P)

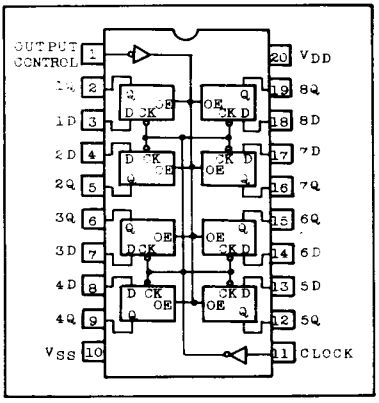


MFP20(F20GA-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN CONNECTION

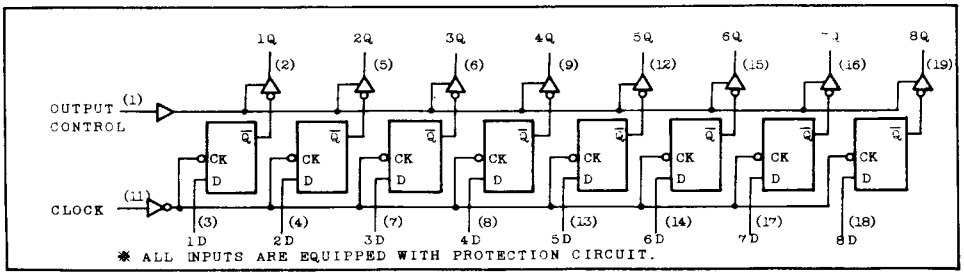


TRUTH TABLE

INPUTS			OUTPUT
OUTPUT CONTROL	CLOCK	DATA	Q
L	↑	H	H
L	↑	L	L
L	↓	*	Q_0 (NO CHANGE)
H	*	*	HIGH IMPEDANCE

* Don't care

BLOCK DIAGRAM



* ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	4.7	-	4.4	-	-	4.0	-	mA
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|<1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H"Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L"Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Output Disable Current	"H"Level	I_{DH}	V_{DH}=8.0V	8	-	0.5	-	10^{-4}	0.5	-	5	μA
	"L"Level	I_{DL}	V_{DL}=0.0V	8	-	-0.5	-	-10^{-4}	-0.5	-	-5	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	12.5	-	10^{-3}	12.5	-	75	μA

* All valid input combinations.

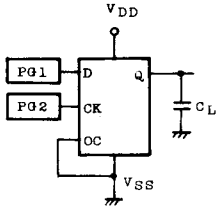
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF, R_L=1kΩ)

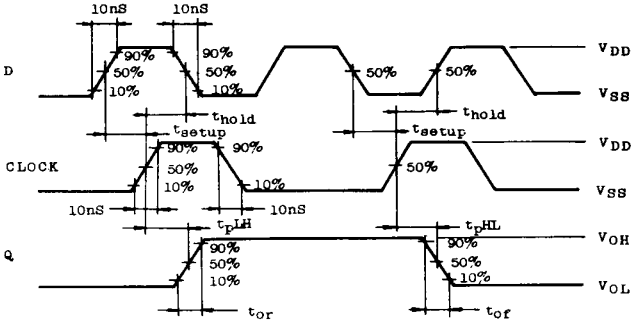
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig.1	-	15	30	ns
Output Fall Time		t_{of}		-	13	30	ns
Propagation Delay Time	Low-High Level	t_{pLH}	CLOCK - Q Fig.1	-	38	57	ns
	High-Low Level	t_{pHL}		-	35	53	ns
Output Disable Time	High Level	t_{pHZ}	OUTPUT CONTROL - Q Fig.2, 3	-	24	36	ns
	Low Level	t_{pLZ}		-	26	39	ns
Output Enable Time	High Level	t_{pZH}		-	24	36	ns
	Low Level	t_{pZL}		-	28	42	ns
Maximum Clock Frequency		$f_{max\phi}$		10	25	-	MHz
Maximum Clock Rise/Fall Time		$t_{r\phi},t_{f\phi}$		1.0	10	-	μs
Minimum Data Set up Time		$t_{set\text{-}up}$	Fig.1	-	-	25	ns
Minimum Data Hold Time		t_{hold}	Fig.1		-	15	ns
Input Capacitance		C_{IN}		-	5		pF
Output Capacitance		C_{OUT}		-	12		pF

TC40H374P/F

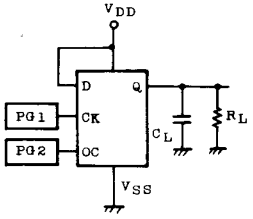
SWITCHING TIME TEST CIRCUIT AND WAVEFORM

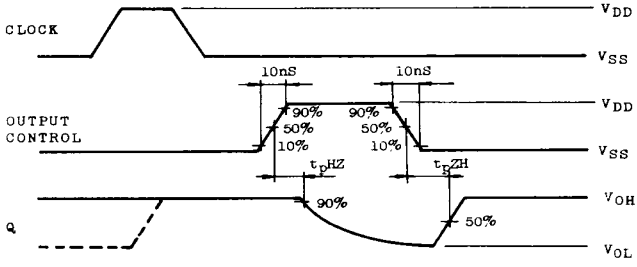
CIRCUIT 1



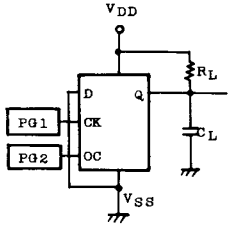


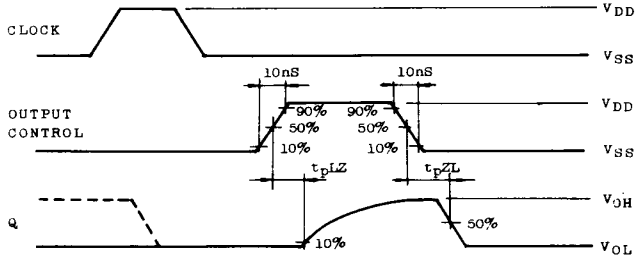
CIRCUIT 2



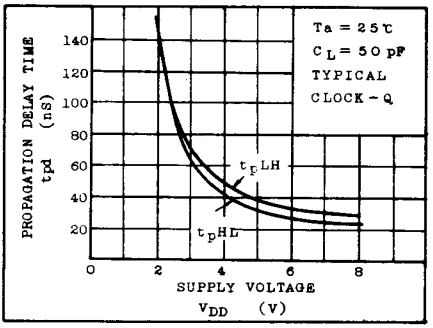


CIRCUIT 3

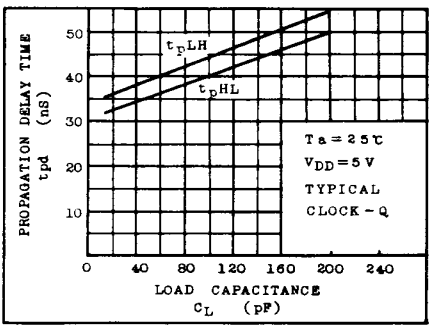




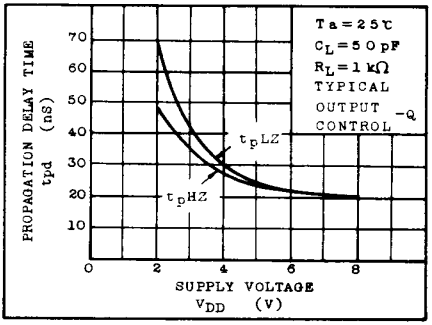
t_{pd} - V_{DD}



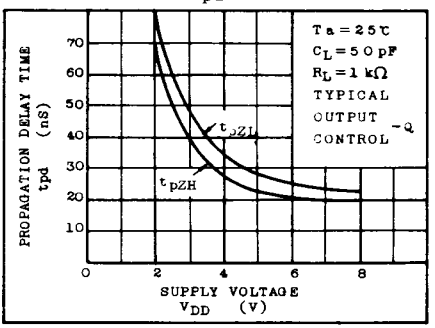
t_{pd} - C_L



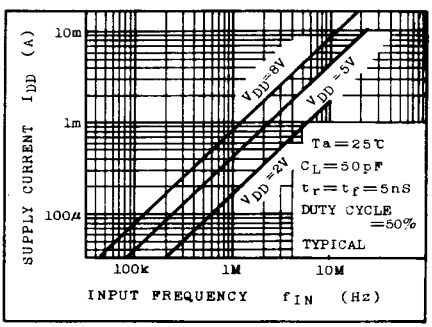
t_{pd} - V_{DD}



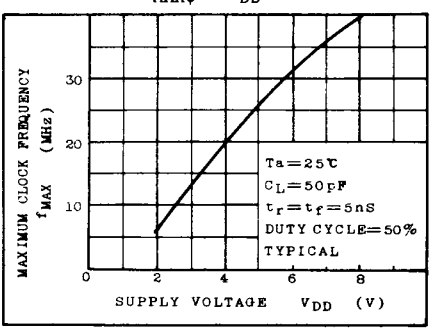
t_{pd} - V_{DD}



I_{DD} - f_{IN}

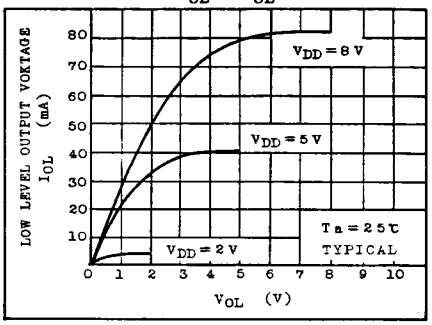


$f_{MAX\phi}$ - V_{DD}



TC40H374P/F

I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})