Freescale Semiconductor, Inc.

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MC68340

ADDENDUM TO

MC68340 Integrated Processor With DMA User's Manual - Rev 1

December 8, 1994

General - AESOP Bulletin Board

Latest information on this product is maintained on the AESOP BBS at (800)843-3451 (US and Canada) or (512)891-3650. Configure modem up to 14.4K baud, 8 bits, 1 stop bit, and no parity. Terminal should support VT100 emulation.

1. Operand Alignment

On page 3-7, third paragraph (under 3.2.2), change the first two lines to: "The CPU32 restricts all operands (both data and instructions) to be word-aligned. That is, word and long-word operands must be located on a word boundary." Long-word operands do not have to be long-word aligned.

2. Additional Note on MBAR Decode

Add to the CPU Space Cycles description on page 3-21: The CPU space decode logic allocates the 256-byte block from $3FF00-3FFFF to the SIM module. An internal 2-clock termination is provided by this initial decode for any access to this range, but selection of specific registers depends on additional decode.

Accesses to the MBAR register at long word $3FF00 are internal only, and are only visible by enabling show cycles. Users should directly access only the MBAR register, and use the LPSTOP instruction to generate the LPSTOP broadcast access to $3FFFE. The remaining address range $3FF04-3FFFD is Motorola reserved and should not be accessed.

3. Additional Notes on CPU Space Address Encoding

On page 3-21, Figure 3-10, the BKPT field for the Breakpoint Acknowledge address encoding is on bits 4-2, and the T bit is on bit 1. The Interrupt Acknowledge LEVEL field is on bits 3-1.

4. Breakpoints

On page 3-22, the first paragraph implies that either a software breakpoint (BKPT instruction) or hardware breakpoint can be used to insert an instruction. As noted in the following paragraphs, only a software breakpoint can be used to insert an instruction on the breakpoint acknowledge cycle.

5. Interrupt Latency

Add to the Interrupt Acknowledge Bus Cycles section on page 3-27: Interrupt latency from IRQx assert to prefetch of the first instruction in the interrupt handler is about 37 clocks + worst case instruction length in clocks (using 2-clock memory and autovector termination). From the instruction timing tables, this gives 37+71 (DIVS.L with worst-case <fea>) = 108 clocks worst case interrupt latency time. For applications requiring shorter interrupt response time the latency can be reduced by using simpler addressing modes and/or avoiding use of longer instructions (specifically DIVS.L, DIVU.L, MUL.L).

6. Interrupt Hold Time and Spurious Interrupts

Add to the Interrupt Acknowledge Bus Cycles section on page 3-27: All interrupts (including level 7) are level sensitive and must remain asserted until the corresponding IACK cycle; otherwise, a spurious interrupt exception may result or the interrupt may be ignored entirely. This is also true for external interrupts which are autovectored using either the AVEC signal or the AVEC register, since the SIM will not respond to an interrupt arbitration cycle on the IMB if the external interrupt at that level has been removed.

7. Typos in IACK Cycle Timing Waveforms

On page 3-29, Figure 3-15, the text "VECTOR FROM 16-BIT PORT" should be on D7-D0, and "VECTOR FROM 8-BIT PORT" should be on D15-D8. The responding device returns the vector number on the least significant byte of the data port.

8. Additional Note on Internal Autovector Operation

Add to the Autovector Interrupt Acknowledge Cycle section on page 3-29: If an external interrupt level is autovectored either by the AVEC register programming or the external AVEC signal, an external IACK will be started and terminated internally. The interrupting device should not respond to this IACK in any way, or the resulting operation is undefined.

9. Additional Notes on Retry Termination

On page 3-33 , Table 3-4: When $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are asserted together in case #5 to force a retry of the current bus cycle, relative timing of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ must be controlled to avoid inadvertantly causing bus error termination case #3. This can be done by asserting $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ either synchronously to the clock to directly control which edge each is recognized on, or asynchronously with $\overline{\text{HALT}}$ asserted for time [spec 47A+spec 47B] ns before $\overline{\text{BERR}}$ to guarantee recognition on or before the same clock edge as $\overline{\text{BERR}}$.

10. Active Negate on Bus Arbitration

The 68340 actively pulls up all tri-stateable bus pins other than the data bus before tristating them during bus arbitration. This pullup funtion is not guaranteed to result in spec VOH levels before tristating, but will help reduce rise time on these signals when using weak external bus pullups.

11. Additional Note on Bus Arbitration Priority

For the bus arbitration description beginning on page 3-40: The arbitration priority between possible bus masters for this device is external request via $\overline{\text{BR}}$ (highest priority), DMA, then CPU (lowest). The priority of DMA channels 1 and 2 relative to each other is selected by their respective MAID levels which must be unique (on current silicon if they are the same DMA channel 1 defaults to highest priority).

12. Additional Note on Bus Arbitration and Operand Coherency

For the bus arbitration description beginning on page 3-40: Each bus master maintains operand coherency when a higher priority request is recognized. For example, a CPU write of a long-word operand to a byte port results in a sequence of four bus cycles to complete the operand transfer - the CPU will not release the bus until the completion of the fourth bus cycle. A single address DMA transfer is handled in a similar manner. For a dual address DMA transfer, the read and write portions are handled as separate operands, allowing arbitration between the read and write bus cycles. Also, if different port sizes are specified in the DMA configuration for the source and destination, arbitration can occur between each of the multiple operand accesses which must be made to the smaller port for each operand access to the larger port. The RMC read/write sequences for a TAS instruction is also indivisible to guarantee data coherency. Arbitration is allowed between each operand transfer of a multi-operand operation such as a MOVEM instruction or exception stacking.

13. Additional Notes on RESET Interaction with Current Bus Cycle

Add to the Reset Operation description beginning page 3-46:

Hardware resets are held off until completion of the current operand transfer in order to maintain operand coherency. The processor resets at the end of the bus cycle in which the last portion of the operand is transfered, or after the bus monitor has timed out. The bus monitor operates whether it is enabled or not, for the period of time that the BMT bits are set to.

The following reset sources reset all internal registers to their reset state: external, POR, software watchdog, double bus fault, loss of clock. Execution of a RESET instruction resets the peripheral module registers (serial, DMA, timers) with the exception of the MCR registers. The MCR register in each module, the SIM40 registers, and the CPU state are not affected by execution of a RESET instruction.

14. External Reset

On page 3-47 , Figure 3-27, the $\overline{\text{RESET}}$ signal negates for two clocks between internal and external assertions, not one. Note that $\overline{\text{RESET}}$ is not actively negated, and its rise time is dependent on the pullup resistor used.

15. Power-On Reset

On page 3-48, Figure 3-28. Power-Up Reset Timing Diagram: CLKOUT is not gated by VCO lock or other internal control signals, and can begin toggling as soon as VCC is high enough for the internal logic to begin operating. For crystal mode and external clock with VCO mode, after the VCO frequency has reached an initial stable value, the 328*TCLKIN delay is counted down, and VCO lock is set after completion of the 328 clock delay. For external clock mode without VCO, the 328*TCLKIN delay starts as soon as EXTAL clock transitions are recognized. See note for page10-3 for more POR information.

Beginning with the F77J mask set (rev C suffix product e.g. MC68340FE16C), the delay to VCO lock for external clock with VCO mode is 1864 clocks.

16. Internal IMB Arbitration

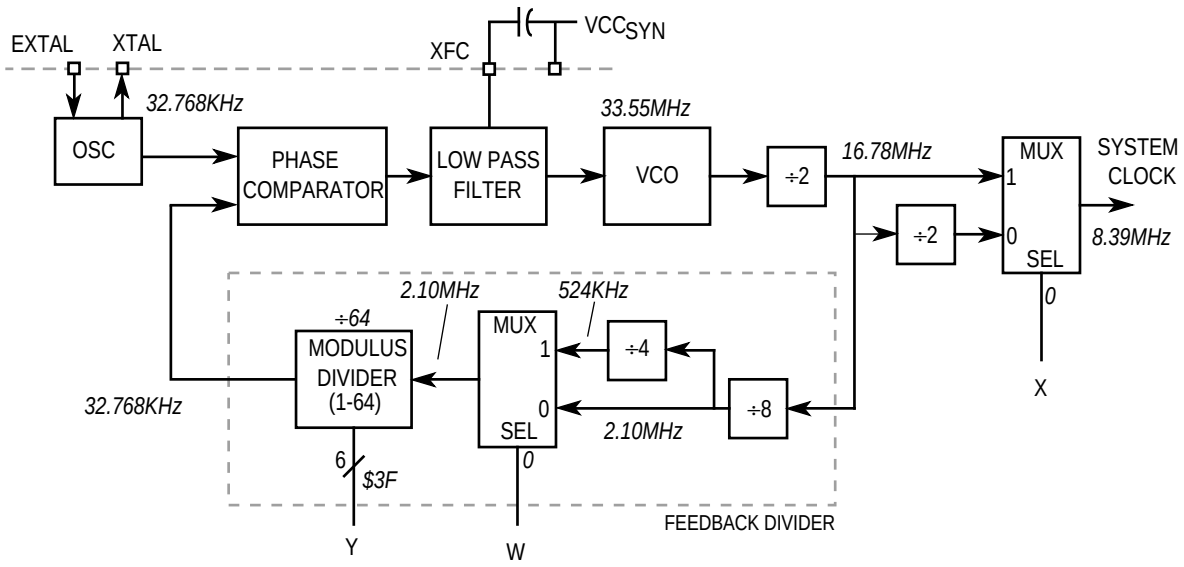
On page 4-6, first paragraph, change the first sentence to read "There are eight arbitration levels for the various bus masters on the MC68340 to access the inter-module bus (IMB)."

17. Additional Note for External Clock Mode with PLL

On page 4-9 External Clock Mode with PLL: the PLL phase locks the CLKOUT falling edge to the falling edge of the EXTAL input clock. Maximum skew between falling edges of the EXTAL and CLKOUT signals is specified in the Section 11 Electrical Characteristics.

18. VCO Block Diagram

The clock output from the VCO block shown in Figure 4-4 on page 4-10 is actually the VCO output divided by two. See the corrected figure below - default values for W,X, and Y SYNCR bits and resulting clock frequencies are shown in italics.



Default bit values after reset (and resulting frequencies) are shown in italics for VCO operation with a 32.768KHz crystal oscillator circuit.

Figure 4-4. Clock Block Diagram for Crystal Operation

19. Recommended XFC capacitor values

On page 4-12, second paragraph, and page 10-2, last paragraph: The XFC capacitor recommendation of 0.01µF to 0.1µF applies specifically to crystal mode operation. When using external clock with VCO mode, for frequencies > 1MHz start with a capacitance value of 10000pf/F_MHz. For example at 16.0MHz the recommended XFC capacitance is approximately 10000pf/16.0 = 625pf - choose the next higher standard value available.

For silicon revisions through 2E16G (B-suffix parts), choosing too large an XFC capacitor can result in critically damped VCO frequency rampup, which prevents proper lock detection required to exit reset. Silicon beginning with F77J (C-suffix parts) implements a revised lock detect mechanism which removes this restriction - the 0.1µF maximum XFC capacitance limit should still be observed.

20. VCO Frequency Limit

On page 4-12, last paragraph: although clearing the X bit does affect the system frequency, it has no affect the VCO frequency, since the divider controlled by X is outside the feedback loop. Changing the W or Y bits does change the VCO frequency, and the maximum VCO frequency limit should be considered when programming these bits.

21. CLKOUT and VCO Frequency Programming

On page 4-13, Table 4-2 should be replaced by the following full table of frequencies. Note that although a complete table is shown for all W:X:Y combinations, both CLKOUT and VCO frequency limits must be observed when programming the SYNCR. For example, a system operating frequency (CLKOUT) of 25.16MHz can be selected with W:X:Y=1:1:23, resulting in a VCO frequency of 50.3MHz. However, programming W:X:Y=1:0:47 to achieve the same system frequency would result in a VCO frequency of >100MHz, which is outside the spec VCO frequency operating range. Programming which violates current 25MHz electrical specs is shown in italics.

Table 4-2. System Frequencies From 32.768-kHz Reference

Y[2]	CLKOUT (kHZ)[1]		VCO (kHz)[1]	CLKOUT (kHZ)[1]		VCO (kHz)[1]
	W=0[2]		W=0[2]	W=1[2]		W=1[2]
	X=0	X=1	X=x	X=0	X=1	X=x
0	131	262	524	524	1049	2097
1	262	524	1049	1049	2097	4194
2	393	786	1573	1573	3146	6291
3	524	1049	2097	2097	4194	8389
4	655	1311	2621	2621	5243	10486
5	786	1573	3146	3146	6291	12583
6	918	1835	3670	3670	7340	14680
7	1049	2097	4194	4194	8389	16777
8	1180	2359	4719	4719	9437	18874
9	1311	2621	5243	5243	10486	20972
10	1442	2884	5767	5767	11534	23069
11	1573	3146	6291	6291	12583	25166
12	1704	3408	6816	6816	13631	27263
13	1835	3670	7340	7340	14680	29360
14	1966	3932	7864	7864	15729	31457
15	2097	4194	8389	8389	16777	33554
16	2228	4456	8913	8913	17826	35652
17	2359	4719	9437	9437	18874	37749
18	2490	4981	9961	9961	19923	39846
19	2621	5243	10486	10486	20972	41943
20	2753	5505	11010	11010	22020	44040
21	2884	5767	11534	11534	23069	46137
22	3015	6029	12059	12059	24117	48234
23	3146	6291	12583	12583	25166	50332
24	3277	6554	13107	*13107*	*26214*	*52429*
25	3408	6816	13631	*13631*	*27263*	*54526*
26	3539	7078	14156	*14156*	*28312*	*56623*
27	3670	7340	14680	*14680*	*29360*	*58720*
28	3801	7602	15204	*15204*	*30409*	*60817*
29	3932	7864	15729	*15729*	*31457*	*62915*
30	4063	8126	16253	*16253*	*32506*	*65012*
31	4194	8389	16777	*16777*	*33554*	*67109*

Y[2]	CLKOUT (kHZ)		VCO (kHz)	CLKOUT (kHZ)		VCO (kHz)
	W=0		W=0	W=1		W=1
	X=0	X=1	X=x	X=0	X=1	X=x
32	4325	8651	17302	*17302*	*34603*	*69206*
33	4456	8913	17826	*17826*	*35652*	*71303*
34	4588	9175	18350	*18350*	*36700*	*73400*
35	4719	9437	18874	*18874*	*37749*	*75497*
36	4850	9699	19399	*19399*	*38797*	*77595*
37	4981	9961	19923	*19923*	*39846*	*79692*
38	5112	10224	20447	*20447*	*40894*	*81789*
39	5243	10486	20972	*20972*	*41943*	*83886*
40	5374	10748	21496	*21496*	*42992*	*85983*
41	5505	11010	22020	*22020*	*44040*	*88080*
42	5636	11272	22544	*22544*	*45089*	*90178*
43	5767	11534	23069	*23069*	*46137*	*92275*
44	5898	11796	23593	*23593*	*47186*	*94372*
45	6029	12059	24117	*24117*	*48234*	*96469*
46	6160	12321	24642	*24642*	*49283*	*98566*
47	6291	12583	25166	*25166*	*50332*	*100663*
48	6423	12845	25690	*25690*	*51380*	*102760*
49	6554	13107	26214	*26214*	*52429*	*104858*
50	6685	13369	26739	*26739*	*53477*	*106955*
51	6816	13631	27263	*27263*	*54526*	*109052*
52	6947	13894	27787	*27787*	*55575*	*111149*
53	7078	14156	28312	*28312*	*56623*	*113246*
54	7209	14418	28836	*28836*	*57672*	*115343*
55	7340	14680	29360	*29360*	*58720*	*117441*
56	7471	14942	29884	*29884*	*59769*	*119538*
57	7602	15204	30409	*30409*	*60817*	*121635*
58	7733	15466	30933	*30933*	*61866*	*123732*
59	7864	15729	31457	*31457*	*62915*	*125829*
60	7995	15991	31982	*31982*	*63963*	*127926*
61	8126	16253	32506	*32506*	*65012*	*130023*
62	8258	16515	33030	*33030*	*66060*	*132121*
63	8389	16777	33554	*33554*	*67109*	*134218*

Note: 1. Some W/X/Y bit combinations shown may select a CLKOUT or VCO frequency higher than spec. Refer to **Section 11 Electrical Characteristics** for CLKOUT and VCO frequency limits.
2. Any change to W or Y results in a change in the VCO frequency - the VCO should be allowed time to relock if necessary.
3. Programming which violates current 25MHz electrical specs is shown in italics (any combination of W = 1 and Y > 23.

22. Additional Note for Global Chip Select

On page 4-14, last paragraph: When operating as a global chip select, CS0 does not assert for accesses to either the MBAR or to internal peripheral module registers.

23. Additional Note on PORTA/B Output Timing

Add to the External Bus Interface Operation description on page 4-15: The Port A and Port B output pins transition after the S4 falling edge for the internal write to the respective data register. This places port pin transitions at roughly the same time DS negates for the data register write - note this output delay is not currently specified in the Electrical Specifications.

24. Typo in Chip Selects

On page 4-17, first paragraph, the last sentence should reference the V-bit in the chip select base address register, not the module base address register.

25. MBAR Register Reset Values

On page 4-20, the reset values for MBAR bits 31-12 are undefined. On current silicon (2E16G) the previous value is not changed by a hardware reset.

26. MBAR AS7 Bit and IACK Cycles

On page 4-21, for the second code sequence, change the "MOVE.L #$FFFFF001,D0" to "MOVE.L #$FFFFF101,D0". This sets AS7 in the MBAR to prevent the address decode for the internal 4K register block from responding to CPU space accesses. In particular, it prevents the register block decode of $FFFFFxxx from interfering with IACK cycles (address $FFFFFFFx), and possibly corrupting the vector number returned. Normal interrupt acknowledge operation for the internal modules is not affected by this change.

27. Additional Note on VCO Overshoot

On page 4-29 place the following note under the Y-bits description:

NOTE

A VCO overshoot can occur when increasing the operating frequency by changing the Y bits in the SYNCR register. The effects of this overshoot can be controlled by following this procedure:

1. Write the X bit to zero. This will reduce the previous frequency by one half.
2. Write the Y bits to the desired frequency divided by 2.
3. After the VCO lock has occurred, write the X bit to one. This changes the clock frequency to the desired frequency.

Steps 1 and 2 may be combined.

28. Typo on Base Address 2

On page 4-30, the chip select register bits for Base Address 2 should be numbered 15-0, not 31-16.

29. SIM40 Example Code

On page 4-39 the code line "MOVE.L #MODBASE+1,D0" should read "MOVE.L #MODBASE+$101,D0" - see notes above for page 4-21. The fourth line from the bottom should read "MOVEQ #7,D0".

30. Bus Error Stack Frame

On page 5-61, in the next-to-last paragraph, delete "(the internal transfer count register is located at SP+$10 and the SSW is located at SP+12)". The stack space allocation is the same for both faults - the location of the internal count register and SSW remains the same. The only difference is that the faulted instruction program counter location SP+10 and SP+12 will contain invalid data. To tell the difference between the two stack frames, look at the first nibble of the faulted exception format vector word located at SP+$E - it will be $0 for the four-word frame, and $2 for the six-word frame.

31. DSO Timing

On page 5-71, Figure 5-23, DSO transitions one clock later than shown.

32. Typo on BDM RSREG Command

On page 5-77, Section 5.6.2.8.6, RSREG register bit #8 should be a "1".

33. IPIPE Timing

On page 5-88, Figure 5-29 shows the third IPIPE assertion low lasting for 1.5 CLKs - it actually asserts for an additional 0.5 CLKs. IPIPE transitions occur after the falling edge of CLKOUT.

34. Additional Notes on DMA Features

In the feature set listed on page 6-1, bullet five is "Operand Packing and Unpacking for Dual-Address Transfers". This packing is for transfers between different port sizes selected in the DMA channel control register, e.g. Byte <> Word transfers. The DMA controller does not do packing for byte > byte transfers, eliminating the problem of residual bytes left in the controller when a channel is stopped after an odd byte transfer count.

35. Additional Note on Cycle Steal

For the cycle steal mode description starting on the bottom of page 6-5, the initial $\overline{\text{DREQ}}$ assertion does not have to be held off until after the channel is started. If $\overline{\text{DREQ}}$ is already asserted when the channel is started by setting the channel start bit, an internal $\overline{\text{DREQ}}$ assertion is generated, providing the edge needed for the DMA cycle to start.

36. $\overline{\text{DONEx}}$ Input Assertion

On page 6-4: Beginning with the F77J mask (C-suffix parts), assertion of $\overline{\text{DONEx}}$ as an input at least one clock before the end of a DMA transfer will cause termination of the channel after that transfer. On prior mask sets (B-suffix and earlier) one more DMA transfer will typically occur.

37. Additional Note on Internal Request Generation

Add to the Internal Request Generation section on page 6-4: For internal request operation, $\overline{\text{DACK}}$ and $\overline{\text{DONE}}$ are not active as outputs during transfers. $\overline{\text{DONE}}$ is valid as an input though and will terminate channel operation if asserted - pull up if not used.

38. Additional Note on DMA Transfer Latency from $\overline{\text{DREQ}}$

Add to the External Request Generation section beginning 6-5: $\overline{\text{DREQ}}$ assertions require two clocks for input synchronization and IMB bus arbitration activity before the resulting DMA bus cycle can start. A $\overline{\text{DREQ}}$ assertion will preempt the next CPU bus cycle if it is recognized two or more clocks before the end of the current bus cycle, unless the current cycle is not the last cycle of an operand transfer, or is the read of an RMC cycle. Operand transfers and RMC read/write sequences are indivisible to guarantee data coherency - the bus cannot be arbitrated from the CPU until the complete operand transfer completes, even if operand and memory sizing results in multiple bus cycles.

For a $\overline{\text{DREQ}}$ assertion during an idle bus period, bus state S0 of the DMA bus cycle starts 2.5 clocks after the clock falling edge which $\overline{\text{DREQ}}$ is recognized on. The maximum latency from the clock falling edge that $\overline{\text{DREQ}}$ is recognized on to the falling edge that AS for the DMA cycle asserts from is shown in the following table for various memory speeds.

Table 1. DREQ Latency (Clocks) vs. Bus Width and Access Times

Access Type	Maximum $\overline{\text{DREQ}}$ Latency (Clocks)							
	16-Bit Bus Clocks/Bus Cycle				8-Bit Bus Clocks/Bus Cycle			
	2	3	4	5	2	3	4	5
Longword	7	9	11	13	11	15	19	24
RMC (TAS)	10	12	14	16	10	12	14	16

39. Additional Note on Burst Transfer $\overline{\text{DREQ}}$ Negation and Overhead

Replace the 2nd paragraph of 6.3.2.1 External Burst Mode with the following: $\overline{\text{DREQ}}$ must be negated one clock before the end of the last DMA bus cycle of a burst to prevent another DMA transfer from being generated. Also, DREQ must be negated two clocks before the end of the last DMA bus cycle to prevent an idle clock between that transfer and the following CPU access.

40. Additional Note on Cycle steal DMA arbitration overhead

Add to the External Cycle Steal Mode description on page 6-5: In general, DMA arbitration occurs transparently. However, for some 2-clock accesses using cycle steal an idle clock can follow the DMA transfer due to incomplete overlap of the DMA transfer with internal IMB arbitration. Specifically, an idle clock can follow 1) single address 2-clock transfers and 2) dual address transfers from memory to 2-clock devices. Arbitration is completely overlapped for all other cases.

41. DREQ Negation on Burst

On page 6-8, Figure 6-5, and on page 6-10, Figure 6-7, $\overline{\text{DREQ}}$x should negate before the falling edge of S2 (one clock earlier than shown) to prevent another DMA transfer from occurring. See the note above for page 6-5 on Burst Transfer $\overline{\text{DREQ}}$ Negation.

42. $\overline{\text{DREQ}}$ Assert Time

On page 6-21, Figure 6-13: The second $\overline{\text{DREQx}}$ assertion should be shown held for an additional clock to guarantee recognition on 2 consecutive clock falling edges. The figure shows it as just being 1 clock period. Note 1 should be deleted.

43. Fast Termination and Burst Request Mode

On page 6-21, delete the reference to Figure 6-14. Figure 6-14 on page 6-22 is label incorrectly - it actually shows operation with fast termination, cycle steal, and dual address transfers. Also, the second $\overline{\text{DREQx}}$ signal should be held for 2 consecutive falling edges - the figure shows it being held for only 1 clock edge. Note 1 of Figure 6-14 should be deleted.

44. Single Address Enable

6-25 SE-Single Address Enable: The note "used for intermodule DMA" should be for the SE=1 case. The 68340 does not support intermodule single address transfers, so the SE bit should always be programmed to "0".

45. Additional Note on DMA Interrupt Prioritization

Add to the Interrupt Register description on page 6-26: When both DMA channels are programmed to the same interrupt level, channel 1 is higher priority than channel 2.

46. Typo in DAPI

On page 6-28, for DAPI = 1, the DAR is incremented according to the destination size (not the source size).

47. Additional note on DMA limited rate operation

On page 6-29, in the BB-Bus Bandwith Field: The DMA "active" count increments only when the DMA channel is the bus master (each channel has its own counter). If a higher priority bus master forces the channel to relinquish the bus before completion of the active count, the counter stops until the channel regains the bus. Higher priority requests could come from 1) the other DMA channel (if it has a higher MAID level), 2) the CPU32 core (if either the interrupt mask level in the SR or the interrupt request level is higher than the DMA channel's ISM level), or 3) an external bus request. When the active count is exhausted, the DMA channel releases the bus, and the "idle" count increments regardless of bus activity.

48. Configuration Error

The description paragraph on page 6-31 for the Configuration Error should be replaced with "A configuration error results when 1) either the SAR or DAR contains an address that does not match the port size specified in the CCR, or 2) the BTC register does not match the larger port size or is zero."

49. Code Examples - Immediate Addressing Mode

On pages 6-39, 6-41, and 6-43 make the following changes (change to immediate addressing mode for source operand):

MOVE.L SARADD,DMASAR1(A0) should be MOVE.L #SARADD,DMASAR1(A0).

MOVE.L DARADD,DMADAR1(A0) should be MOVE.L #DARADD,DMADAR1(A0).

MOVE.L NUMBYTE,DMABTC1(A0) should be MOVE.L #NUMBYTE,DMABTC1(A0).

50. Serial Oscillator Problems with DMA activity

Add to the Crystal Input or External Clock (X1) section on page 7-5: A high $\overline{\text{DREQ1}}$ request rate (greater than 1MHz) with excessive undershoot on $\overline{\text{DREQ1}}$ can result in internal signal coupling to the serial module oscillator X1 pin, damping out oscillation. Avoid routing $\overline{\text{DREQ1}}$ near the serial oscillator external components, and use termination techniques such as series termination of the $\overline{\text{DREQ1}}$ driver (start with 33Ω) to limit edge rate of the signal and accompanying undershoot.

51. Additional Note on $\overline{\text{RTSx}}$ operation details

Add to the $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ descriptions on page 7-6: The RTSx outputs are active low signals - they drive a logic "0" when set, and a logic "1" when cleared.

$\overline{\text{RTSx}}$ can be set (output logic level 0) by any of the following:

- Writing a "1" to the corresponding bit in the OPSET register $71E
- Issuing an "Assert $\overline{\text{RTS}}$" command using command register CR
- If RxRTS=1, set by receiver FIFO transition from FULL to not-FULL

$\overline{\text{RTSx}}$ can be cleared (output logic level 1) by any of the following:

- Hardware reset of the serial module
- Writing a "1" to the corresponding bit in the OPRESET register $71F
- Issuing a "Negate $\overline{\text{RTS}}$" command using command register CR
- If RxRTS=1, cleared by receiver FIFO transition from not-FULL to FULL
- If TxRTS=1, cleared by completion of last character, including transmission of stop bits

52. Serial Frequency Restriction - Suffix B and Earlier

On page 7-8 , place the following notes at the end of Section 7.3.1 Baud Rate Generator:

The initial implementation of the serial module through "B" suffix parts (e.g. MC68340FE16B) restricts the minimum CLKOUT frequency at which the baud rate generators can be used to approximately 8.3MHz. Operation below this frequency results in a synchronized internal clock which is at a lower frequency than the X1 input, which then results in incorrect baud rates. One method to extend the minimum CLKOUT frequency is to reduce the X1 frequency by powers of 2 as shown in the table below. The corresponding baud rates selected by the clock select register programming are scaled by the same factor. This method preserves most of the standard baud rates (19200, 9600, 4800, etc.).

Serial XTAL Frequency	CLKOUT F_{min}	Max AvailableBaud Rate
3.6864MHz	8.29MHz	76.8k
1.8432	4.15	38.4k
0.9216	2.07	19.2k

CLKOUT min = 2.25*XTAL frequency

Alternatively, the baud rate clock can be supplied directly through the SCLK input. Since there is a single

SCLK input, both serial channels must use the same baud rate clock, although one could be clocked in the 1x mode and the other in the 16x mode. When using this method, the X1 input can be tied to ground - no crystal is required.

53. Serial Frequency Restriction - Suffix C and Later

Beginning with "C" suffix 68340 production material, the serial module internal clock synchronization has been revised to relax CLKOUT minimum frequency requirements when using the internal baud rate generators. The revised CLKOUT requirements are a relaxation of the current specifications - no change to existing designs will be required to accommodate this feature. Specifications shown here are preliminary, and subject to change without notice.

Previously, a minimum 8.3MHz CLKOUT frequency was required to use the internal baud rate generators with the default 3.6864MHz serial crystal. In the new serial module, the serial clock synchronization has been modified to allow the minimum CLKOUT frequency to be scaled depending on the maximum baud rate selected. Operation and specifications for external clocking via SCLK are not affected by this change.

The table below shows the resulting minimum CLKOUT frequency for each programmable baud rate. Note that applications using the VCO clock modes - crystal and external clock with VCO - are restricted to a 131KHz minimum CLKOUT frequency. An errata exists which also limits CLKOUT to 100KHz for external clock without VCO mode; refer to the silicon errata.

Minimum CLKOUT Frequency vs. Baud Rate

baud rate	**CLKOUT** F_{min}	**baud** rate	**CLKOUT** F_{min}
50	3250Hz*	1800	116kHz*
75	4850Hz*	2000	129kHz*
110	7090Hz*	2400	154kHz
134.5	8660Hz*	4800	309kHz
150	9650Hz*	7200	465kHz
200	12.9kHz*	9600	621kHz
300	19.3kHz*	19200	1.26MHz
600	38.5kHz*	38400	2.56MHz
1050	67.3kHz*	76800	8.29MHz
1200	76.9kHz*		

*Note: See text for other minimum system frequency considerations

The minimum CLKOUT frequency is calculated using the formula:

$$CLKOUT(min) = 1/((1/(baud\_rate*sample\_rate)-T_{setup}-T_{hold})/2)$$

where Sample_rate = 48 for 76.8Kbaud and 32 for others, and $T_{setup}+T_{hold}$ = 30ns

$$CLKOUT(min) = 1/((1/(baud\_rate*32)-30ns)/2)(50\text{-}38400\ baud)$$

$$1/((1/(baud\_rate*48)-30ns)/2)(76.8K\ baud)$$

Note that with this revision, replacing the serial crystal with a lower subfrequency (1.8432MHz for example) no longer affects the minimum CLKOUT frequency for a specific baud rate, since the selected baud clock is now synchronized. Also, the logic for the CTSx inputs uses the 1200baud clock as a sample clock - CLKOUT Fmin should be kept above 76.9KHz to avoid affecting CTSx sampling.

54. 68340 RTS Difference from 68681

Add to the description for receiver-controlled RTS operation in the next-to-last paragraph on page 7-13: Unlike the 68681, the RTSx signal does not have to be manually asserted the first time in the mode to support control-flow capability on the receiver.

55. Additional Note on Serial multidrop operation

Add to the Multidrop Mode section beginning on page 7-15: For multidrop mode, it is not necessary to disable the transmitter to manipulate the A/D bit, as generally implied in the manual, nor is it necessary to wait until the previous character completes transmission (i.e. TxEMP). The serial module logic latches this bit and appends it to the data character when the character is transferred from the transmit buffer to the serial output shift register. Once this transfer occurs (as indicated by the TxRDY assertion), the A/D bit in MR1 can be changed without affecting the character in progress. The proper programming sequence to change the A/D bit for the next character would be:

1.) poll TxRDY until asserted (or interrupt on TxRDY)
2.) set/clear A/D bit in MR1 for new character
3.) write character to transmit buffer (TB)
4.) A/D bit can be changed only after $\overline{\text{TxRDY}}$ asserts again

No other bits in MR1 should be modified when changing the A/D bit.

56. Typo in Timer Registers

On page 8-17, last paragraph, the sentence "The ADDR column indicates the offset of the register from the base address of the timer." should be changed to "The ADDR column indicates the offset of the register from the SIM40 base address." The offset is not from the base address of the timers.

57. Typo in CPE Description

The CPE bit header on page 8-21 should be "Counter/Prescaler Enable".

58. Typo in Status Register Configuration

On page 8-27, Section 8.5.1, the Status Register (SR) description should say: "• Clear the TO, TG, and TC bits to reset the interrupts."

59. Typos in Timer Initialization Examples

On pages 8-28 and starting 8-29, the Timer1 register offsets should be from the timer base address, not from the SIM40 base address. The correct equates for the Timer1 register offsets are:

* Timer1 register offsets from timer1 base address

```
IR1       EQU     $4      interrupt register timer1
CR1       EQU     $6      control register timer1
SR1       EQU     $8      status register timer1
CNTR1     EQU     $A      counter register timer1
PRLD11    EQU     $C      preload register 1 timer1
COM1      EQU     $10     compare register timer1
```

On page 8-28, change the last code line from "CLR.W SR1(A0)" to "ORI.W #$7000,SR1(A0)". The TO, TG, and TC interrupt status bits are cleared by writing a "1" to the corresponding bit, allowing individual bits to be cleared without affecting the other bits.

On page 8-29, 7th line down, change "MOVE.W #$020F,IR1(A0)" to "MOVE.W #$0274,IR1(A0)". Change the comment line above from vector $0F to $74. This change switches the interrupt vector from the Uninitialized vector to a user defined vector.

60. Additional Note on Oscillator Layout Guidelines

Add to the Processor Clock Circuitry (page 10-1) and Serial Interface (page 10-4) sections: In general, use short connections and place external oscillator components close to the processor. Do not route other signals through or near the oscillator circuit, especially high frequency signals like CLKOUT, $\overline{AS}$, and $\overline{DREQ1}$ (see notes on $\overline{DREQ1}$ and serial oscillator for p.7-15). Place a ground shield around the oscillator logic; use a separate trace for ground to the oscillator so that it does not carry any of the digital switching noise.

61. Recommended 32KHz Oscillator Circuit

On page 10-2, Figure 10-2, the component values shown in the example 32KHz oscillator circuit may not provide enough loop gain for all crystals. For a more generally robust oscillator circuit, change C1 and C2 as shown below. A 10M resistor can be substituted for the 20M R2 bias resistor as shown.

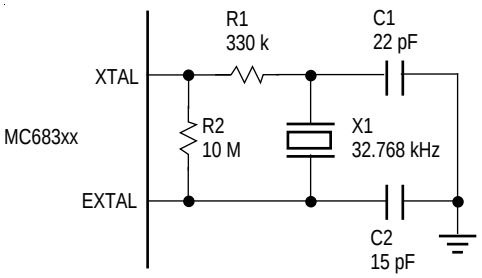


Figure 10-2. Sample Crystal Circuit

62. Additional Notes on Power-On Reset

Replace Section 10.1.2 Reset Circuitry on page 10-3 with the following paragraphs:

A power-on reset (POR) is generated by the SIM module when it detects a positive going V_{CC} transition—the V_{CC} threshold is typically in the range 2.0–2.7V, and varies depending on processing and environmental variables. Hysteresis is included in the reset circuit to prevent reassertion for a monotonically increasing V_{CC} voltage; however, excessively long V_{CC} rise times (>100 ms) may allow the reset logic to release

RESET before V_{CC} has stabilized. The reset thresholds provided in the SIM should not be relied upon to monitor V_{CC}, since internal logic may fail at voltages between spec V_{CCmin} and the reset trigger threshold. An external low voltage monitor circuit, such as the MC34064, should be used instead.

When the processor is used in crystal clock mode, the simplest external reset logic consists of simply a 1K pullup resistor from RESET to V_{CC}. This solution relies on a monotonically increasing V_{CC} that has a rise time on the order of 100ms or less - the actual allowable rise time is dependent on the startup time of the 32.768kHz oscillator circuit. As noted above, this does not provide rigorous V_{CC} monitoring, and may be susceptible to sags or glitches in the V_{CC} supply voltage.

In external clock mode, either with or without the PLL, the POR time delay of 328 * T_{clkin} does not provide adequate time for V_{CC} to stabilize before allowing reset to negate. Applications using these two clocking modes should include an external reset circuit which generates an appropriate delay for the power source being used, as well as a voltage monitor if needed. Note that beginning with 1F77J silicon (C-suffix parts) the delay for external clock with VCO mode has changed from 328 clocks to 1864 clocks; an external reset circuit is still recommended.

63. SRAM Interface

The SRAM interface shown in Figure 10-5, page 10-3 is incorrect - see the corrected drawing below.

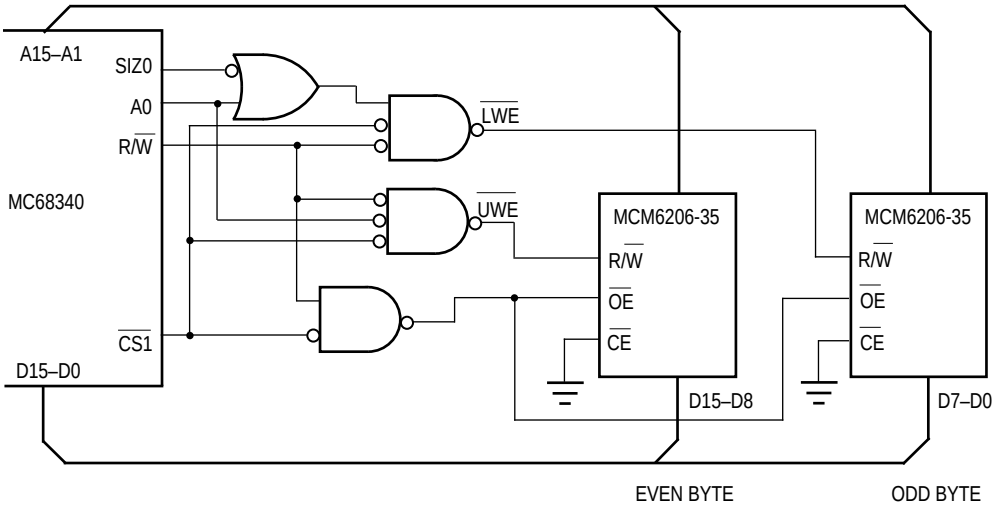


Figure 10-3. SRAM Interface

64. Additional Notes on ROM Interface

10-4 Figure 10-6 ROM interface: Connect $\overline{OE}$ to $\overline{CS0}$ and $\overline{CE}$ to ground to maximize available access time (at the expense of power consumption). Alternatively, connect $\overline{OE}$ and $\overline{CE}$ to $\overline{CS0}$ to deselect the EPROM between accesses and lower power consumption.

65. Corrections to 8/16-Bit DMA Control Logic

On page 10-10, the logic driving $\overline{OE}$ on the 74F245 in Figure 10-14 should be corrected as shown below. Although not detailed, the byte enables for the memory block should be controlled during reads to prevent contention between the upper and lower bytes of the data bus when D7-D0 is muxed to the upper data byte.

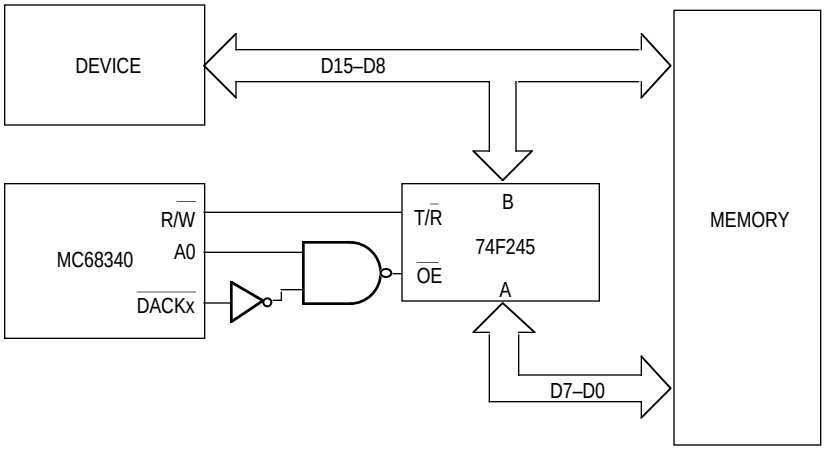


Figure 10-14. Circuit For Interfacing 8-Bit Device to 16-Bit Memory in Single-Address DMA Mode

66. Thermal Characteristics

On page 11-1,θ_{JA} for PGA package should be changed from 27° C/W (estimated) to 30° C/W (spec). θ_{JA} for the 144-pin TQFP (PV) package is 49°C/W

67. Clock VIH

11-5 DC Electrical Specifications: The Clock Input High Voltage spec applies to both the EXTAL and X1 inputs.

68. Input Clock Duty Cycle in External Clock w/PLL mode

On page 11-6, Note 7 at the bottom: The input clock 20/80% duty cycle for external clock with PLL mode can be used when the VCO is not turned off during LPSTOP. During LPSTOP with the VCO turned off, the input clock is used for clocking the SIM, and must meet the tighter duty cycle requirements outlined in Note 6.

69. Typos on Clock Skew Notes

11-7 Note 11: Delete the second sentence "Clock skew is measured from the rising edges of the clock signals". The clock skew is 10-40ns between corresponding rising or falling edges of EXTAL and CLKOUT.

Note 12: The last sentence should say "Clock skew is measured from the falling edges of the clock signals". The PLL phase locks the falling edge of CLKOUT to the falling edge on EXTAL.

69. Bus Arbitration Notes

On page 11-15, Figure 11-6, specification #47A should be measured to the falling edge of S4. The figure incorrectly shows it measured to the rising edge of S5, one-half clock later.

70. Standard MC68340 Ordering Information

Update table 12.1 as shown below.

Supply Voltage	Package Type	Frequency (MHz)	Temperature	Order Number
5.0 V	Ceramic Quad Flat Pack FE Suffix	0 – 16.78 0 – 16.78 0 – 25	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340FE16 MC68340CFE16 MC68340FE25
5.0 V	Plastic Pin Grid Array RP Suffix	0 – 16.78 0 – 16.78 0 – 25	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340RP16 MC68340CRP16 MC68340RP25
5.0 V	Thin Quad Flat Pack PV Suffix	0 – 16.78 0 – 8.39	0° C to 70° C 0° C to 70° C	MC68340PV16 MC68340PV25
3.3 V	Thin Quad Flat Pack PV Suffix	0 – 16.78 0 – 8.39	0° C to 70° C 0° C to 70° C	MC68340PV16V MC68340PV8V
3.3 V	Ceramic Quad Flat Pack FE Suffix	0 – 8.39 0 – 8.39 0 – 16.78	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340FE8V MC68340CFE8V MC68340FE16V
3.3 V	Plastic Pin Grid Array RP Suffix	0 – 8.39 0 – 8.39 0 – 16.78	0° C to +70° C -40° C to +85° C 0° C to 70° C	MC68340RP8V MC68340CRP8V MC68340RP16V

71. TxRDY/RxRDY Pin Swap

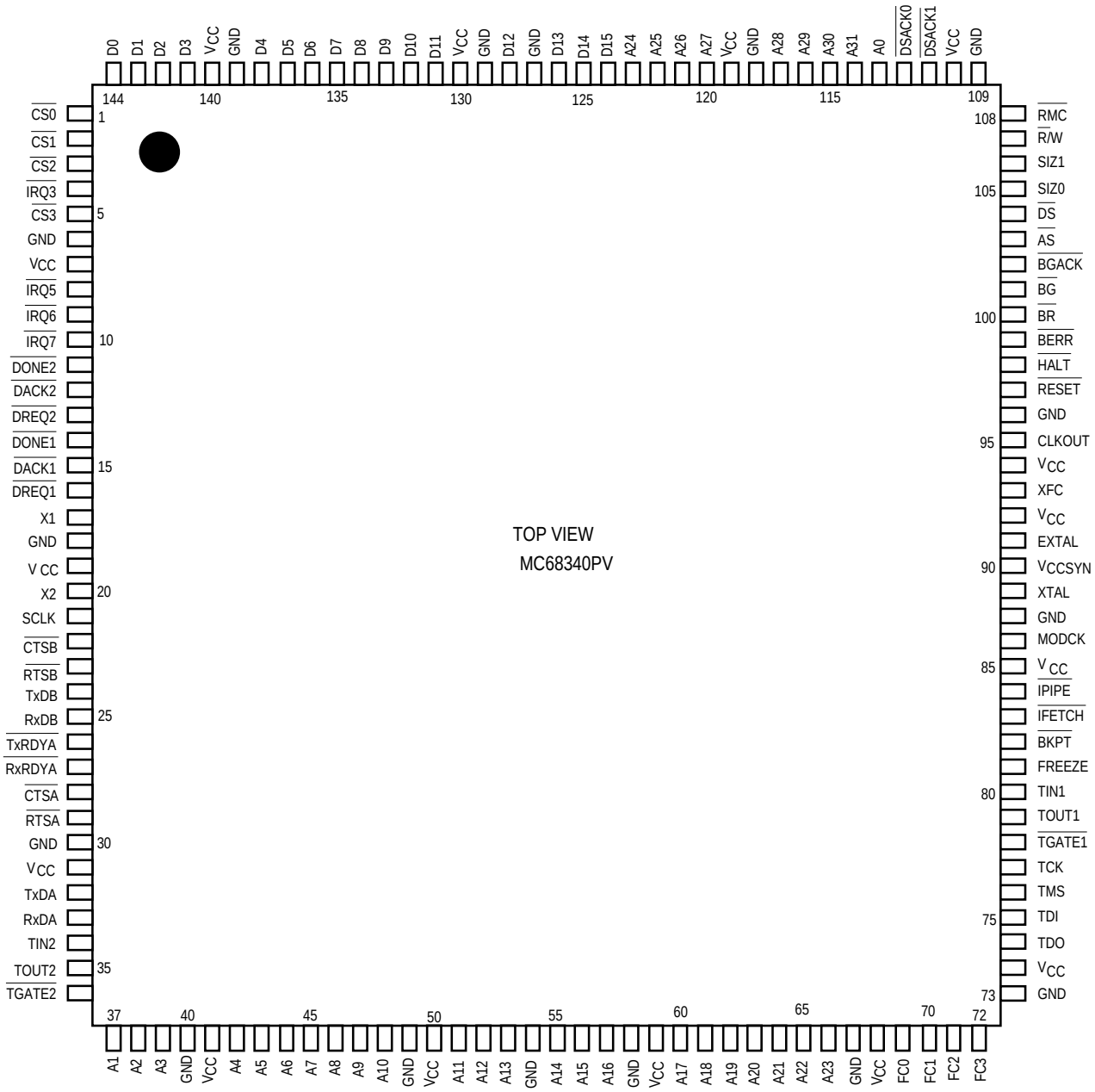
Add to the Pin Assignment section beginning page 12-2: Early documentation for the 68340, including the MC68340UM/AD Rev. 0 User's Manual, showed TxRDY and RxRDY swapped. The MC68340UM Rev. 1 documentation correctly shows the pinout of the CQFP with RxRDY on pin 82 and TxRDY on pin 83, and the PPGA package with RxRDY on pin B5 and TxRDY on pin A4.

72. TQFP pinout and case outline

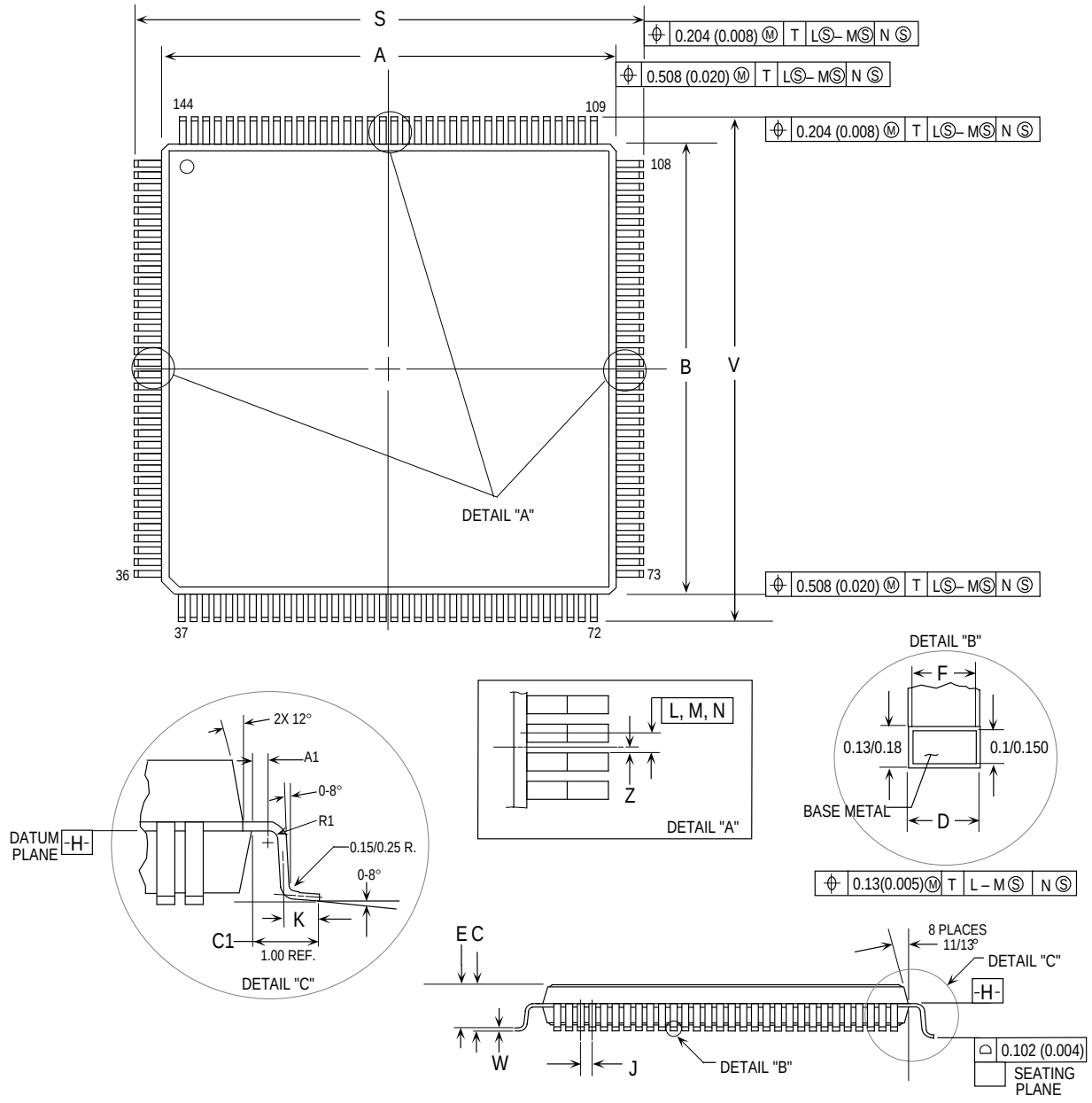
Note, the TQFP package pinout is a mirror image of the CQFP package (die is flipped). Pinout and mechanical information for the TQFP package are shown on the following pages.

Pin Assignments

144-Lead Thin QUAD Flat Pack (PV Suffix).



PACKAGE DIMENSIONS
PV SUFFIX
CASE 918-01



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.900	20.100	0.783	0.791
B	19.900	20.100	0.783	0.791
C	1.400	1.600	0.056	0.062
D	0.170	0.280	0.0067	0.0110
E	1.350	1.450	0.054	0.057
F	0.160	0.270	0.063	0.011
G	20.00 BSC.		0.197 BSC.	
K	0.450	0.750	0.018	0.029
S	21.900	22.100	0.863	0.870
V	21.900	22.100	0.863	0.870
W	0.050	0.150	0.002	0.006
Z	0.250 BSC.		0.250 BSC.	
A1	0.100	—	0.004	—
C1	1.000 REF		0.039 REF	
R1	1.050 REF		0.006 REF	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE **-H-** IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS **-L-**, **-M-**, AND **-N-** TO BE DETERMINED AT DATUM PLANE **-H-**.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE **-T-**.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE **-H-**.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

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