AK4350

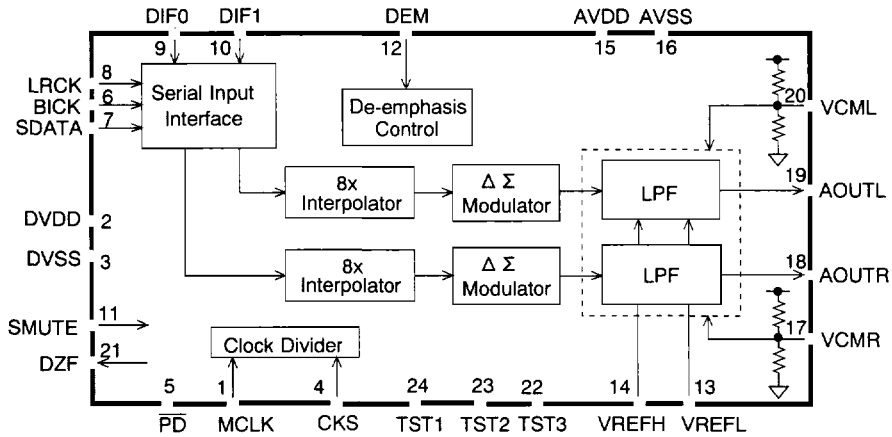
2V & Low Power Multi-bit △ Σ DAC

GENERAL DESCRIPTION

The AK4350 is a 18 bit low voltage & power stereo DAC for digital audio system. The AK4350 uses the new developed Multi-bit △ Σ architecture, this new architecture achieves DR=92dB at low voltage operation. The AK4350 includes post filter with single-ended output and does not need any external parts. THe AK4350 is suitable for the portable audio system like MD, etc as low power and small package.

FEATURES

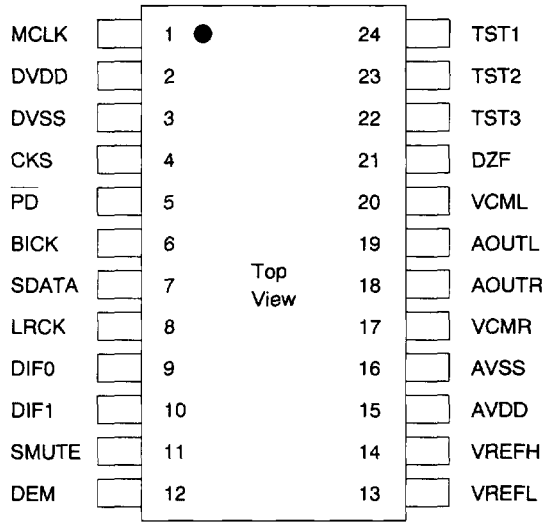
- ☐ Multi-bit △ Σ DAC
- ☐ Sampling Rage : 8kHz ~ 50kHz
- ☐ On chip post filter
- ☐ On chip Buffer with Single End Output
- ☐ On chip Perfect filtering 8 times FIR Interpolator
  - Passband : 20kHz
  - Passband Ripple : ± 0.06dB
  - Stopband Attenuation : 43dB
- ☐ Digital De-emphasis : 44.1kHz
- ☐ Soft Mute
- ☐ Master Clock : 256fs/384fs
- ☐ THD+N : -85dB
- ☐ DR : 92dB
- ☐ Low Voltage Operation : 2V
- ☐ Low Power Dissipation : 7.4mW(@2V)
- ☐ Small Package : 24pin VSOP



■ Ordering Guide

AK4350-VF	-10 ~ +70 ℃	24pin VSOP(0.65mm Pitch)
AKD4350	Evaluation Board	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	FUNCTION
1	MCLK	I	Master Clock Pin
2	DVDD	-	Digital Power Supply Pin
3	DVSS	-	Digital Ground Pin
4	CKS	I	Master Clock select Pin "L": 256fs "H": 384fs
5	PD	I	Power-Down Pin When at "L", the AK4350 is in power-down mode and is held in reset. The AK4350 should always be reset upon power-up.
6	BICK	I	Serial Bit Input Clock Pin This clock is used to latch audio data.
7	SDATA	I	Audio Data Input Pin
8	LRCK	I	L/R Clock Pin This input determines which audio channel is currently being input on SDATA pin.
9 10	DIF0 DIF1	I I	Digital Input Format Pins These pins select one of four input modes.
11	SMUTE	I	Soft Mute Pin When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
12	DEM	I	De-emphasis Enable Pin When this pin goes "H", de-emphasis(fs=44.1kHz) is enabled.
13	VREFL	I	"L" Reference Voltage Input Pin Normally connected to AVSS.
14	VREFH	I	"H" Reference Voltage Input Pin Normally connected to AVDD.
15	AVDD	-	Analog Power Supply Pin
16	AVSS	-	Analog Ground Pin
17	VCMR	O	Rch Common Voltage Pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.
18	AOUTR	O	Rch Analog Output Pin
19	AOUTL	O	Lch Analog Output Pin
20	VCML	O	Lch Common Voltage Pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.
21	DZF	O	Zero Input detect pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".
22	TST3	O	Test Pin
23	TST2	O	Test Pin
24	TST1	I	Test Pin (Pull-down Pin)

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies: Analog	(AVDD pin)	AVDD	-0.3	6.0	V
Digital	(DVDD pin)	DVDD	-0.3	AVDD+0.3 or 6.0	V
Input Current, Any Pin Except Supplies		IIN	-	± 10	mA
Input Voltage		VIND	-0.3	AVDD+0.3 or 6.0	V
Ambient Operating Temperature		Ta	-10	70	℃
Storage Temperature		Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS,DVSS=0V; Note1)

Parameter		Symbol	min	typ	max	Units
Power Supplies: Analog	(AVDD pin)	AVDD	1.8	2.0	3.3	V
Digital	(DVDD pin)	DVDD	1.8	2.0	AVDD	V
Voltage Reference	(Note 2)	VREFH		-	AVDD	V
		VREFL	AVSS	-		

Note: 1. All voltages with respect to ground.
2. Analog output voltage scales with the voltage of (VREFH - VREFL).
AOUT(typ.@0dB)= 0.96Vpp * (VREFH - VREFL) / 2

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=2.0V, VREFH=AVDD, VREFL=AVSS, fs=44.1kHz; Signal Frequency=1kHz; Measurement Bandwidth=10Hz ~ 20kHz; $R_L \geqq 10k\ \Omega$; unless otherwise specified)

Parameter	min	typ	max	Units
Dynamic Characteristics (Note 3)				
THD+N		-85	-79	dB
Dynamic Range (A-weight)	88	92		dB
S/N (A-weight)	88	92		dB
Interchannel Isolation	90	100		dB
DC Accuracy				
Interchannel Gain Mismatch		0.1	0.3	dB
Gain Drift		60		ppm/ ℃
Analog Output				
Output Voltage (Note 4)	0.90	0.96	1.02	Vpp
Load Resistance	10			k Ω
Power Supplies				
Power Supply Current				
Normal Operation ($\overline{PD}$="H")				
AVDD + DVDD		3.7	5.4	mA
Power-Down-Mode ($\overline{PD}$="L")				
AVDD + DVDD (Note 5)		10	50	uA
Power Dissipation (AVDD+DVDD)				
Normal Operation		7.4	10.8	mW
Power-Down-Mode (Note 5)		20	100	uW
Power Supply Rejection	-	50	-	dB

Note 3. Measured by AD725C(Shibasoku). Averaging mode.
In case of AVDD=DVDD=3.0V,
THD+N: -92dB
DR: 94dB (A-weight)
S/N: 95dB(A-weight)

4. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFH - VREFL).
AOUT(typ.@0dB) = 0.96Vpp * (VREFH - VREFL) / 2。
5. In case of power-down-mode, all digital input pins including clock pins (MCLK, BICK, LRCK) are held DVDD or DGND.

FILTER CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=1.8 ~ 3.3V; fs=44.1kHz)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband	-0.1dB (Note 6)	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband	(Note 6)	SB	24.1			kHz
Passband Ripple		PR			± 0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay	(Note 7)	GD	-	14.7	-	1/fs
Digital Filter + Analog Filter						
Frequency Response	0 ~ 20.0kHz		-	± 0.2	-	dB

Note: 6. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@-0.1dB), SB=0.546*fs(@-43dB).

7. The calculating delay time which occurred by digital filtering. This time is from setting the 16bit data of both channels to input resistor to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=2.7 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
High-Level Output Voltage	Iout=-20uA	VOH	DVDD-0.1	-	-	V
Low-Level Output Voltage	Iout=20uA	VOL	-	-	0.1	V
Input Leakage Current	(Note 8)	Iin	-	-	± 10	uA

Note: 8. TST1 pin has internal pull-down devices.

SWITCHING CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=1.8 ~ 3.3V; CL=20pF)

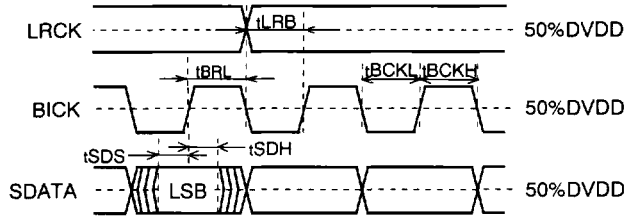
Parameter		Symbol	min	typ	max	Unit
Master Clock Frequency						
External Clock 256fs:		fCLK	2.048	11.2896	12.8	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
External Clock 384fs:		fCLK	3.072	16.9344	19.2	MHz
	Pulse Width Low	tCLKL	23			ns
	Pulse Width High	tCLKH	23			ns
LRCK Frequency		fs	8	44.1	50	kHz
Audio Interface Timing (Note 9)						
BICK Period		tBCK	312.5			ns
BICK Pulse Width Low		tBCKL	100			ns
Pulse Width High		tBCKH	100			ns
LRCK Edge to BICK rising (Note 10)		tLRB	50			ns
BICK rising to LRCK Edge (Note 10)		tBRL	50			ns
SDATA Setup Time		tSDS	50			ns
SDATA Hold Time		tSDH	50			ns
Reset Timing						
$\overline{PD}$ Pulse Width (Note 11)		tRST	300			ns

Notes 9. Refer to the operating overview section "Audio Data Interface".

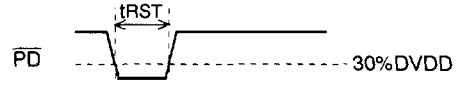
10. BICK rising edge must not occur at the same time as LRCK edge.

11. The AK4350 can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

■ Timing Diagram



Audio Data Input Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4350 are MCLK(256fs/384fs), LRCK (fs), BICK(32fs ~). The master clock(MCLK) should be synchronized with LRCK but the phase is free of care. The frequency of MCLK is determined by the sampling rate(LRCK), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an MCLK frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK4350.

All external clocks (MCLK, BICK, LRCK) should always be present whenever the AK4350 is in normal operation mode ($\overline{PD}$="H"). If these clocks are nor provded, the AK4350 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4350 should be in the power-down mode ($\overline{PD}$="H").

As the AK4350 includes the phase detection circuit for LRCK, the AK4350 adjusts the phase of LRCK automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

LRCK (fs)	MCLK		BICK(64fs)
	CKS="L"; 256fs	CKS="H"; 384fs	
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz

Table 1. Examples of System Clock

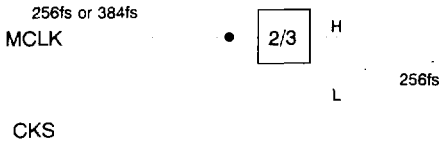


Figure 1. Internal Clock Circuit

■ Serial Data Interface

The AK4350 interfaces with external system by using SDATA, BICK and LRCK pins. Four types of data format are available and one of them is selected by setting DIF0 and DIF1. Format 0 is compatible with existing 16bit DACs and digital filters. Format 1 is an 18bit version of format 0. Format 2 is similar to AKM ADCs(except AK5326/7/8/9) and many DSP serial ports. Format 3 is compatible with the I ² S serial data protocol. In formats 2 and 3, 16bit data followed by two zeros also could be input. In all modes, the serial data is MSB-first and 2's complement format.

DIF1	DIF0	MODE	BICK	Figure
0	0	0: 16bit, LSB justified	≧ 32fs	Figure 2
0	1	1: 18bit, LSB justified	≧ 36fs	Figure 2
1	0	2: 18bit,MSB justified	≧ 36fs	Figure 3
1	1	3: I ² S compatible	≧ 32fs or ≧ 36fs	Figure 4

Table 1. Digital Input Formats

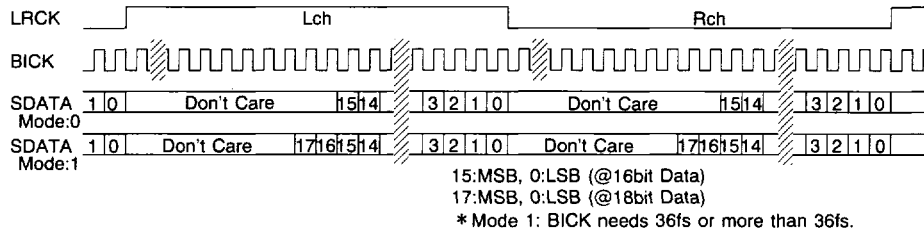


Figure 2. Mode 0,1 Timing

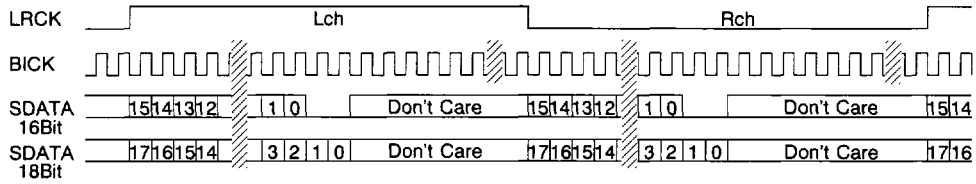


Figure 3. Mode 2 Timing

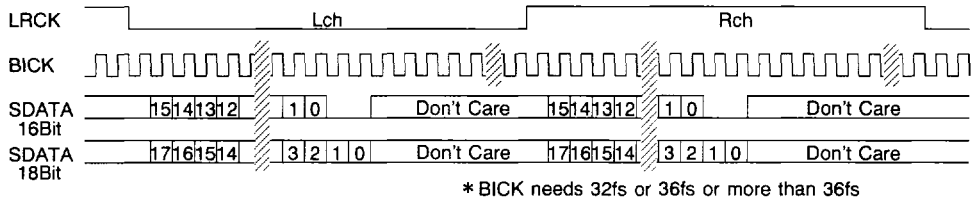


Figure 4. Mode 3 Timing

■ De-emphasis Filter

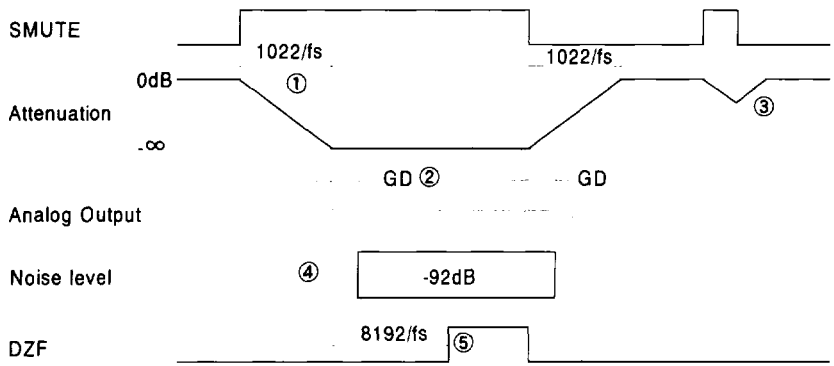
The AK4350 includes the digital de-emphasis filter (tc=50/15us) by IIR filter. This filter corresponds to a sampling frequency of 44.1kHz. The de-emphasis is enabled by setting DEM pin "H".

■ Zero detection

When the input data at both channels are continuously zeors for 8192 LRCK cycles or when the muting period exceeds 8192 + 1022 = 9214 LRCK cycles, DZF goes to "H". DZF goes "L" immediately after non zero data is input or soft mute is released.

■ Soft mute operation

When SMUTE goes to "H", the output signal is attenuated by - ∞ during 1022 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1022 LRCK cycles. If the soft mute is cancelled within 1022 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

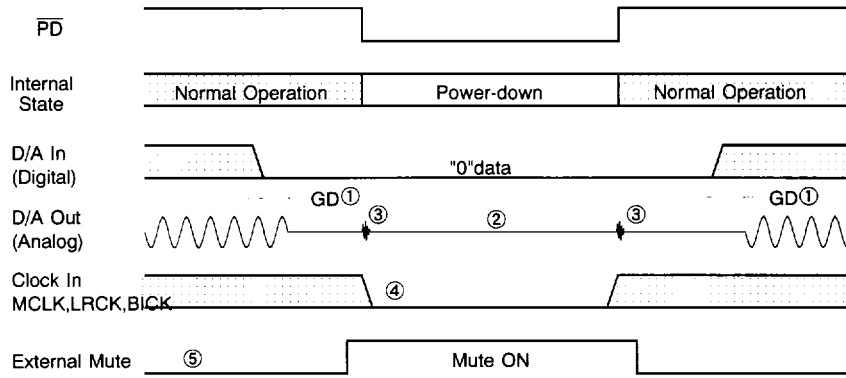


① The output signal is attenuated by - ∞ during 1022 LRCK cycles (1022/fs)
② Analog output corresponding to digital input have the group delay (GD).
③ If the soft mute is cancelled within 1022 LRCK cycles, the attenuation is discontinued and returned to 0dB.
④ The noise level on analog output is about 92dB in audio band(20kHz).
⑤ When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes to "L" if input data are not zero after DZF "H".

Figure 5. Soft mute operation

■ Power-Down

The AK4350 is placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.



① Analog output corresponding to digital input have the group delay (GD).
② Analog outputs are floating (Hi-Z) at the power-down mode.
③ Click noise occurs at the edges (" ↓ ↑ ") of $\overline{PD}$ signal.
④ When the external clocks(MCLK, BICK, LRCK) are stopped, the AK4350 should be in the power-down mode.
⑤ Please mute the analog output externally if the click noise (③) influences system application. The timing example is shown in this figure.

Figure 6. Power-down/up sequence example

■ System Reset

The AK4350 should be reset once by bringing $\overline{PD}$ pin "L" upon power-up. The internal timing starts clocking by LRCK " ↑ " upon exiting reset.

SYSTEM DESIGN

Figure 7 shows the system connection diagram. An evaluation board [AKD4350] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

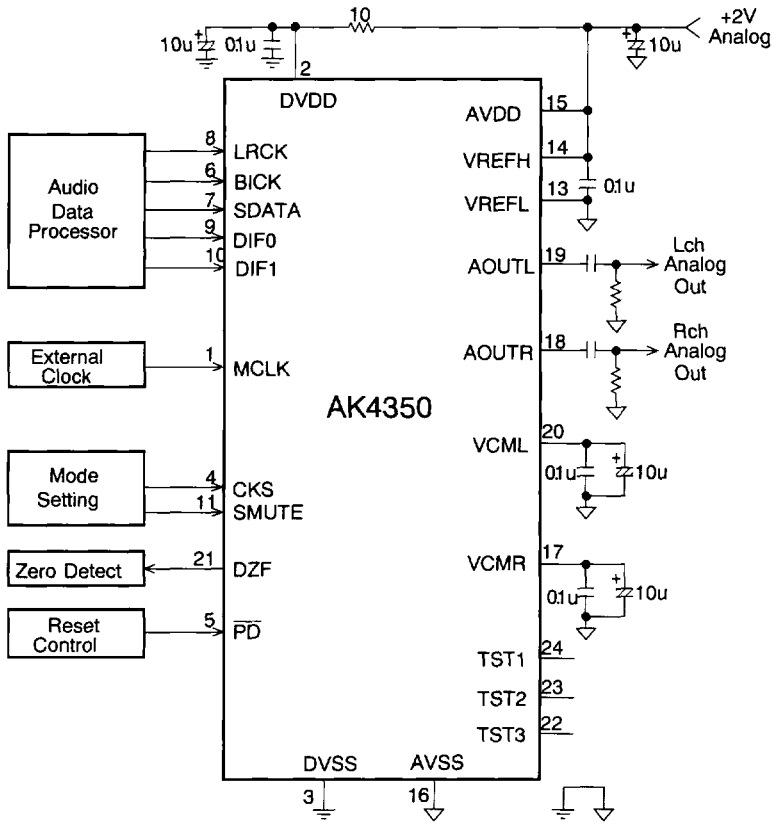


Figure 7. Typical Connection Diagram

NOTE:

- LRCK=fs, BICK ≧ 32fs or 36fs, MCLK=256fs/384fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. Figure 7 shows the power supply connection example. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10 Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.
Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be as near to the AK4350 device as possible, with the low value ceramic capacitor between VREFH and VREFL being the nearest.

2. Voltage Reference

The differential voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is connected to AVSS. An electrolystic capacitor 10uF parallel with a 0.1uF ceramic capacitor are attached between VREFH and VREFL pins. VCML and VCMR pins are a signal ground of this chip. An electrolystic capacitor less than 10uF parallel with a 0.1uF ceramic capacitor attached between VCML, VCMR pins and AVSS eliminates the effects of high frequency noise. Especially, the ceramic capacitor should be connected to these pins as near as possible.
No load current may be drawn from VCML and VCMR pins. All signals, especially clocks, should be kept away from the VREFH, VREFL, VCML and VCMR pins in order to avoid unwanted coupling into the AK4350.

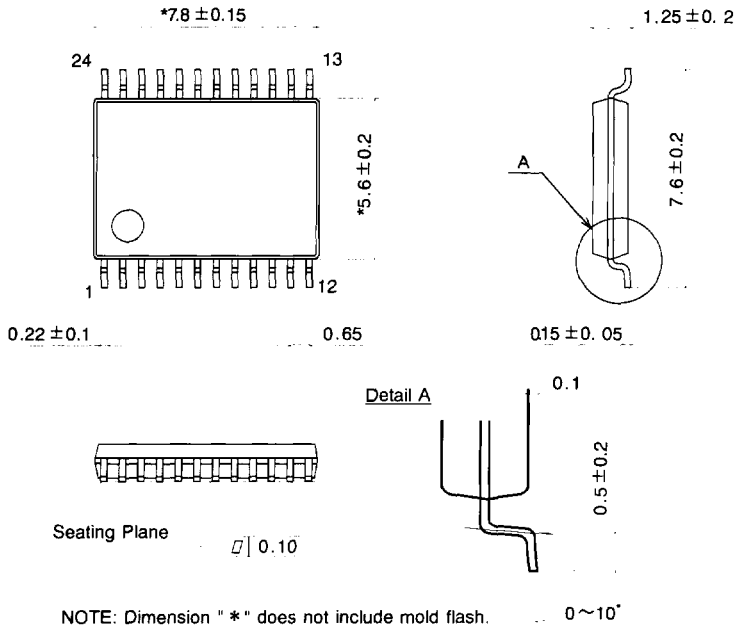
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCML, VCMR voltage. The output signal range is typically 0.96Vpp. If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required. The output voltage is a positive full scale for 7FFFH and a negative full scale for 8000H. The ideal output is the VCML, VCMR voltage for 0000H.

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of a few mV + VCOM voltage.

PACKAGE

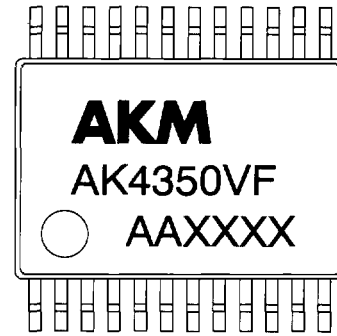
● 24pin VSOP (Unit: mm)



■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



Contents of AAXXXX
AA : Lot #
XXXX : Date Code