

Spartan-3A DSP Starter Board

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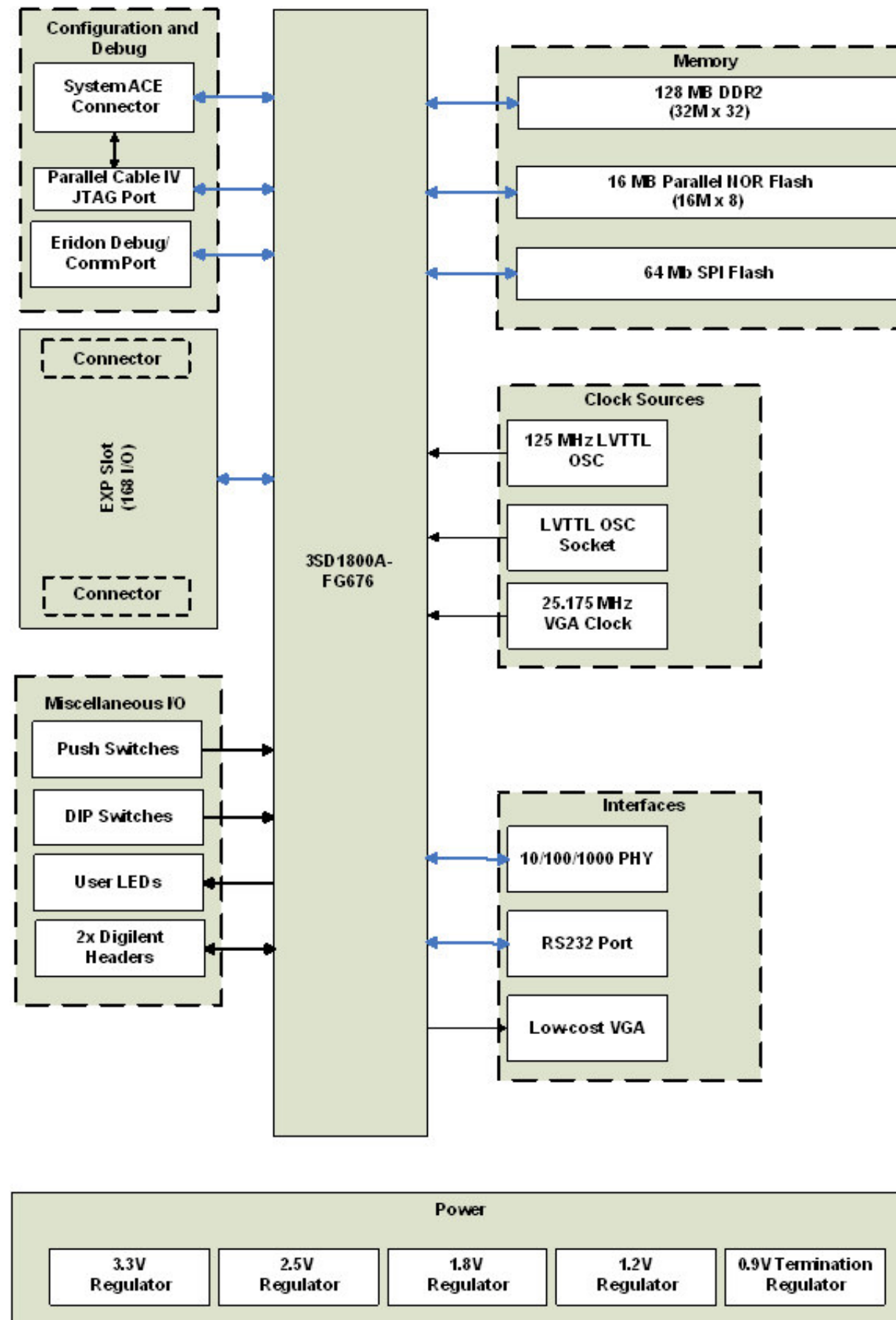
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07/11/08

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Title	Spartan-3A DSP Starter Board	Sheet 1 - Lead Sheet
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B	0381257	1
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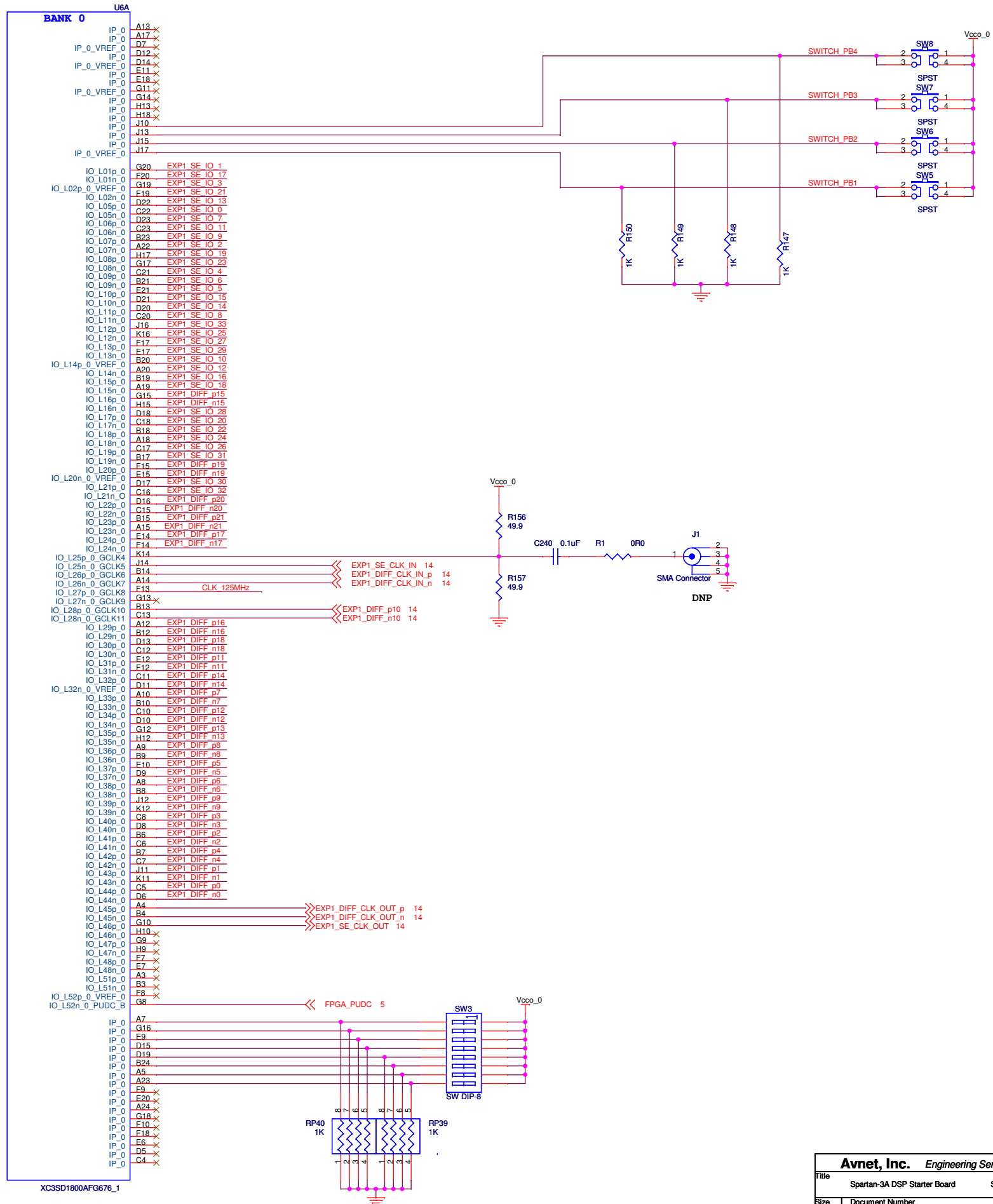
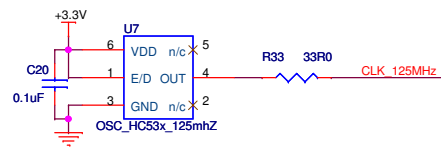


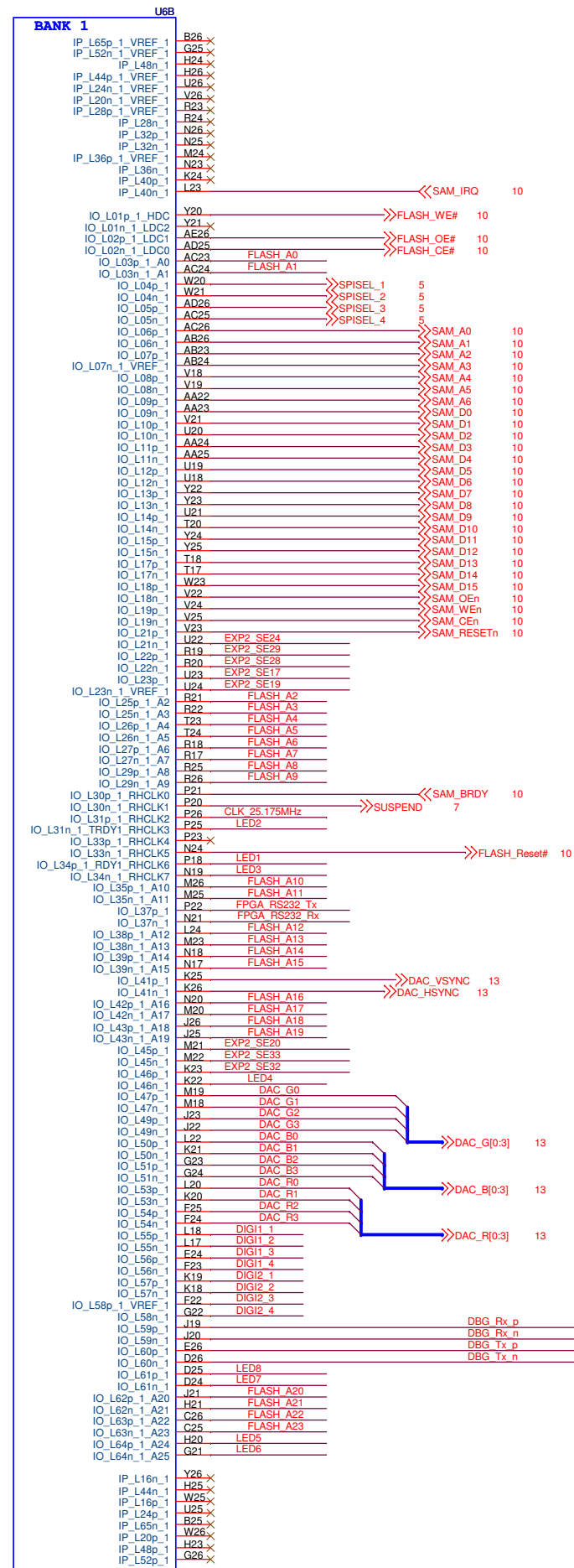
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14 EXP1_SE_IO_[0:33] <<

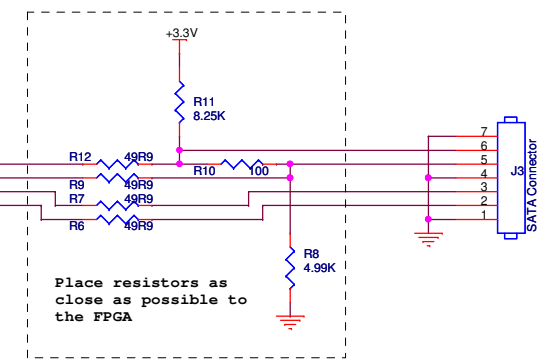
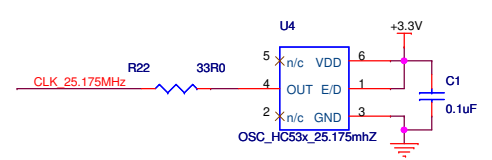
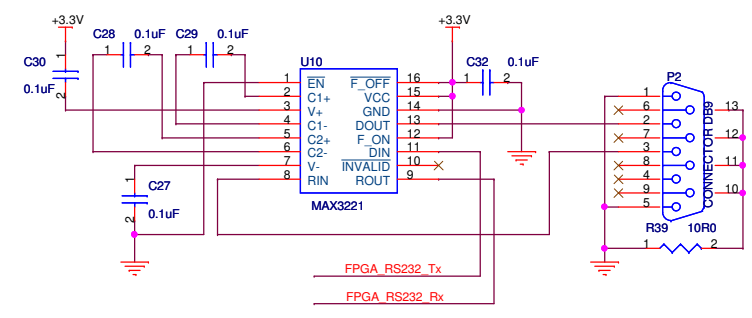
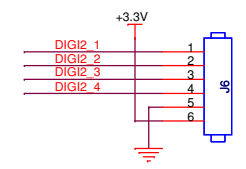
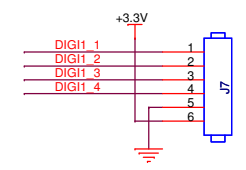
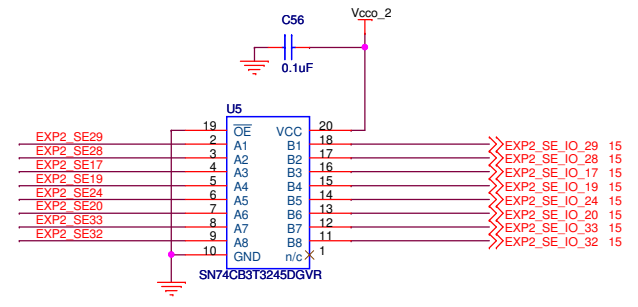
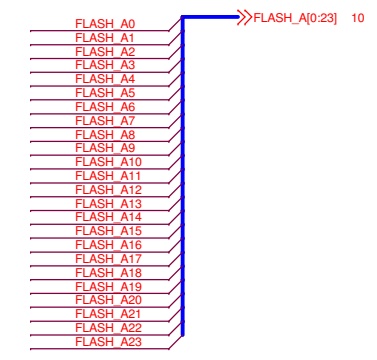
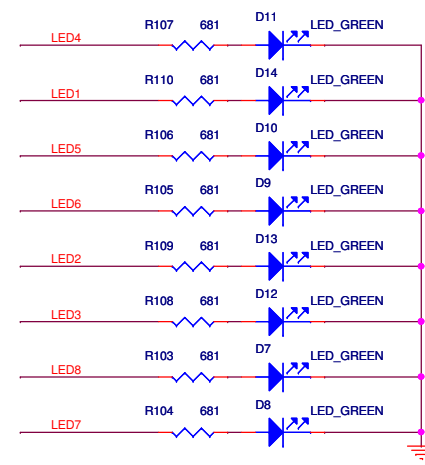
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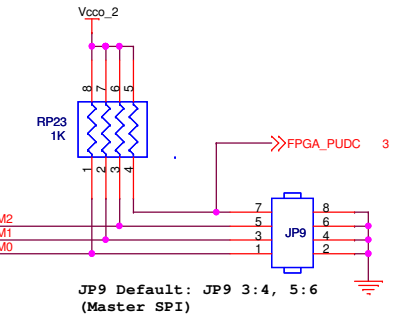
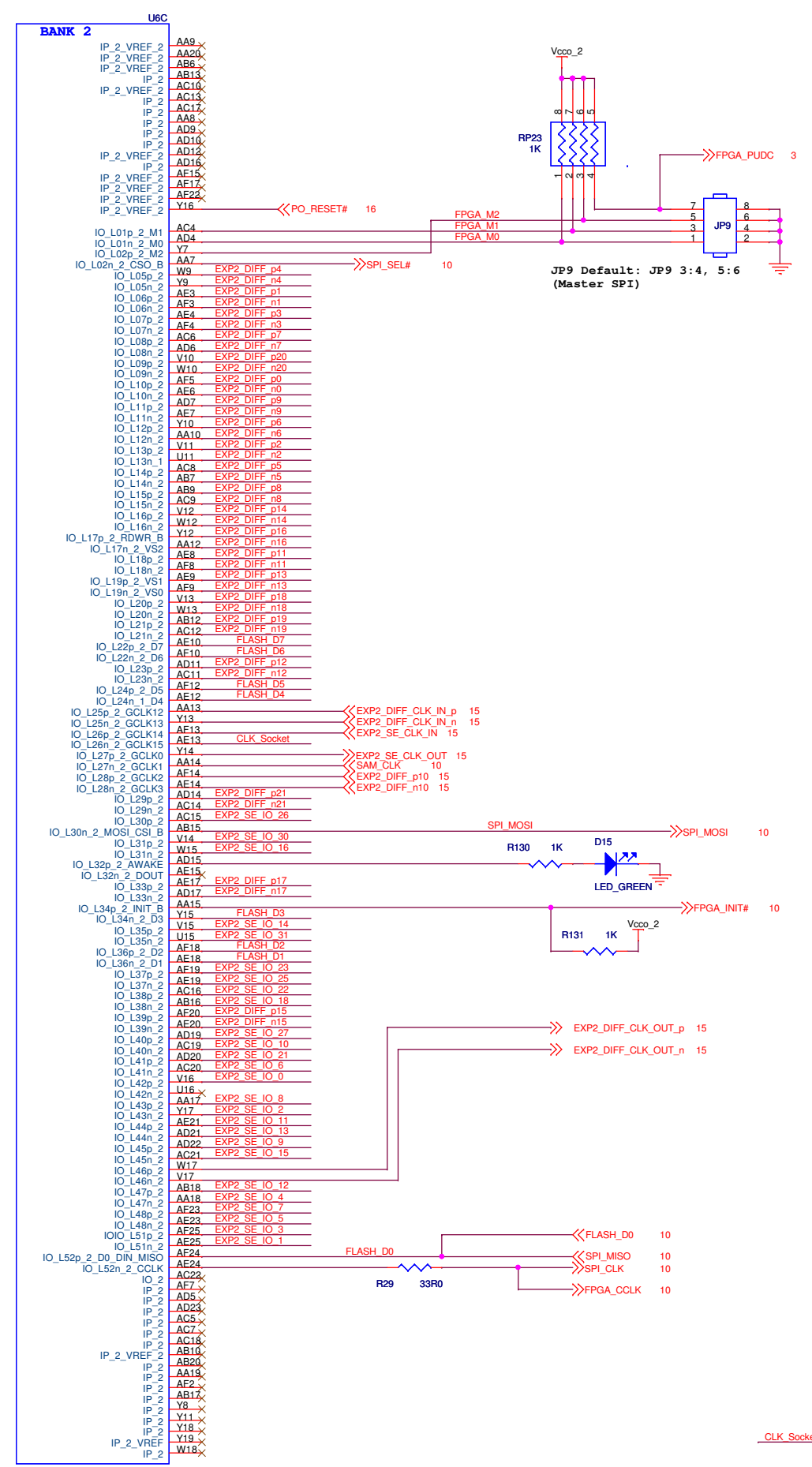
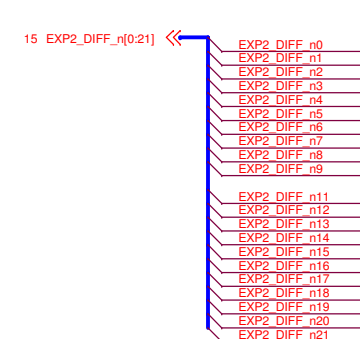
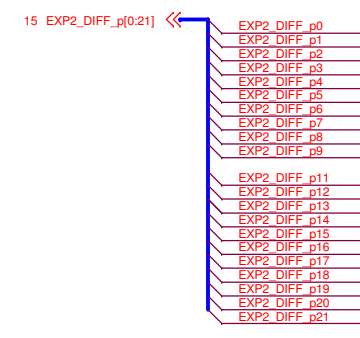
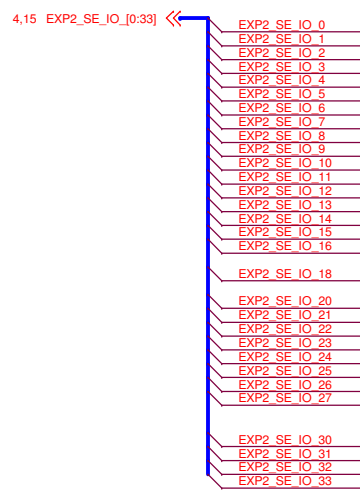
14 EXP1_DIFF_n[0:21] <<





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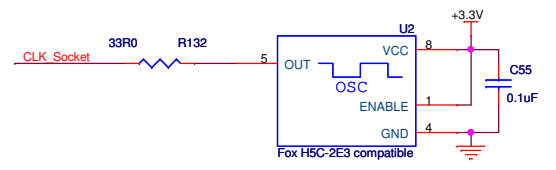
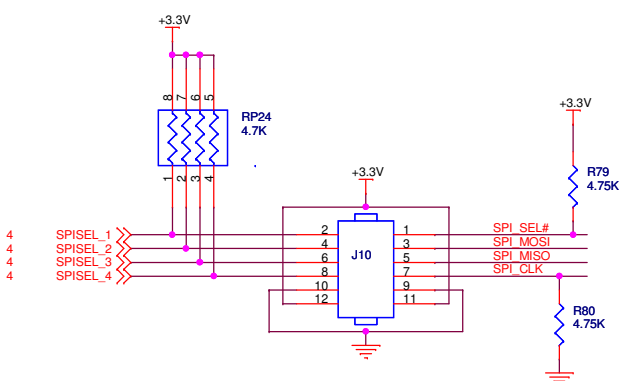
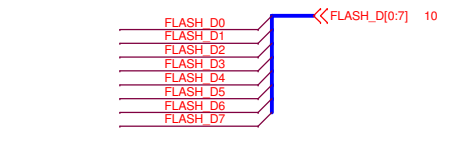
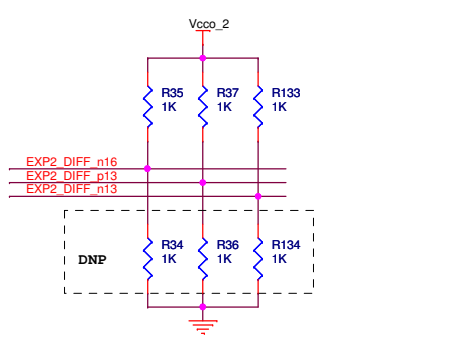


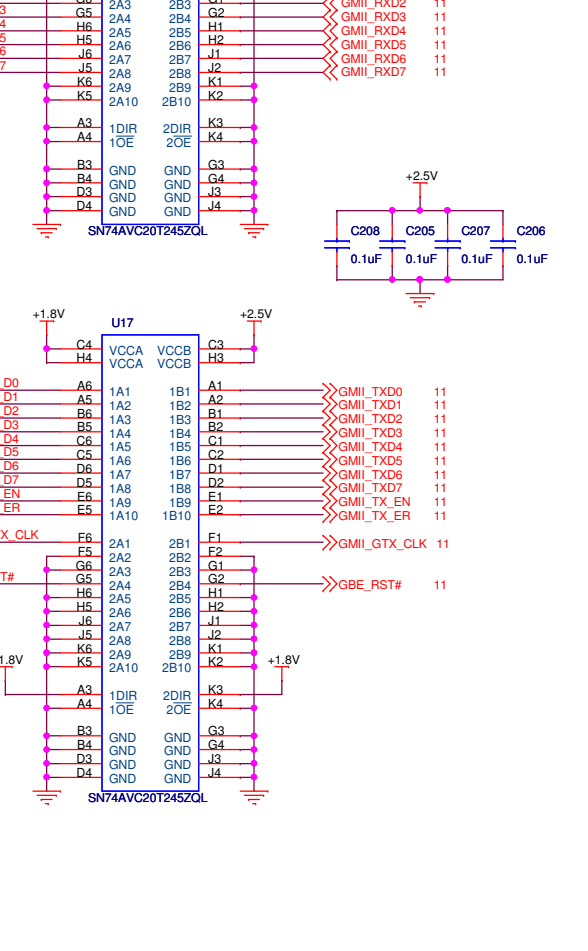
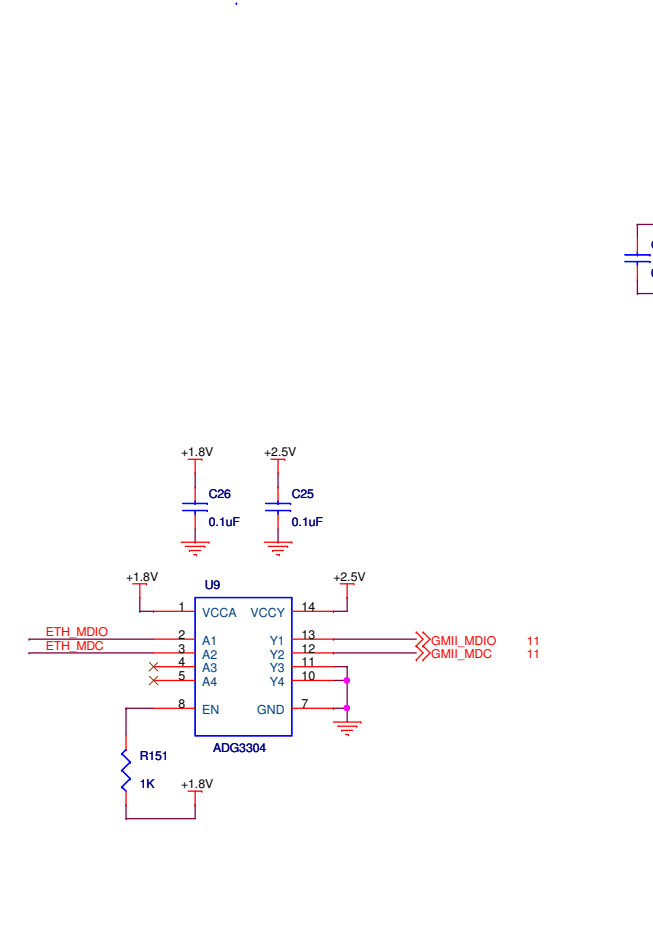
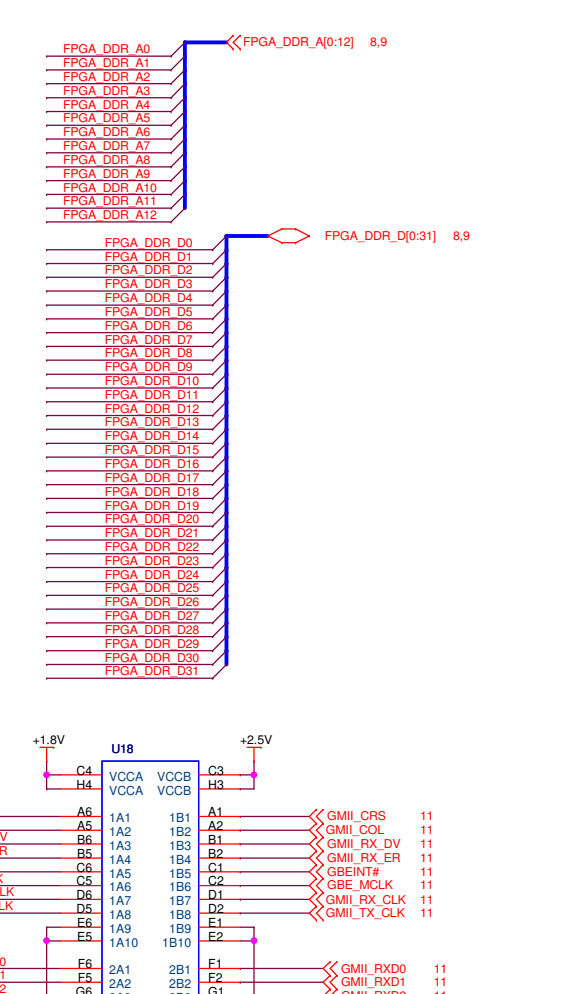
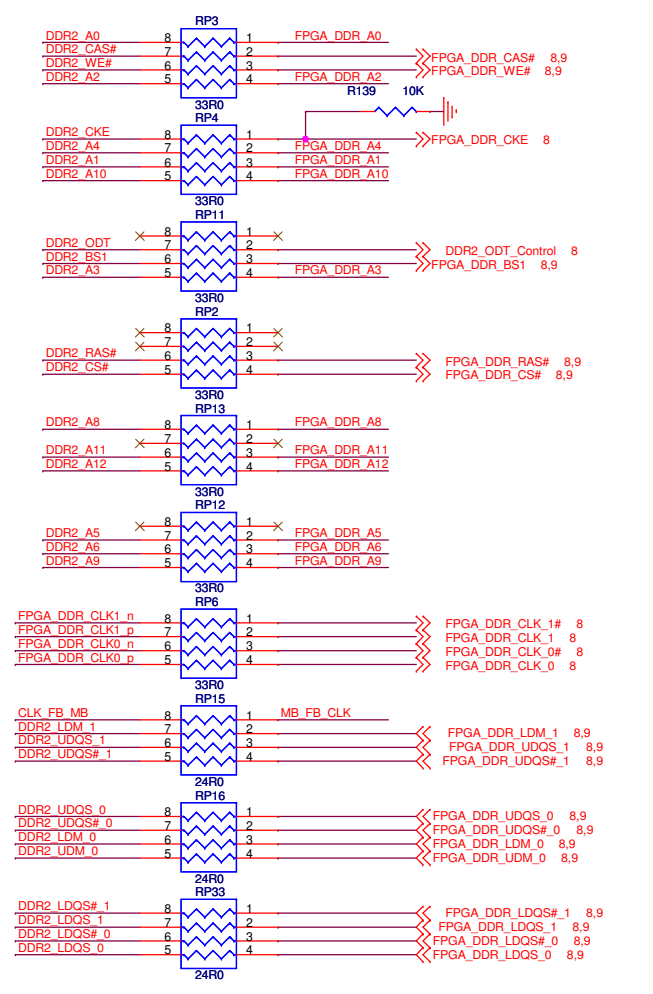
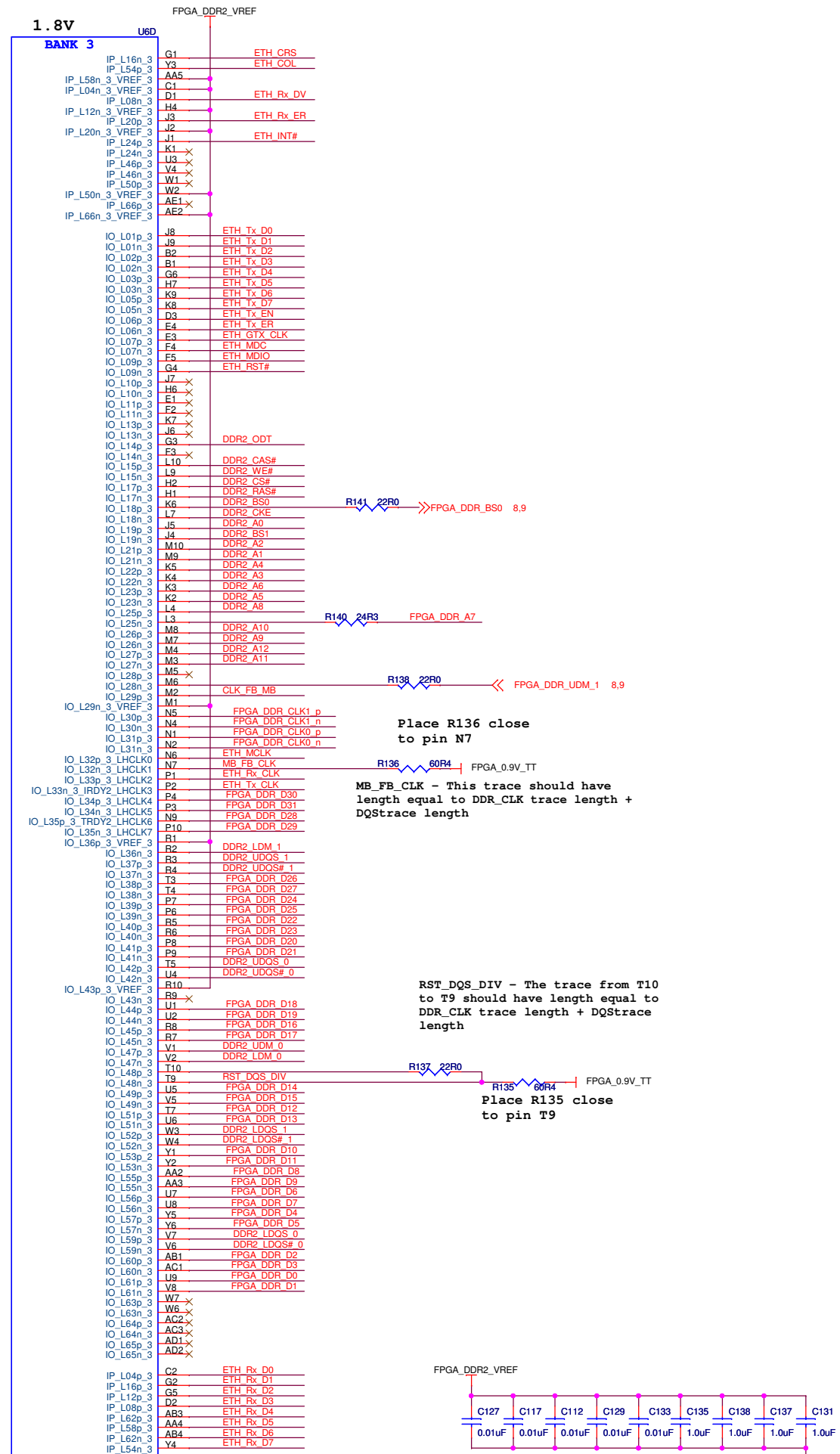


Configuration Mode	PC Pull-up	M2 JP9 5:6	M1 JP9 3:4	M0 JP9 1:2	PUDC_B JP9 7:8
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SPI	Yes	Closed	Closed	Open	Closed
Master SPI	No	Closed	Closed	Open	Open
BPI Up	Yes	Closed	Open	Closed	Closed
BPI Up	No	Closed	Open	Closed	Open
Slave Parallel	Yes	Open	Open	Closed	Closed
Slave Parallel	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

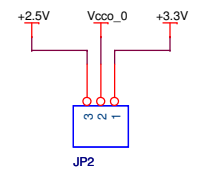
Resistors R34 - R37 and R133-R134 are for variant select (VS) to support SPI configuration of the FPGA.

VS[2:0] = b111 results in a SPI read command of Fast Read (0x0B) which is compatible with Intel S33 Flash.



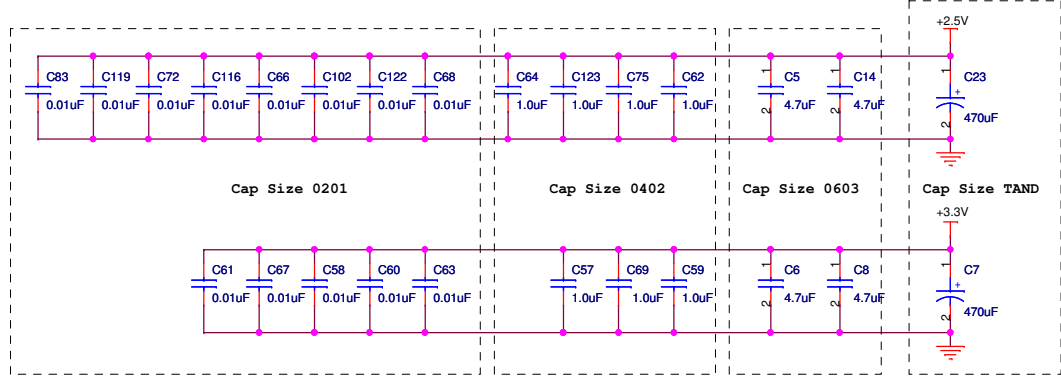
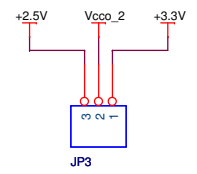


EXP1 VOLTAGE SELECT

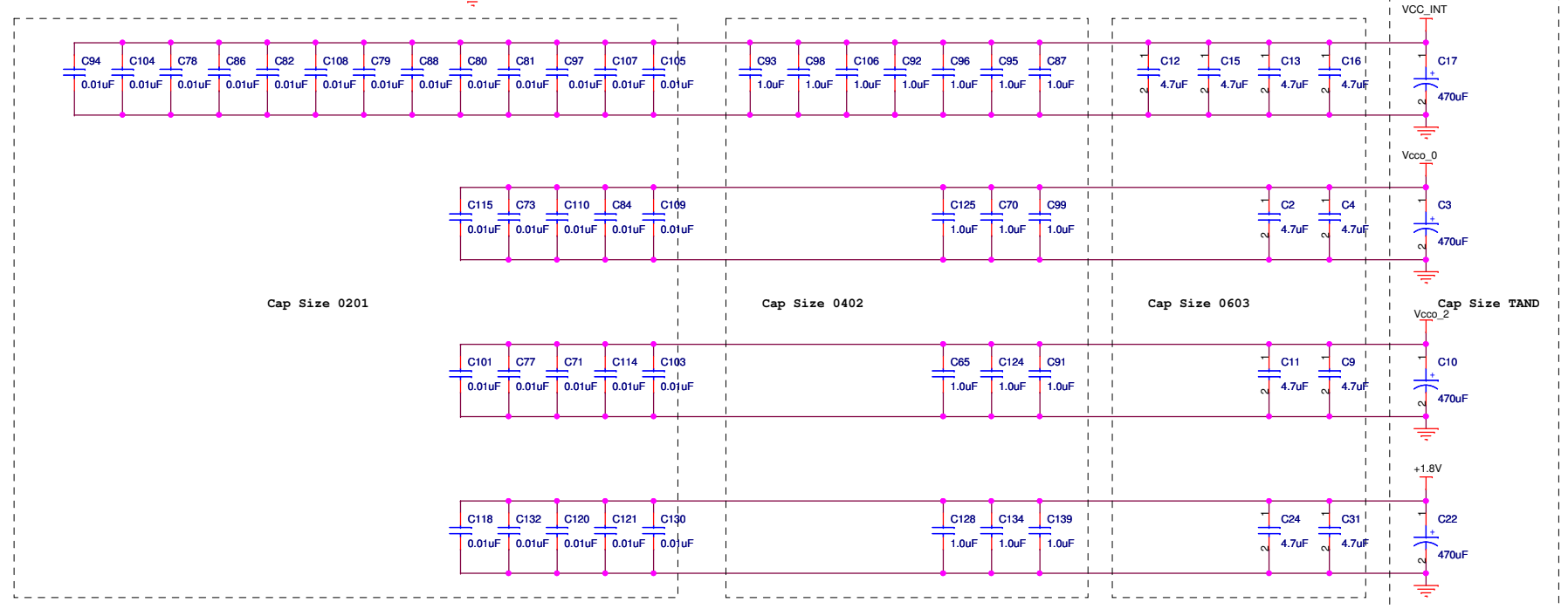
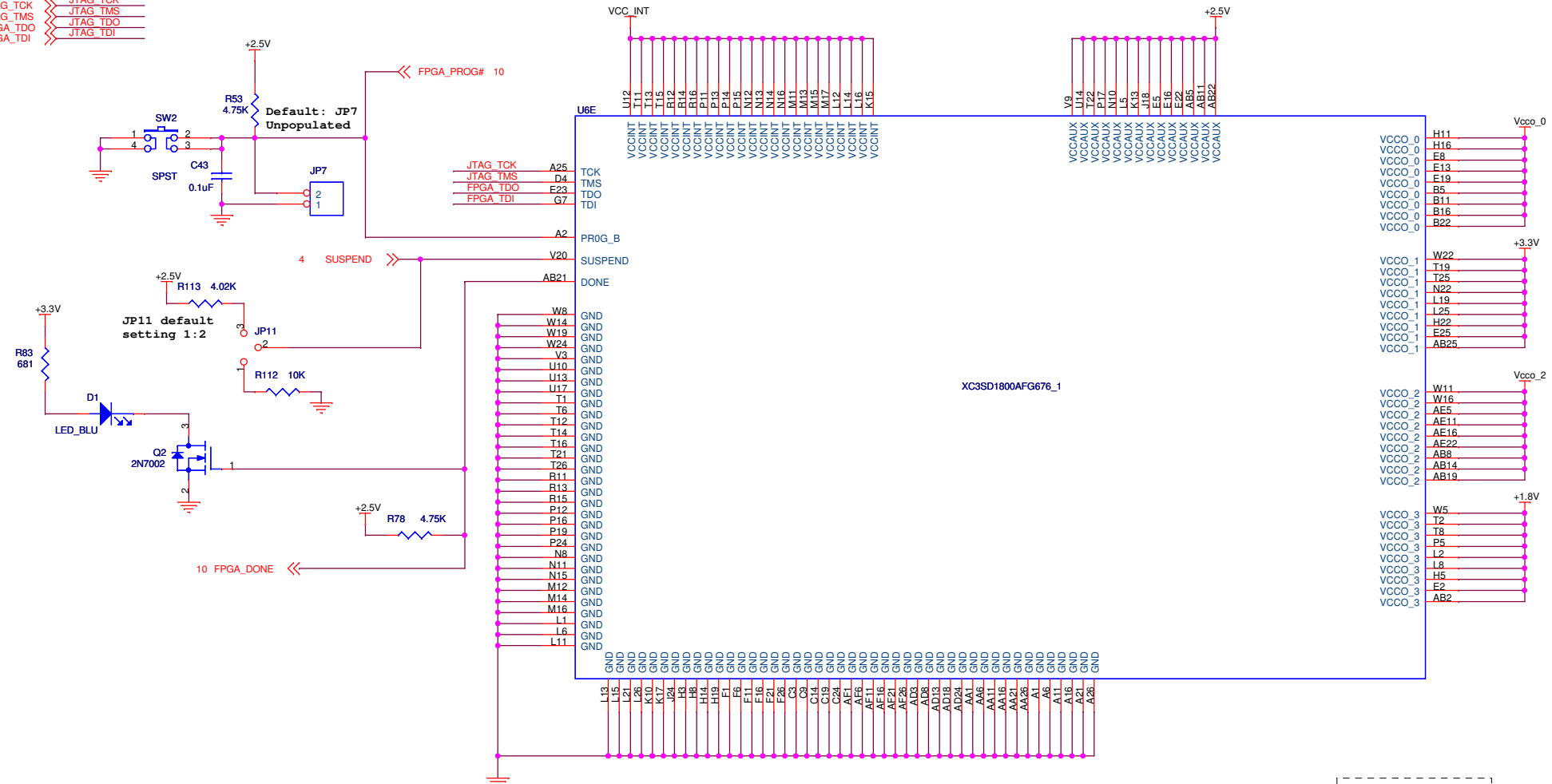


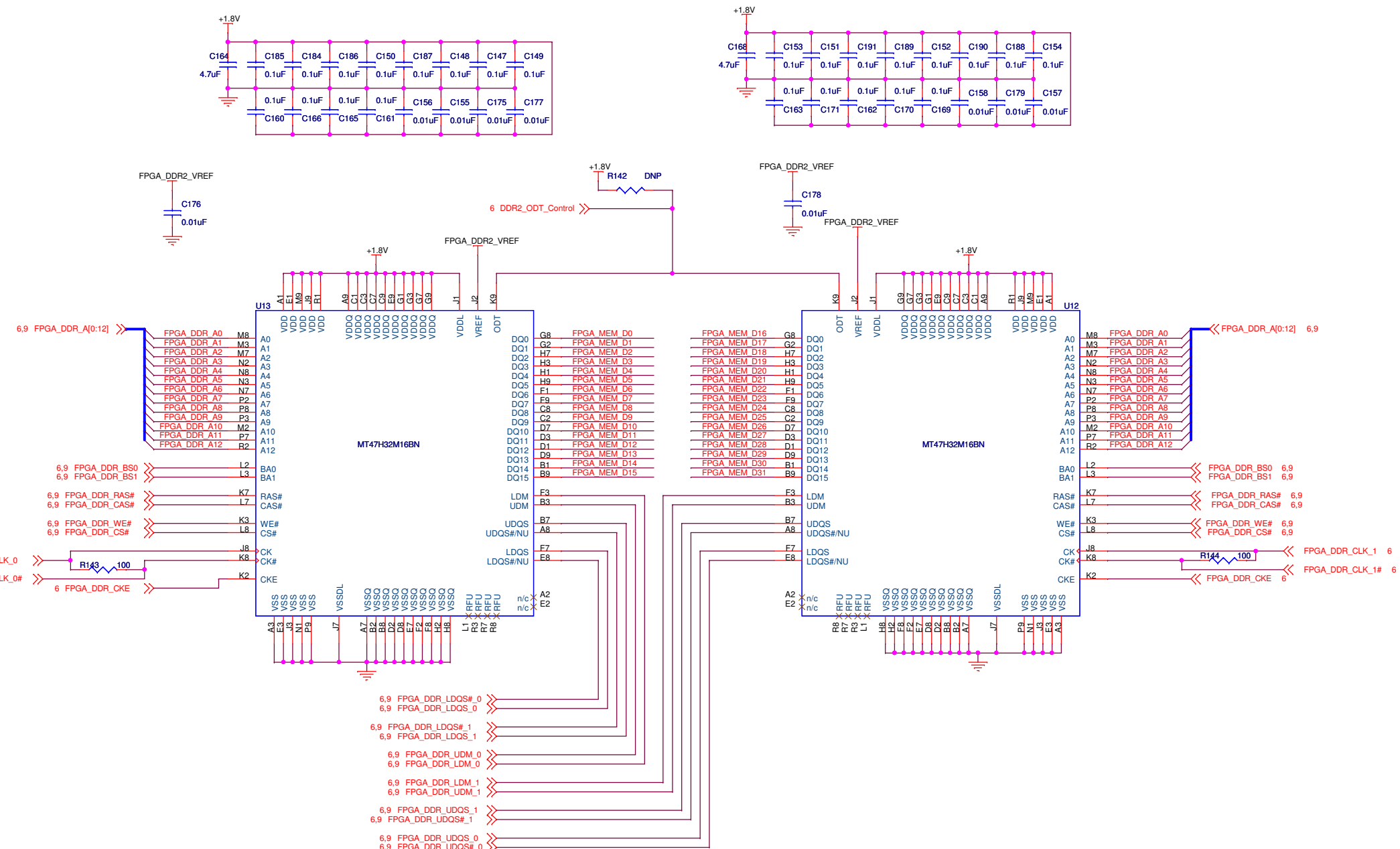
Default: JP2 1:2 (VCCO_0 = +3.3V)
 Default: JP3 1:2 (VCCO_2 = +3.3V)

EXP2 VOLTAGE SELECT

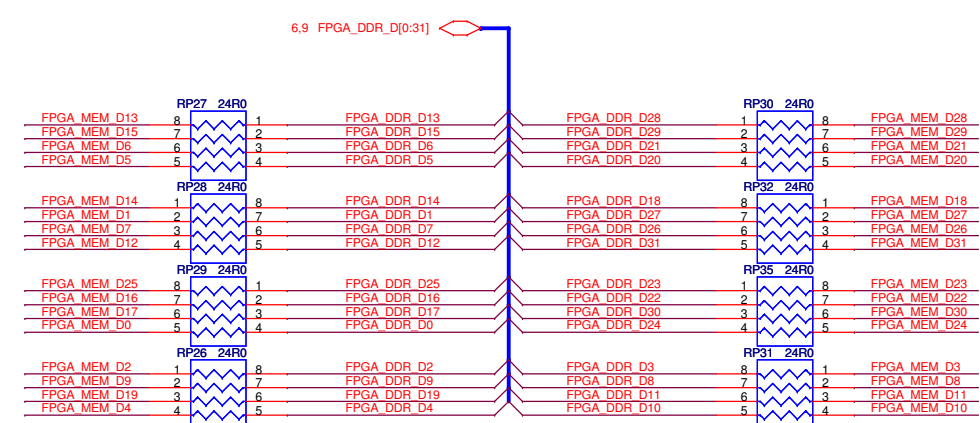


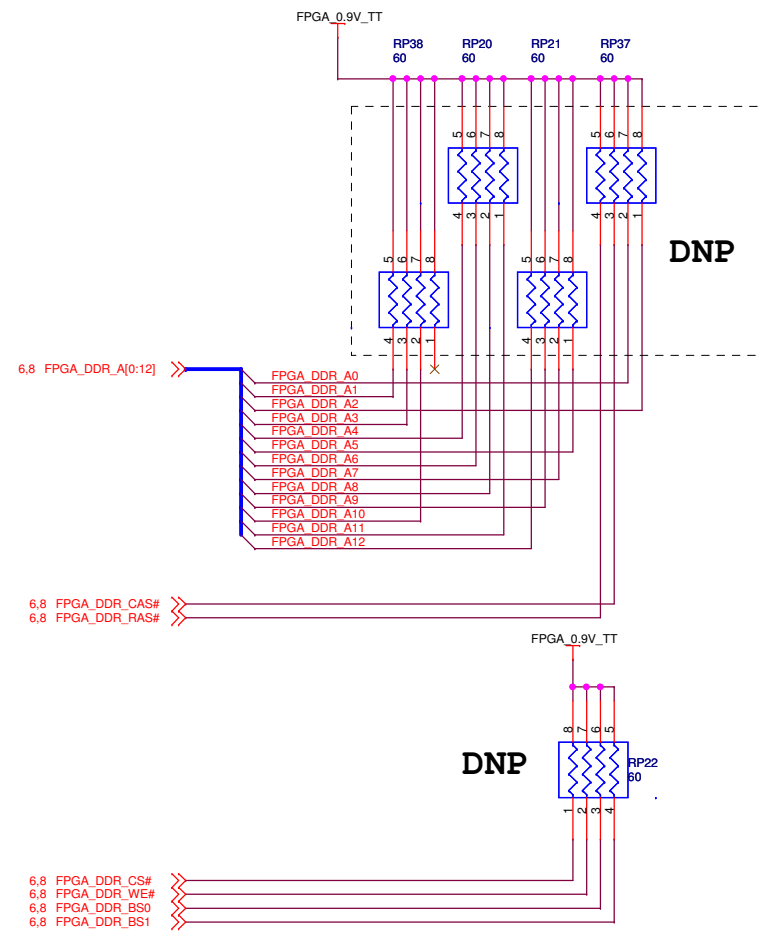
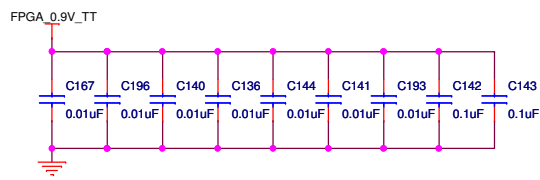
- 10 JTAG_TCK <> JTAG_TCK
- 10 JTAG_TMS <> JTAG_TMS
- 10 JTAG_TDO <> JTAG_TDO
- 10 JTAG_TDI <> JTAG_TDI



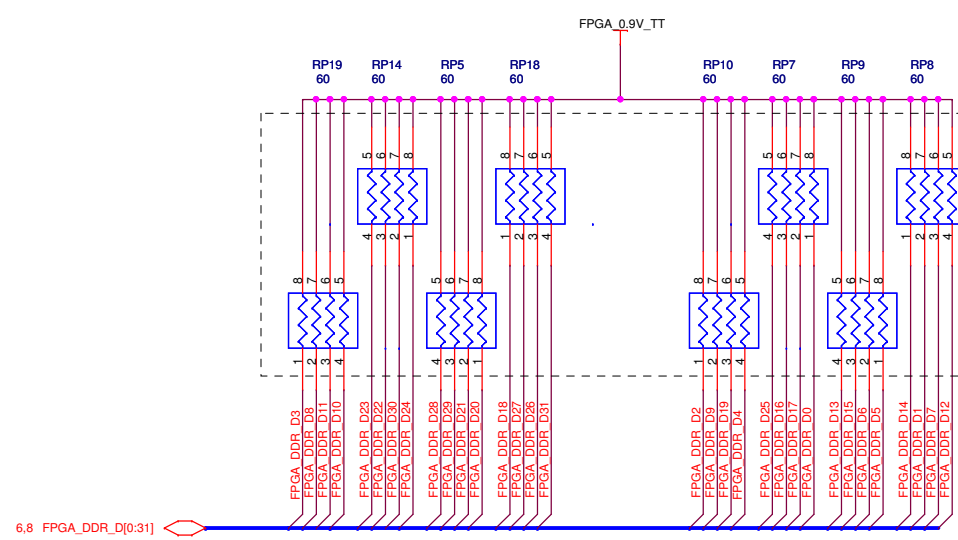
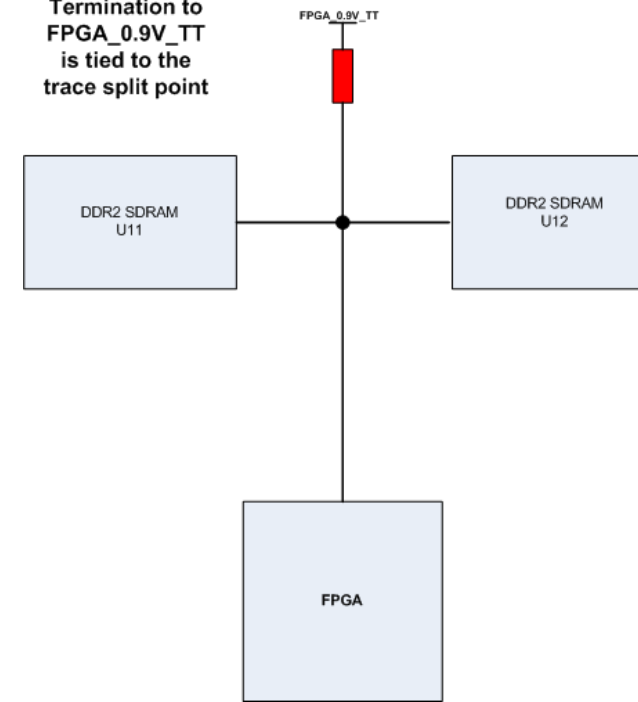


Place series terminations close to FPGA



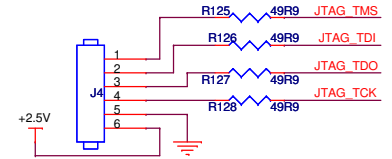
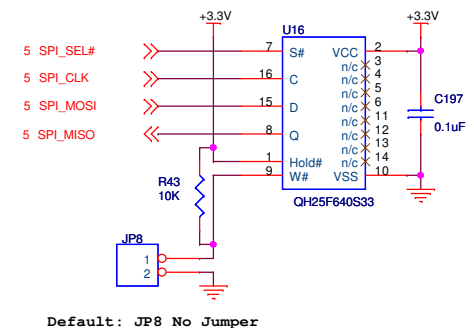
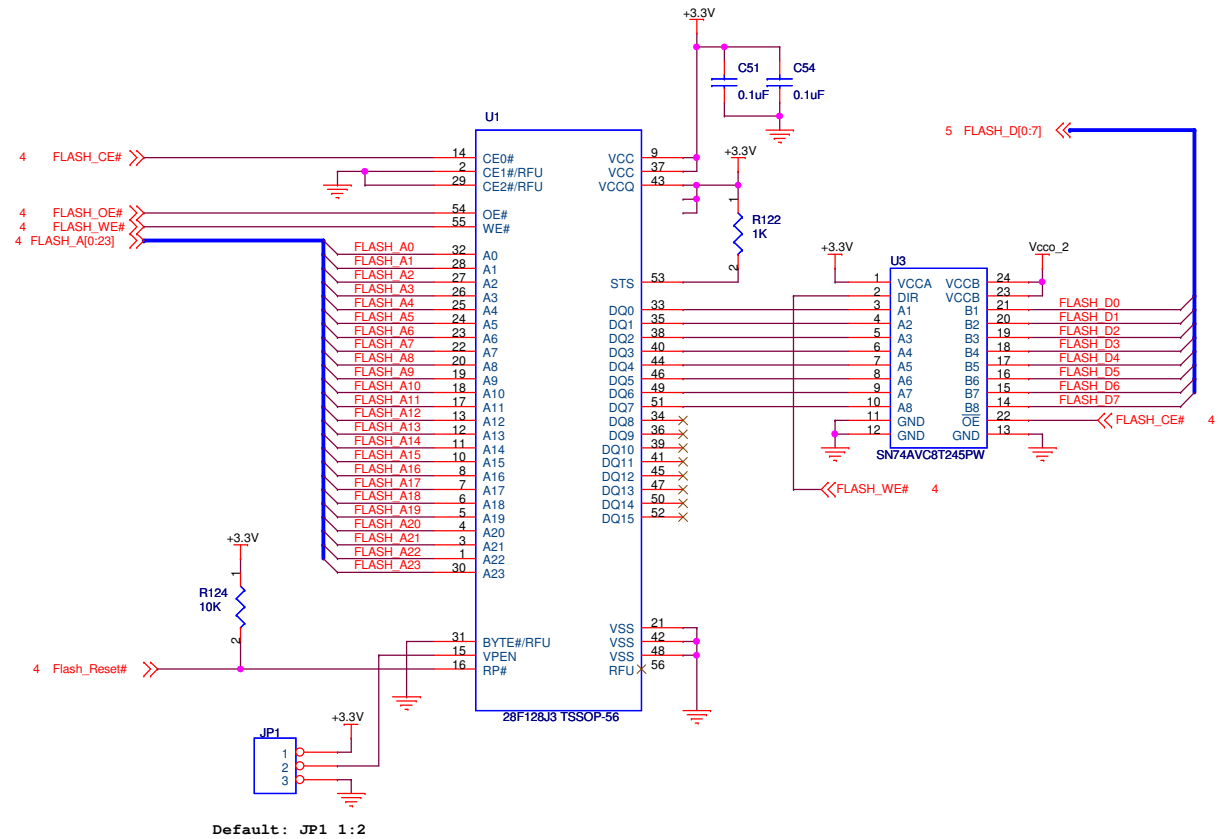


NOTE:
Termination to
FPGA_0.9V_TT
is tied to the
trace split point

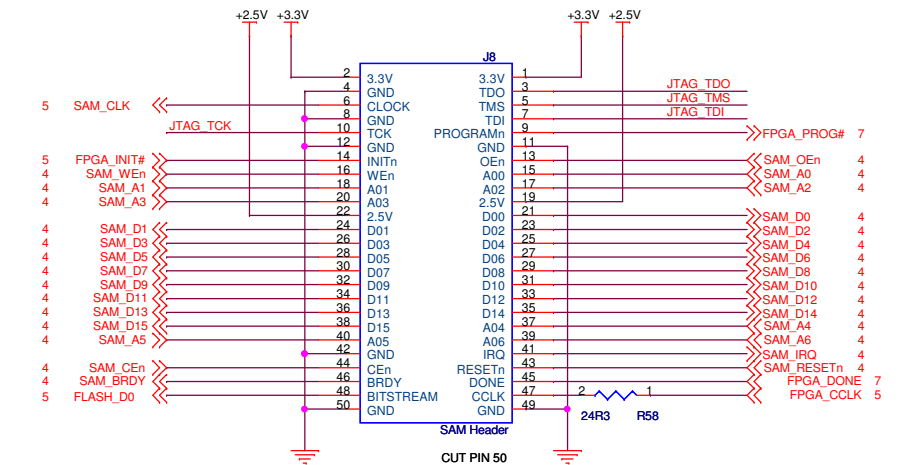
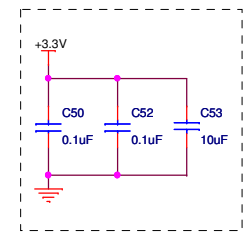
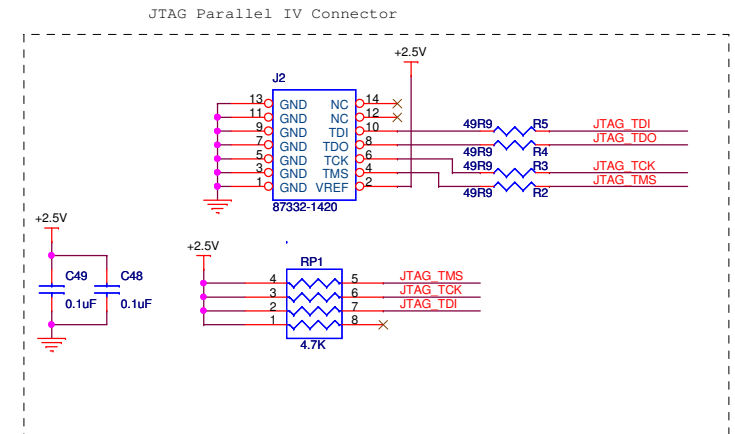


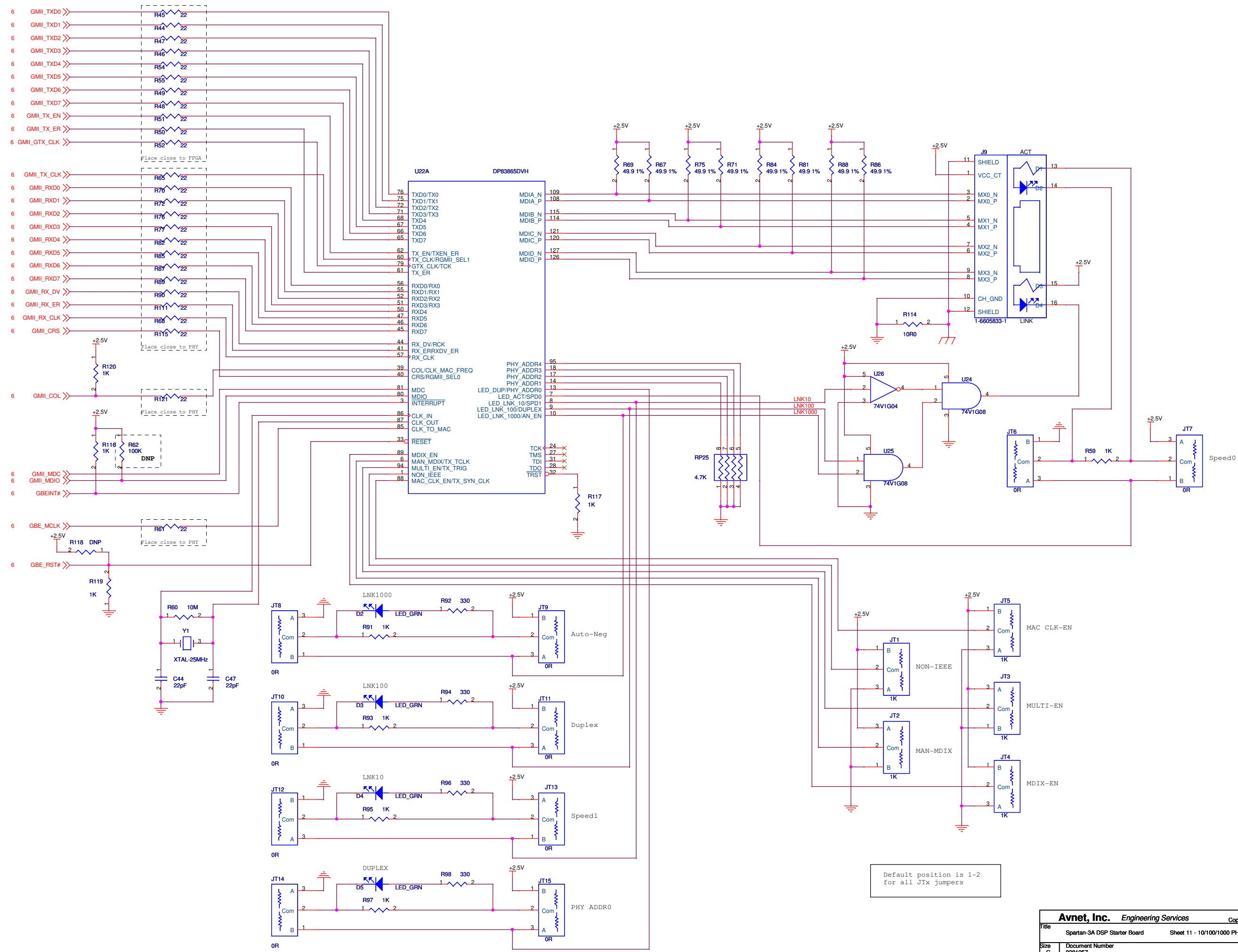
Layout Note:
Install
terminators as
close as possible
to the FPGA (U6)

- 6.8 FPGA_DDR_UDQS_0
- 6.8 FPGA_DDR_UDQS#_0
- 6.8 FPGA_DDR_UDQS_1
- 6.8 FPGA_DDR_UDQS#_1
- 6.8 FPGA_DDR_LDM_0
- 6.8 FPGA_DDR_LDM_1
- 6.8 FPGA_DDR_LDM#_0
- 6.8 FPGA_DDR_LDM#_1
- 6.8 FPGA_DDR_LDQS_0
- 6.8 FPGA_DDR_LDQS#_0
- 6.8 FPGA_DDR_LDQS_1
- 6.8 FPGA_DDR_LDQS#_1

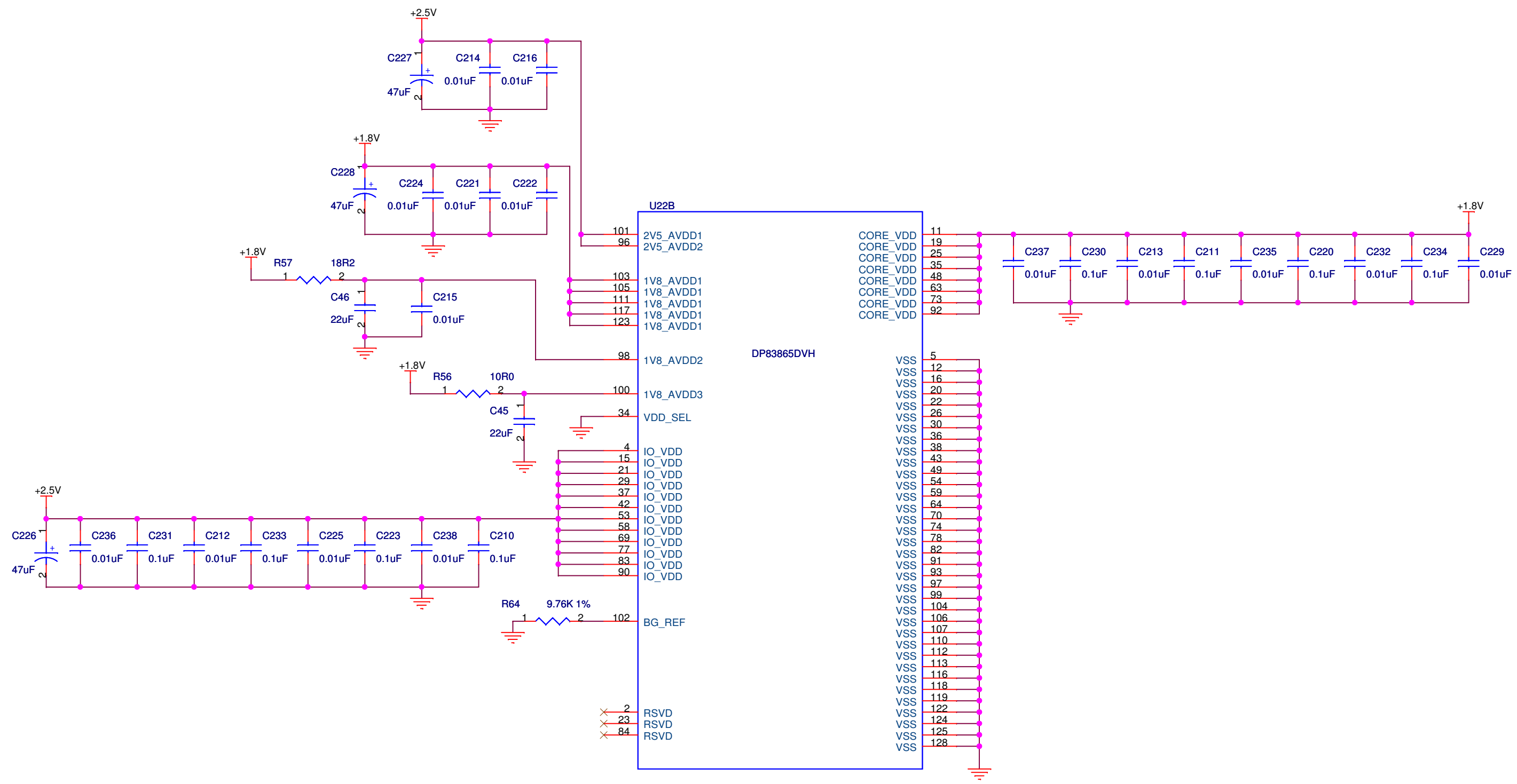


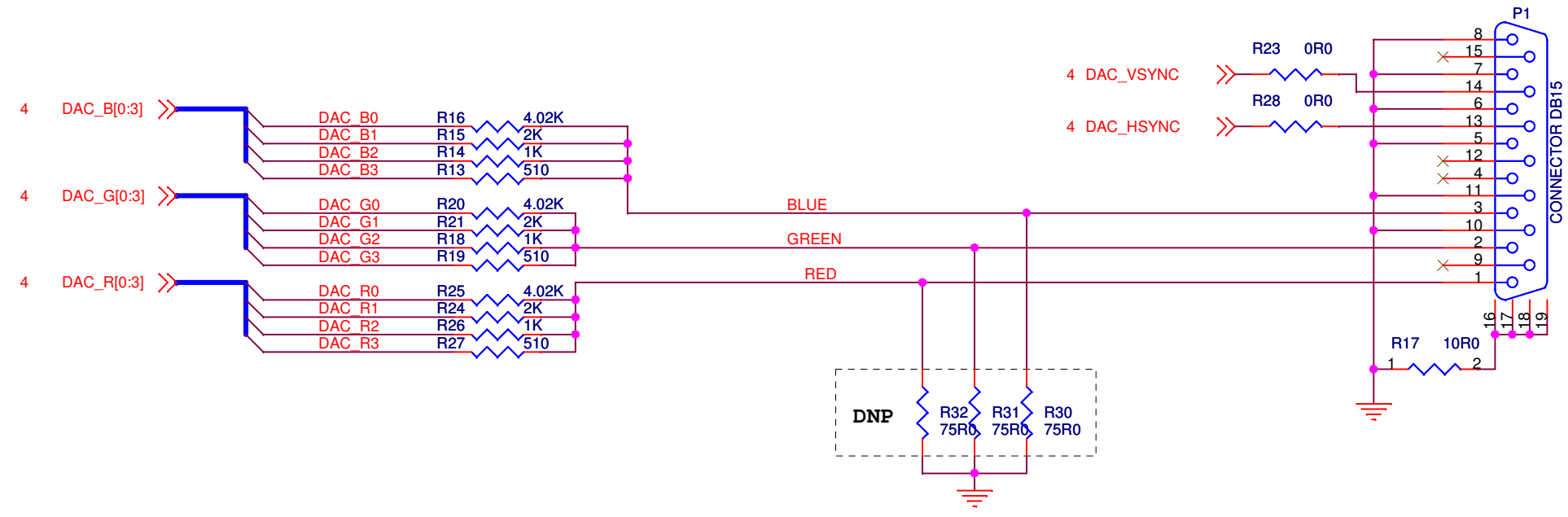
Layout Note: Place J4 and J2 close together

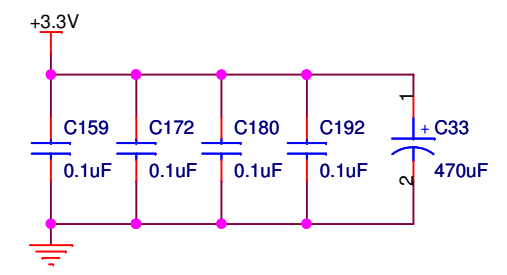
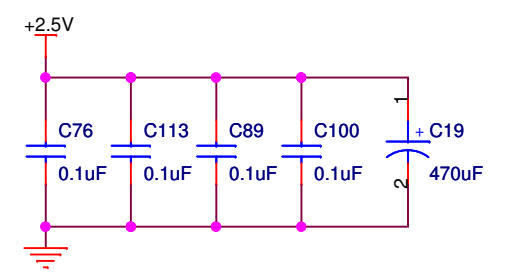
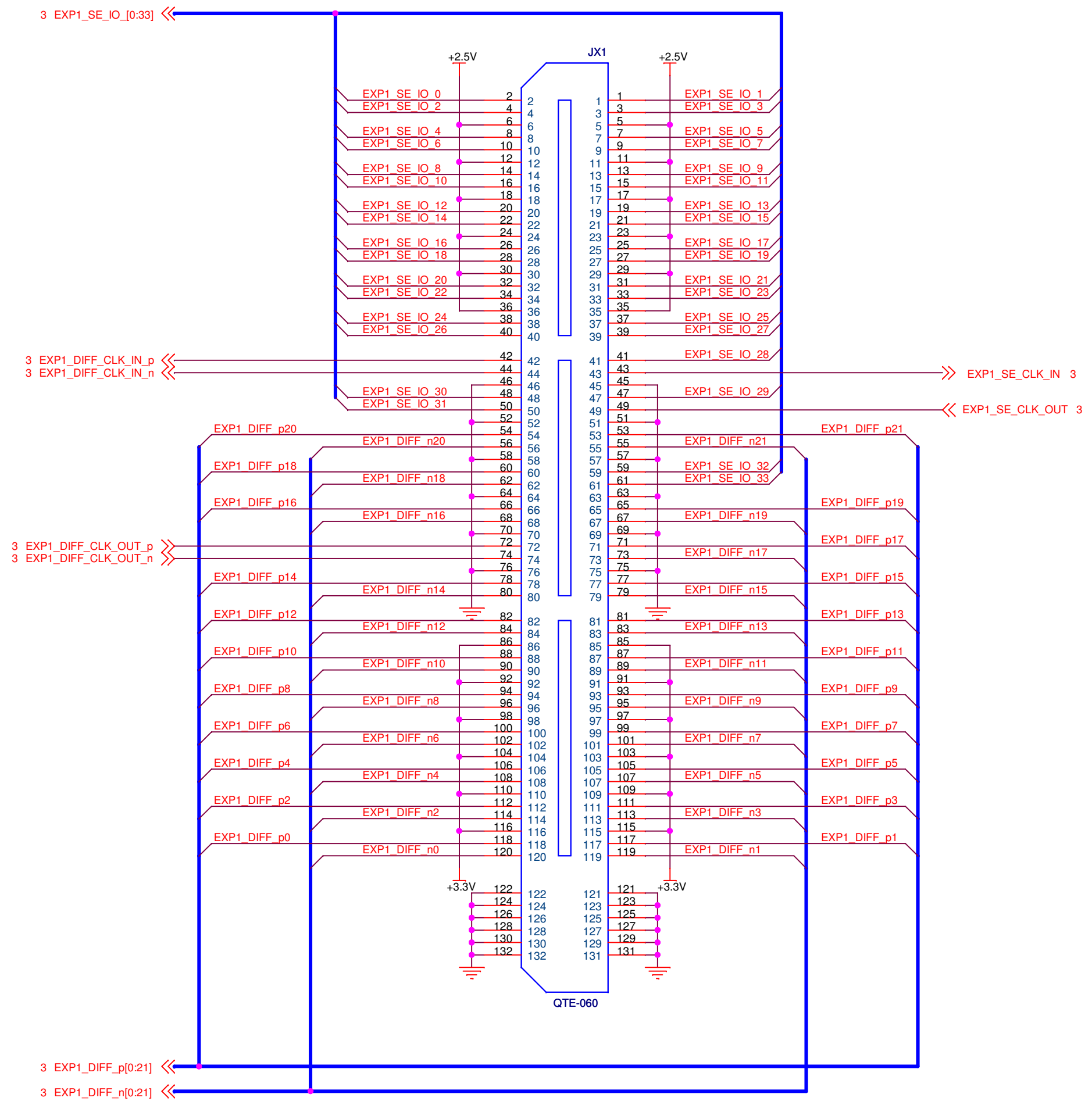




Default position is 1-2 for all JTx jumpers







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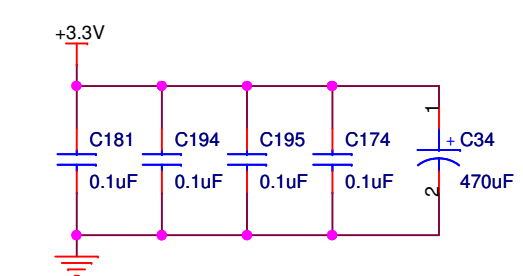
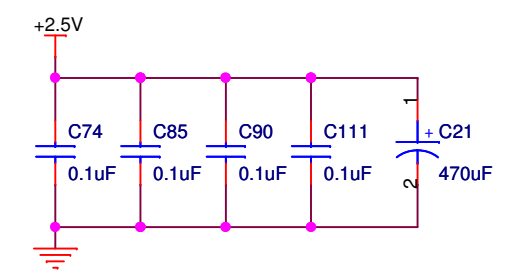
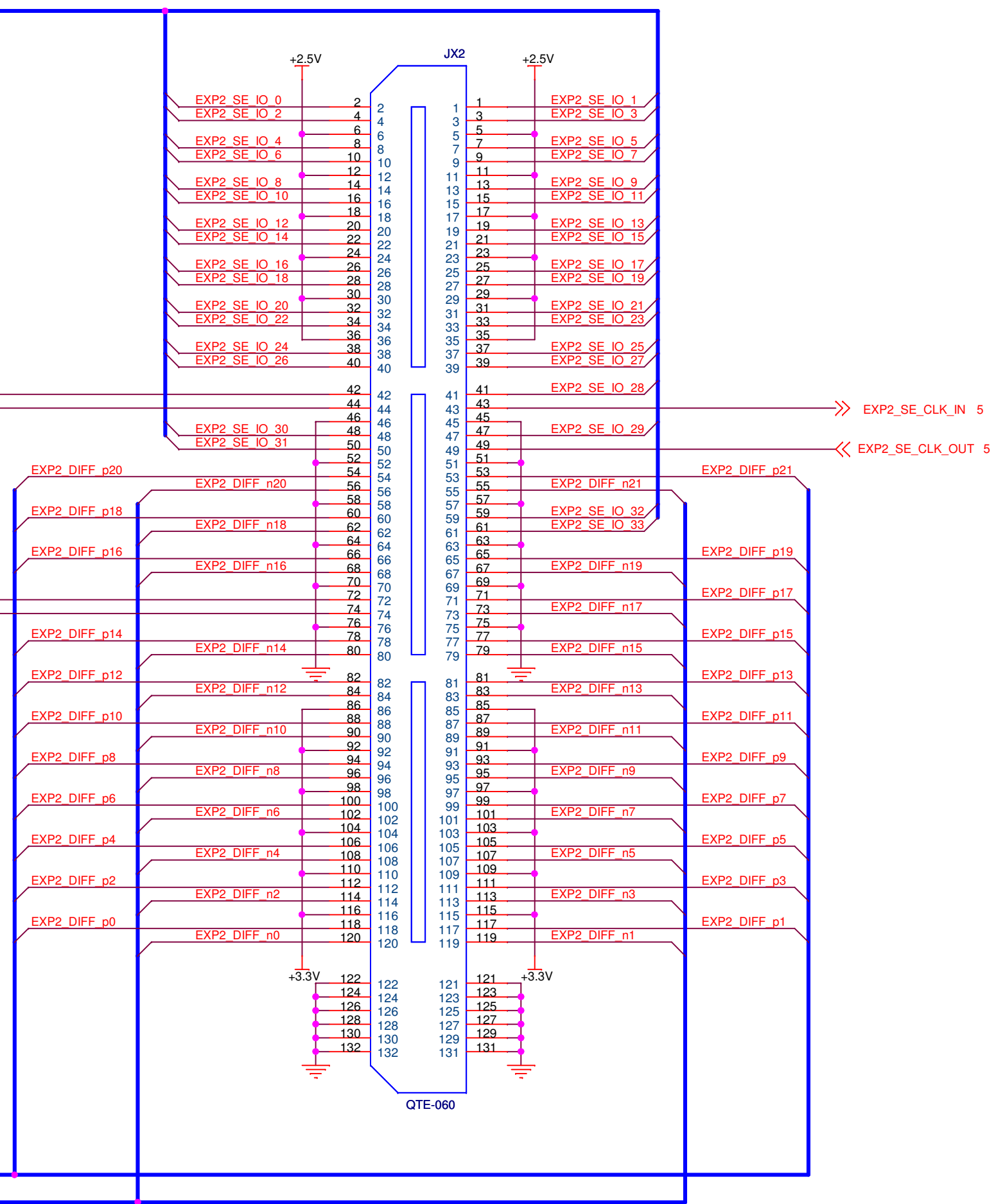
4,5 EXP2_SE_IO_[0:33] <<<

5 EXP2_DIFF_CLK_IN_p <<<
5 EXP2_DIFF_CLK_IN_n <<<

5 EXP2_DIFF_CLK_OUT_p <<<
5 EXP2_DIFF_CLK_OUT_n <<<

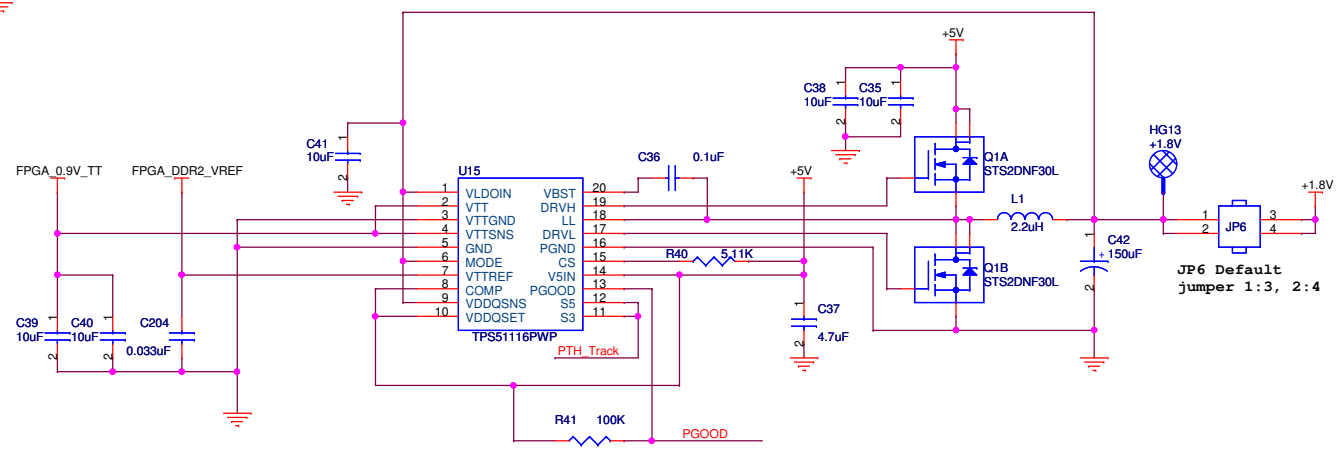
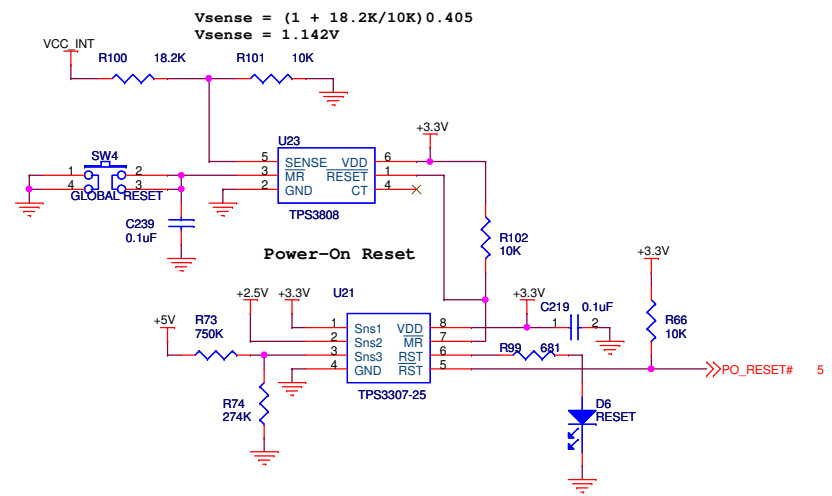
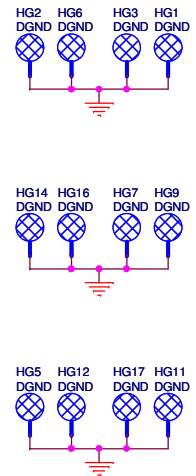
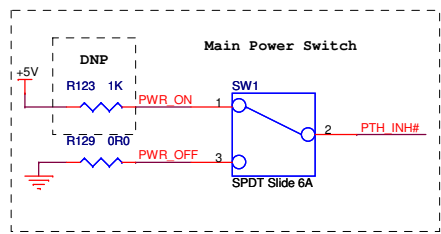
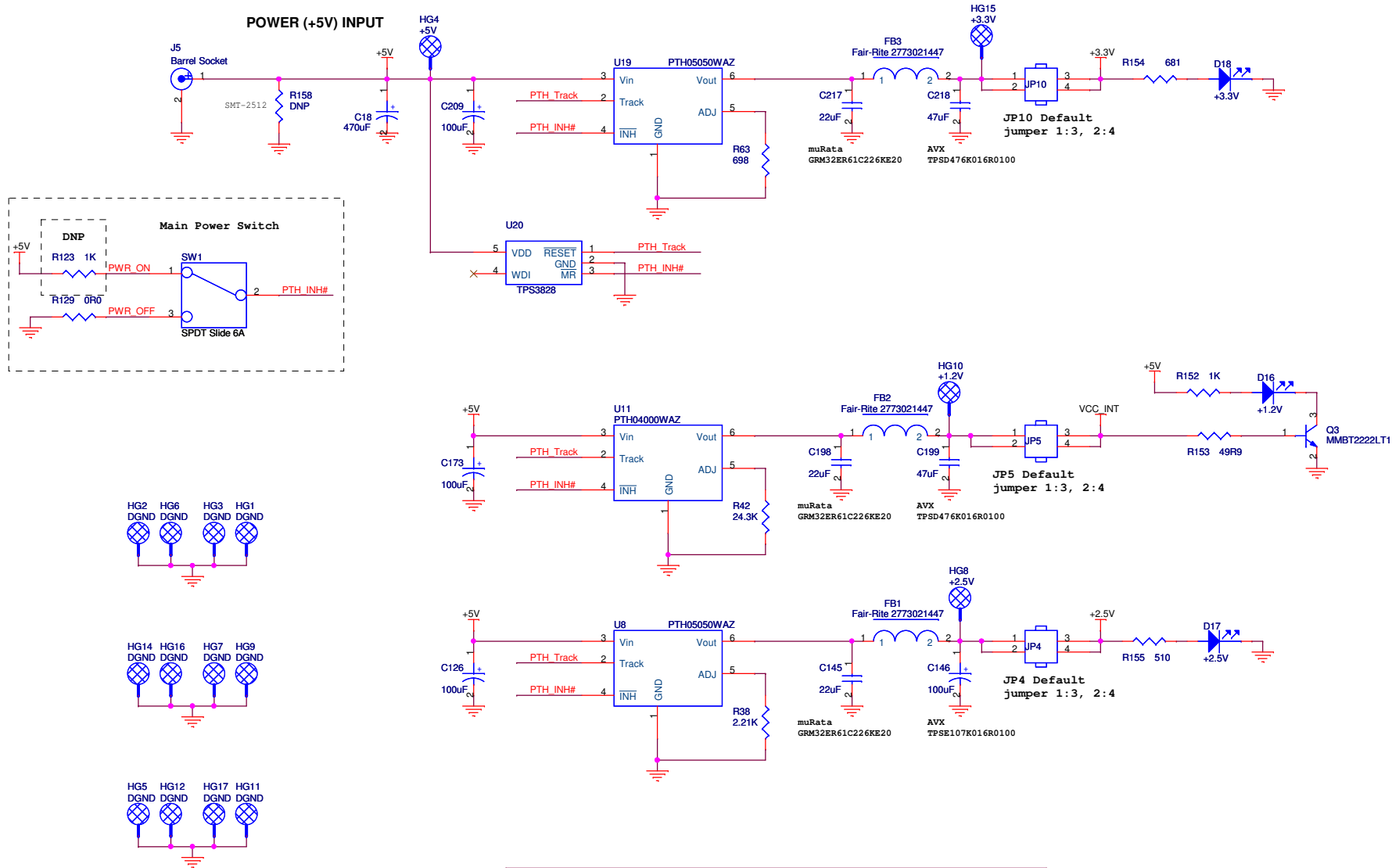
5 EXP2_DIFF_p[0:21] <<<

5 EXP2_DIFF_n[0:21] <<<



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POWER (+5V) INPUT



REV A

REV 1

ADDED POWER LEDS TO VCC_INT, +2.5V AND +3.3V RAILS
CONNECTED U20.3 TO PTH_INH# NET
ADDED A 2512 PKG LOAD RESISTOR TO +5V RAIL AT PWR JACK
ADDED PARALLEL TERMINATION TO SMA CLOCK INPUT
REMOVED LEVEL SHIFTER U14 & DIRECTLY CONNECTED SPI NETS TO U16
GROUNDING UNUSED I/O PINS ON TRANSCEIVERS U9, U17 & U18
CHANGED NAME OF PIN "V24" ON FPGA SYMBOL FROM "IP" TO "IO"

09/21/07: Updated Bank 2 of FPGA package by adding pin AA8 (IP_2) and changing pin AC22 from IP_2 (input only) to IO_2 (bidirectional)

11/26/07: Changed U1 device type from 28F128J3/P30 EBGA to 28F128J3 TSSOP-56

07/11/08: Corrected typo on pin U23 of FPGA (U6)

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Title		
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