Signetics

SCN2641
Asynchronous Communications Interface

Product Specification

Microprocessor Products

2

DESCRIPTION

The Signetics SCN2641 is a universal asynchronous data communications controller chip that interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt-driven system environment. The SCN2641 accepts programmed instructions from the microprocessor while supporting asynchronous serial data communications in full- or half-duplex mode.

The SCN2641 serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2641 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The SCN2641 is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 24-pin DIP.

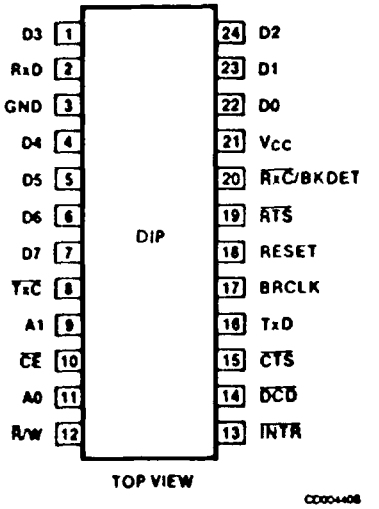
FEATURES

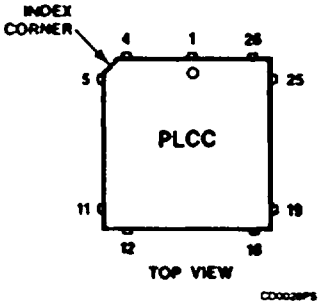
- 5- to 8-bit characters plus parity
- 1, 1½ or 2 stop bits transmitted
- Odd, even or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loopback mode
- Baud rate:
  - DC to 1M bps (1X clock)
  - DC to 62.5K bps (16X clock)
  - DC to 15.625K bps (64X clock)
- Internal or external baud rate clock
- 16 internal rates
- Double-buffered transmitter and receiver
- Single +5V power supply
- 400 mil package width

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Serial peripherals

PIN CONFIGURATION



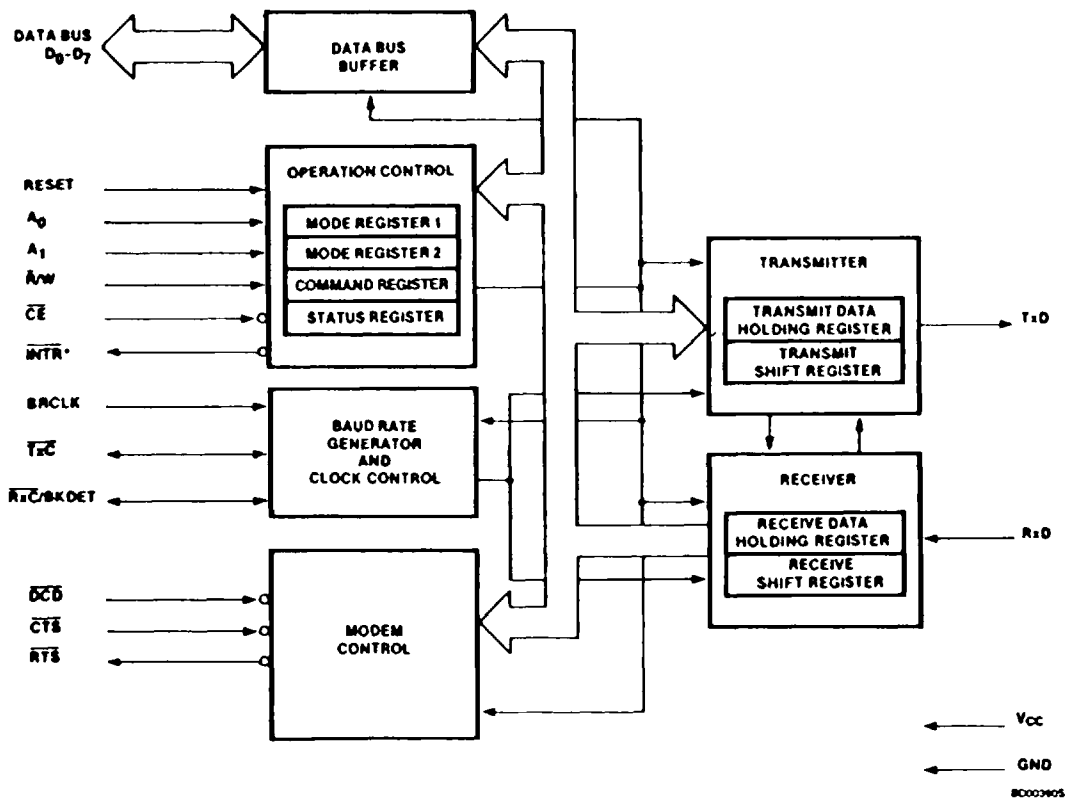


Pin	Function	Pin	Function
1	D2	15	INTR
2	D3	16	DCD
3	RxD	17	CTS
4	GND	18	NC
5	D4	19	TxD
6	D5	20	BRCLK
7	D6	21	RESET
8	NC	22	NC
9	D7	23	RTS
10	TxC	24	NC
11	A1	25	RxC/BKDET
12	CE	26	Vcc
13	A0	27	D0
14	R/W	28	D1

ORDERING CODE

PACKAGES	V_{CC} = 5V± 5%, T_A = 0°C to 70°C
Plastic DIP	SCN2641CC1N24
Plastic LCC	SCN2641CC1A28

BLOCK DIAGRAM



*Open drain output pin

BLOCK DIAGRAM

The SCN2641 consists of five major sections. These are the transmitter, receiver, timing, operation control and modem control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing are presented in the SCN2641 programming section of this data sheet.

Timing

The SCN2641 contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for certain errors and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, appends start and stop bits, and, optionally, a parity bit, and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for two input signals and one output signal used for "handshaking" and status indication between the CPU and a modem.

INTERFACE SIGNALS

The SCN2641 interface signals can be grouped into two types: the CPU-related signals (shown in table 2), which interface the SCN2641 to the microprocessor system and the device-related signals (shown in table 3), which are used to interface to the communications device or system.

OPERATION

The functional operation of the SCN2641 is programmed by a set of control words supplied by the CPU. These control words speci-

able 1. BAUD RATE GENERATOR CHARACTERISTICS (BRCLK = 3.6864MHz)

MR23 - 20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	4608
0001	75	1.2	—	3072
0010	110	1.7596	-0.022	2095
0011	134.5	2.152	—	1713
0100	150	2.4	—	1536
0101	300	4.8	—	768
0110	600	9.6	—	384
0111	1200	19.2	—	192
1000	1800	28.8	—	128
1001	2000	32.055	0.174	115
1010	2400	38.4	—	96
1011	3600	57.6	—	64
1100	4800	76.8	—	48
1101	7200	115.2	—	32
1110	9600	153.6	—	24
1111	19200	307.2	—	12

fy items such as baud rate, number of bits per character, etc. The programming procedure is described in the SCN2641 programming section of this data sheet.

After programming, the SCN2641 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The SCN2641 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. The receiver looks for a high-to-low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{INTR}$ output is asserted. If the character length is less than 8 bits, the high-order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive-going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 20 can be programmed to be a break detect output by appropriate setting of MR27 - MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 20 will go low. Refer to the break detection timing diagram.

Transmitter

The SCN2641 is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The SCN2641 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{INTR}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

The transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG status bit and the $\overline{INTR}$ output are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit (CR3) high.

Table 2. CPU-RELATED SIGNALS

PIN NAME	PIN NO. DIP	PIN NO. PLCC	INPUT/ OUTPUT	FUNCTION
V_{CC}	21	26	I	+5V supply input
GND	3	4	I	Ground
RESET	18	21	I	A high on this input performs a master reset on the SCN2641. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with appropriate control words.
$A_1 - A_0$	9, 11	11, 13	I	Address lines used to select internal SCN2641 registers.
$\overline{R}/W$	12	14	I	Read command when low, write command when high.
$\overline{CE}$	10	12	I	Chip enable command. When low, indicates that control and data lines to the SCN2641 are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the $D_0 - D_7$ lines in the three-state condition.
$D_7 - D_0$	7-4,1, 24-22	9,7-5, 2,1, 28,27	I/O	8-bit, three-state data bus used to transfer commands, data and status between the SCN2641 and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{INTR}$	13	15	O	Interrupt request output (open drain). This output is asserted (low) under the following conditions. 1. When the transmitter holding register (THR) is ready to accept a data character from the CPU. This corresponds to assertion of status bit SR0. If this is the only condition asserting the output, the output will be negated (high) when the THR is loaded by the CPU, or if the transmitter is disabled via command register bit CR0. 2. When the receiver holding register (RHR) has a character ready to be read by the CPU. This corresponds to assertion of status bit SR1. If this is the only condition asserting the output, the output will be negated (high) when the RHR is read by the CPU, or if the receiver is disabled via command register bit CR2. 3. When the transmitter has completed serialization of the last character loaded by the CPU. This corresponds to assertion of status bit SR2. If this is the only condition asserting the output, the output will be negated (high) when the THR is loaded by the CPU. 4. When a change of state has occurred at the $\overline{DCD}$ input while either the receiver or the transmitter are enabled. This corresponds to assertion of status bit SR2. If this is the only condition asserting the output, the output will be negated (high) when the status register is read by the CPU.

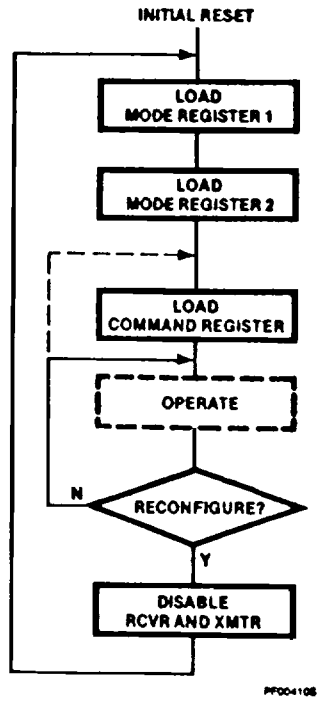
PROGRAMMING

Prior to initiating data communications, the SCN2641 operational mode must be programmed by performing write operations to the mode and command registers. The SCN2641 can be reconfigured at any time during program execution. A flowchart of the initialization process appears in figure 1.

The internal registers of the SCN2641 are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in table 4.

Reading or loading the mode registers is done as follows: the first write (or read) operation addresses mode register 1 and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointer is reset to mode register 1 by a RESET input or by performing a read command register operation, but is unaffected by any other read or write operation.

The SCN2641 register formats are summarized in tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the SCN2641, while the command register controls the operation within the basic framework. The SCN2641 indicates its status in the status register. These registers are cleared when a RESET input is applied.



NOTE:
Mode Register 1 must be written before 2 can be written. Mode register 2 need not be programmed if external clocks are used.

Figure 1. SCN2641 Initialization Flowchart

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR1 and MR10 select the baud rate multiplier. 1X, 16X and 64X multipliers are programmable or the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

MR17 and MR16 select character framing of 1, 1.5 or 2 stop bits. (If 1X baud rate is

programmed, 1.5 stop bits default to 1 stop bit on transmit.)

The bits in the mode register affecting character assembly and disassembly (MR12 – MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half-duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 – MR15 must be changed within n-bit times of the assertion of RxRDY/TxRDY. (n = smaller of the new and old character lengths.)

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable as per table 1. MR23 – MR20 are don't cares if external clocks are selected (MR25 – MR24 = 0). The individual rates are given in table 1.

MR24 – MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 8 and 20. Refer to table 6.

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high), while the TxRDY and TxEMT status bits go low. Disabling the receiver causes the RxRDY status bit to go low. If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be negated. A 0-to-1 transition of CR2 will initiate start bit search on the second $\overline{RxC}$ rising edge following the transition.

Bit CR5 (RTS) controls the RTS output. Data at the output is the logical complement of the register data.

Setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The user should wait at least one bit time after terminating the break before loading the THR with the next character to be transmitted.

Setting CR4 causes the error flags in the status register (SR3, SR4 and SR5) to be cleared. This is a one-time command. There is no internal latch for this bit.

Table 3. DEVICE-RELATED SIGNALS

PIN NAME	DIP	PLCC	INPUT/ OUTPUT	FUNCTION
BRCLK	17	20	I	Clock input to the internal baud rate generator (see table 1). Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$/ BKDET	20	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
RxD	2	3	I	Serial data input to the receiver. "Mark" is high, "space" is low.
$\overline{TxC}$	8	10	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output.
TxD	16	19	O	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{DCD}$	14	16	I	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{INTR}$ when its state changes if CR2 or CR0 = 1. If DCD goes high while receiving, the RxC is internally inhibited. Operation of the receiver resumes on the second $\overline{RxC}$ rising edge following assertion of DCD.
$\overline{CTS}$	15	17	I	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{RTS}$	19	23	O	General-purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details.

Table 4. REGISTER ADDRESSING

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	Three-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Invalid
0	1	0	0	Read mode registers ½
0	1	0	1	Write mode registers ½
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE:
See AC characteristics section for timing requirements.

When CR5 (RTS) is set, the RTS pin is forced low. A 1-to-0 transition of CR5 will cause $\overline{RTS}$ to go high (inactive) one TxC time after the last serial bit has been transmitted. If a 1-to-0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain low (active) until both the THR and the transmit shift register are empty and then go high one TxC time later.

The SCN2641 can operate in one of four submodes. The operational submode is determined by CR7 and CR6. CR7 - CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

CR7 - CR6 = 01 places the SCN2641 in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU-to-receiver communications continue normally, but the CPU-to-transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. The $\overline{INTR}$ pin will reflect only the data set change condition.
4. The TxEN command (CR0) is ignored.

Two diagnostic submodes can also be configured. In local loopback mode (CR7 - CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmitter clock.
4. The $\overline{RTS}$ and TxD outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the SCN2641.

The second diagnostic mode is the remote loopback mode (CR7 - CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{INTR}$ output is held high.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in table 8) indicate receiver and transmitter conditions and modem/data set status

SR0 is the transmitter ready (TxRDY) status bit. It is valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{INTR}$ output pin is low, except in the automatic echo and remote loopback modes.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to 0, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{INTR}$ output is low.

Table 5. MODE REGISTER 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Stop Bit Length		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
00 = Invalid 01 = 1 stop bit 10 = 1½ stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Invalid 01 = 1X rate 10 = 16X rate 11 = 64X rate	

NOTE:
Baud rate factor applies only if external clock is selected. Factor is 16X if internal clock is selected.

Table 6. MODE REGISTER 2 (MR2)

MR27 - MR24										MR23 - MR20
	TxC	RxC	Pin 8	Pin 20		TxC	RxC	Pin 8	Pin 20	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	NF	RxC/TxC	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	
0010	I	E	1X	RxC	1010	I	E	NF	RxC	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	See baud rates in table 1
0100	E	E	TxC	RxC	1100	E	E	NF	RxC/TxC	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	
0110	I	E	16X	RxC	1110	I	E	NF	RxC	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	

NOTES:
E = External clock
I = Internal clock (BRG)
NF = No function; output not valid
1X and 16X are clock outputs

Table 7. COMMAND REGISTER (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request To Send	Reset Error	Force Break	Receive Control (RxEN)		Transmit Control (TxEN)
00 = Normal operation 01 = Automatic echo mode 10 = Local loopback 11 = Remote loopback		0 = Force $\overline{RTS}$ output high after TxSR serialization 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flags in status register (FE, O	0 = Normal 1 = Force break	0 = Disable 1 = Enable	Not used. Must be programmed to '1'	0 = Disable 1 = Enable

Table 8. STATUS REGISTER (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
	Data Carrier Detect	Framing Error	Overrun Error	Parity Error	TxEMT/DSCHG	RxRDY	TxRDY
Not used	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	0 = Normal 1 = Framing Error	0 = Normal 1 = Overrun Error	0 = Normal 1 = Parity error	0 = Normal 1 = Change in $\overline{DCD}$ or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register busy

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DCD}$ input (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when the TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 = 1 while SR6 remains unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{INTR}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. This bit is cleared when the receiver is disabled and by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

Bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. The bit is reset when the receiver is disabled and when the reset error command is given.

SR6 reflects the condition of the DCD input. A low input sets the status bit and a high input clears it.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
Output voltage						V
V_{OL}	Low	I_{OL} = 2.2mA			0.4	
V_{OH}[7]	High	I_{OH} = −400μA	2.4			
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}			10	μA
3-state output leakage current						μA
I_{LH}	Data bus high	V_O = 4.0V			10	
I_{LL}	Data bus low	V_O = 0.45V			10	
I_{CC}	Power supply current				150	mA

CAPACITANCE T_A = 25°C, V_{CC} = 0V

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						pF
C_{IN}	Input	fc = 1MHz			20	
C_{OUT}	Output	Unmeasured pins tied to ground			20	
$C_{I/O}$	Input/Output				20	

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%[4,5,6]

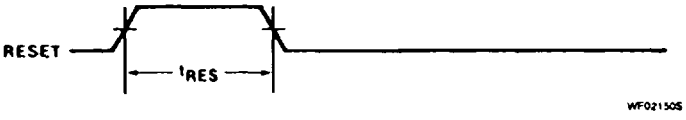
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Pulse width						ns
t_{RES}	Reset		1000			
t_{CE}	Chip enable		250			
t_{CED}	CE to CE delay		600			
Set-up and hold time						ns
t_{AS}	Address set-up		10			
t_{AH}	Address hold		10			
t_{CS}	$\overline{R}$/W control set-up		10			
t_{CH}	$\overline{R}$/W control hold		10			
t_{DS}	Data set-up for write		150			
t_{DH}	Data hold for write		10			
t_{RXS}	Rx data set-up		300			
t_{RXH}	Rx data hold		350			
t_{DD}	Data delay time for read	C_L = 150pF			200	ns
t_{DF}	Data bus floating time for read	C_L = 150pF			100	ns
Input clock frequency						MHz
f_{BRG}	Baud rate generator		1.0	3.6864	4.0	
$f_{R/T}$[10]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	
Clock state						ns
t_{BRH}[9]	Baud rate high		90			
t_{BRL}[9]	Baud rate low		90			
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		480			
$t_{R/TL}$[10]	$\overline{TxC}$ or $\overline{RxC}$ low		480			
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 150pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[8]	C_L = 150pF		0		ns

NOTES:

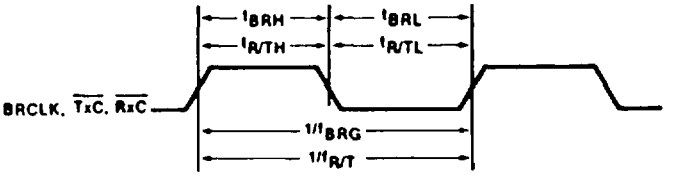
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of 20ns maximum.
6. Typical values are at +25°C, typical supply voltages and typical processing parameters.
7. $\overline{INTR}$ output is open drain.
8. Parameter applies when internal transmitter clock is used.
9. t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL} respectively.
10. In asynchronous local loopback mode, using 1X clock, the following parameters apply:
    $f_{R/T}$ = 0.83MHz max
    $t_{R/TL}$ = 700ns min

TIMING DIAGRAMS

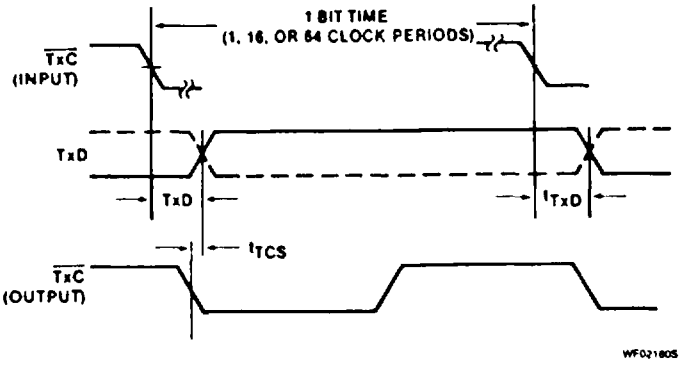
RESET



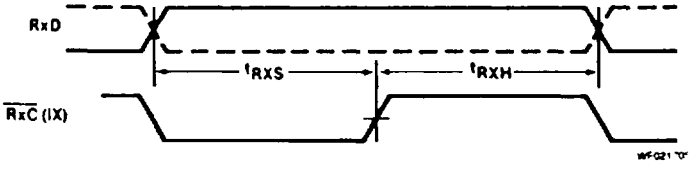
CLOCK



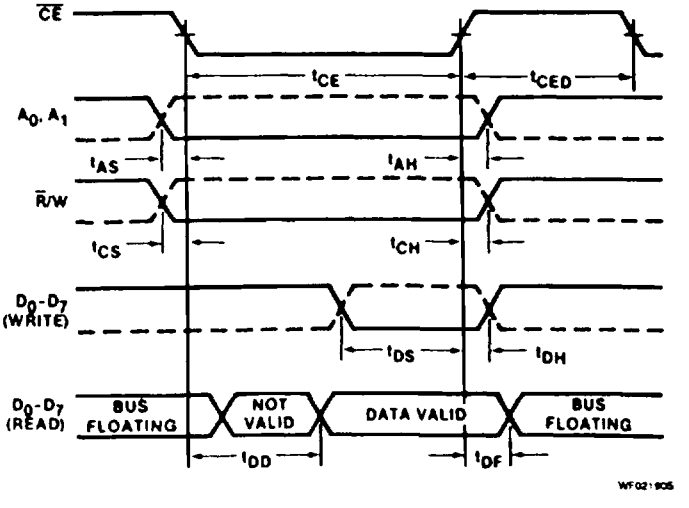
TRANSMIT



RECEIVE

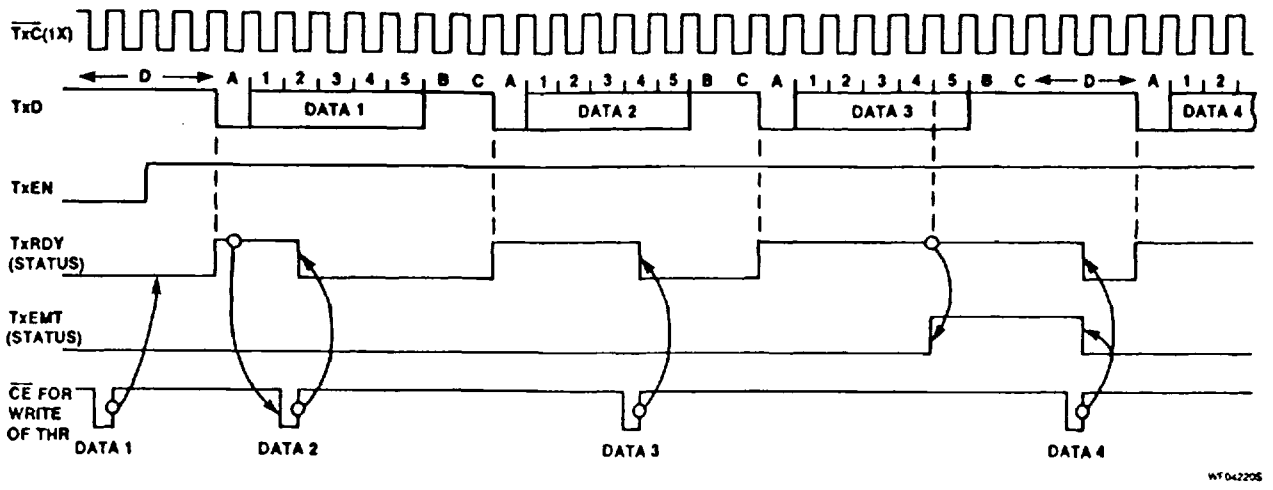


READ AND WRITE



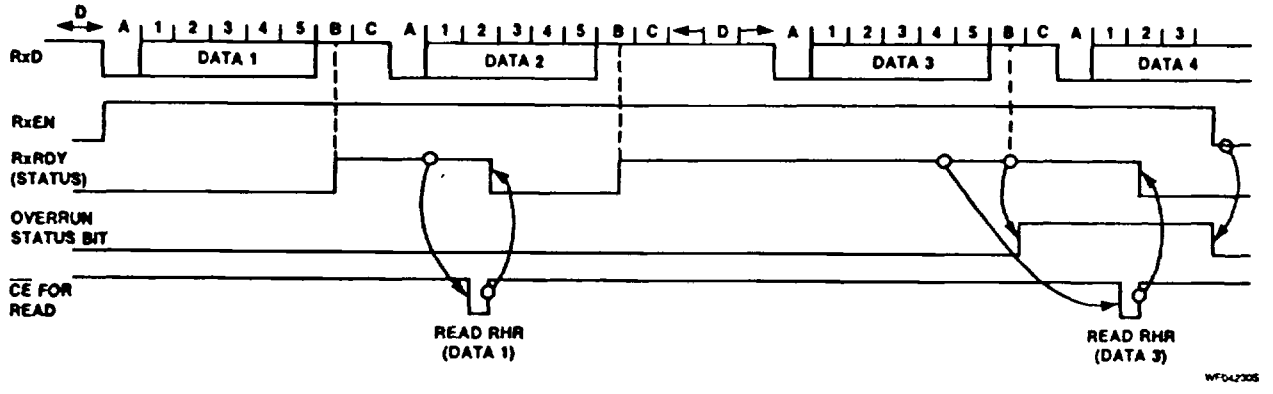
TIMING DIAGRAMS (Continued)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits)



NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

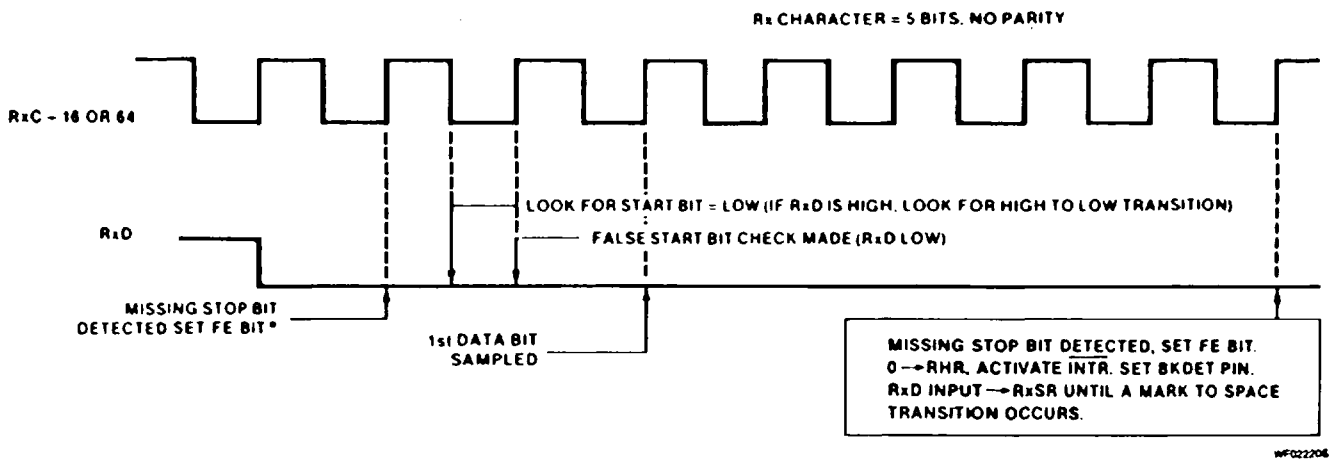
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits)



NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected.

TIMING DIAGRAMS (Continued)

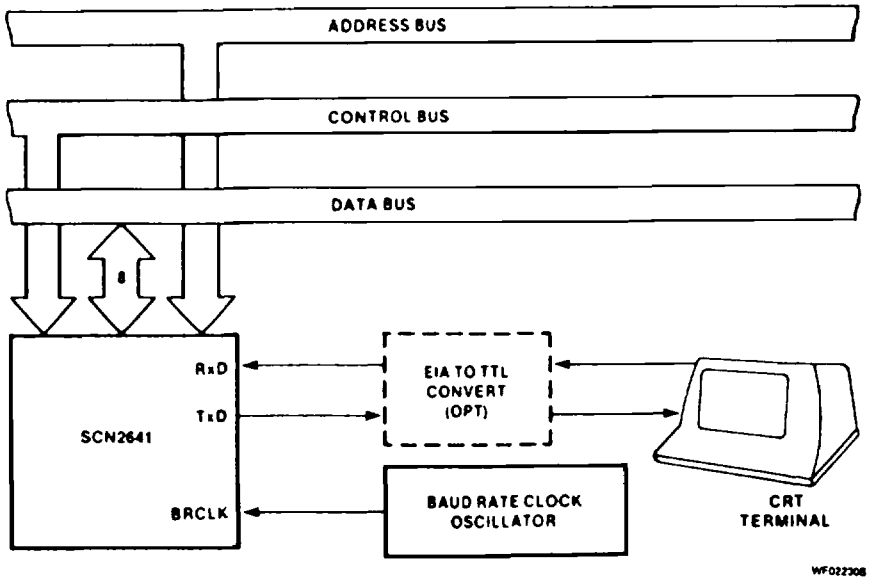
BREAK DETECTION TIMING



*If the stop bit is present, the start bit search will commence immediately.

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL



TYPICAL APPLICATIONS (Continued)

ASYNCHRONOUS INTERFACE TO TELEPHONE LINES