NEC

MOS Integrated Circuit

μPD75P036

4-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD75P036 is a 4-bit signgle-chip microcontroller that replaced the μPD75028's on-chip ROM with one-time PROM or EPROM. Because this device can operate at the same supply voltage as its mask version, it is suited for preproduction in development stage or small-scale production.

The one-time PROM version is programmable only once and is useful for small-scale production of many different products and time-to-market of a new product. The EPROM version is programmable, erasable, and reprogrammable, and is suited for the evaluation of application systems. ★

Detailed functions are described in the followig user's manual. Be sure to read it for designing.

μPD75028 User's Manual: IEU-1280

FEATURES

- μPD75028 compatible
  - At full production, the μPD75P036 can be replaced with the μPD75028 which incorporates mask ROM
- Memory capacity
  - Program memory (PROM): 16256 x 8 bits
  - Data memory (RAM): 1024 x 4 bits
- Internal pull-up resistors can be specified by software: Ports 0-3, 6-8
- Internal pull-down resistors can be specified by software: Port 9
- Open-drain input/output: Ports 4, 5, 10
- Can operate at low voltage: V_{DD} = 2.7 to 6.0 V

ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grade	
μPD75P036CW	64-pin plastic shrink DIP (750 mils)	One-time PROM	Standard	
μPD75P036GC-AB8	64-pin plastic QFP (14 x 14 mm)	One-time PROM	Standard	
μPD75P036KG	64-pin ceramic WQFN	EPROM	Not applicable	★

Caution Internal pull-up/pull-down resistors cannot be specified by mask option as for this device.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on e devices and its recommended applications.

The reliability of the EPROM version, μPD75P036KG, is not guaranteed when used in mass-produced application sets. Please use this device only experimentally or for evaluation during trial manufacture.

The function common to the one-time PROM and EPROM versions is referred to as PROM throughout this document.

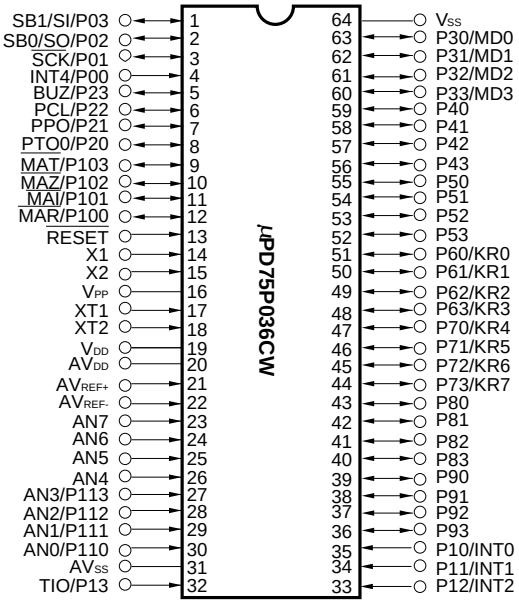
The information in this document is subject to change without notice.

Document No. U10051EJ3V0DS00 (3rd edition)
(Previous No. IC-2967
Date Published September 1995 P
Printed in Japan

The mark ★ shows revised points.

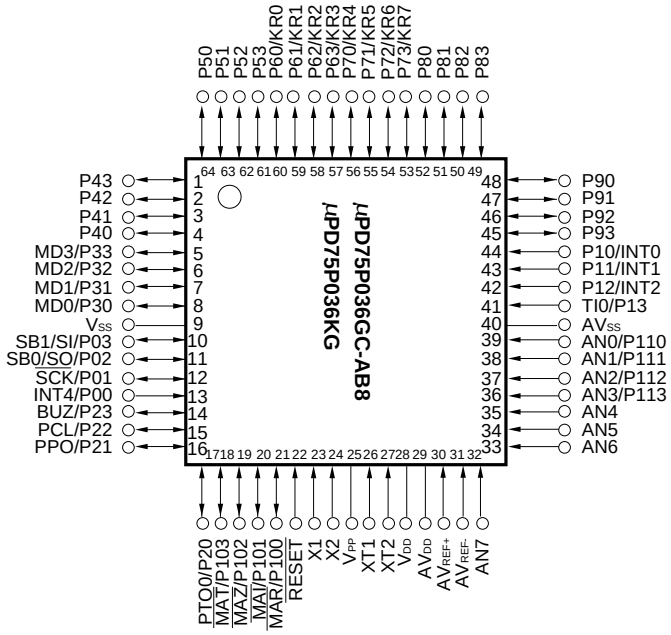
PIN CONFIGURATIONS (Top View)

• 64-pin plastic shrink DIP (750 mils)



• 64-pin plastic QFP (14 x 14 mm)

• 64-pin ceramic WQFN

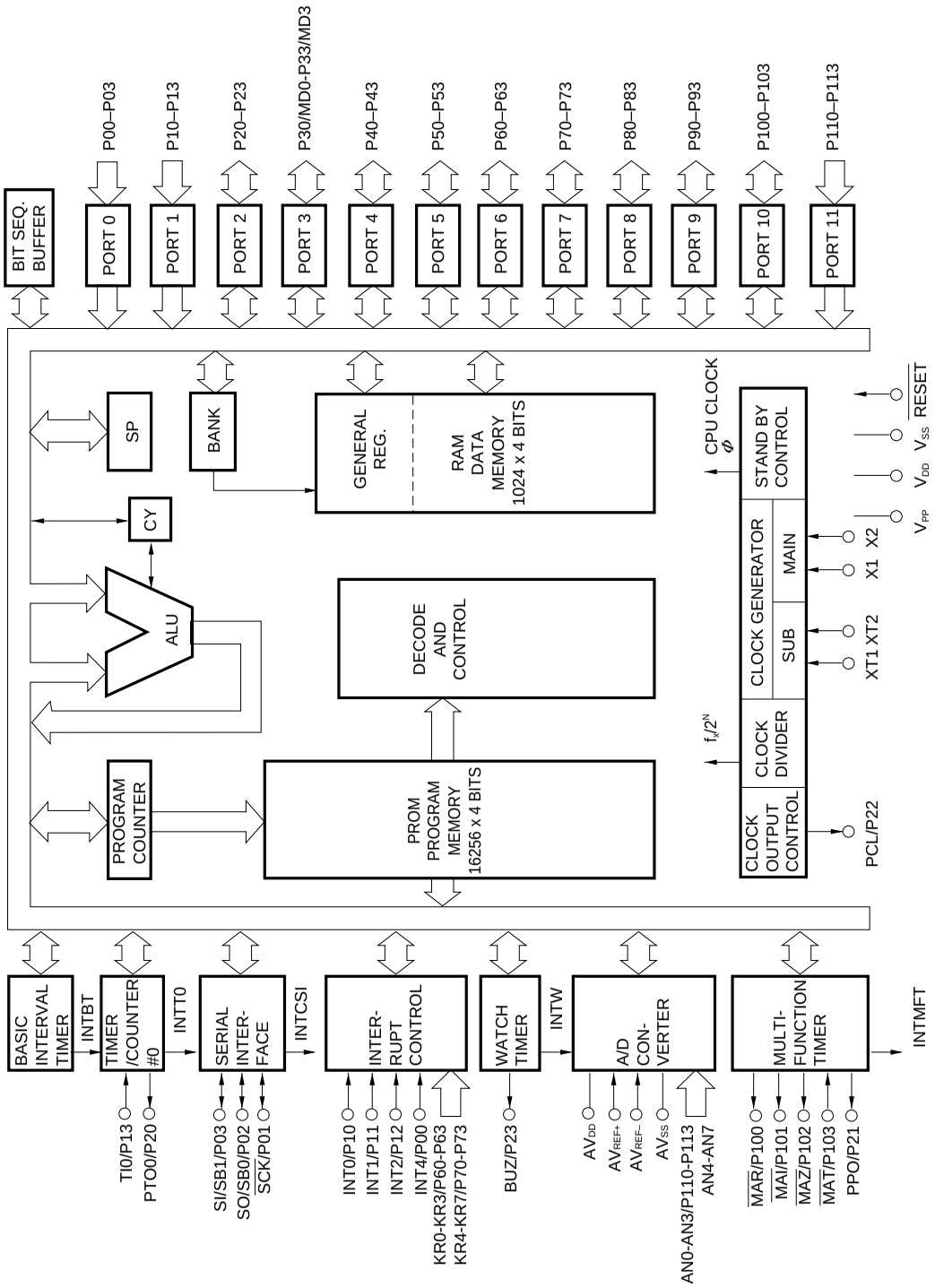


PIN IDENTIFICATION ★

P00-P03	: Port 0	INT0, INT1, INT4	: External Vectored Interrupt	
P10-P13	: Port 1	INT2	: External Test Input	
P20-P23	: Port 2	X1, X2	: Main System Clock Oscillation	
P30-P33	: Port 3	XT1, XT2	: Subsystem Clock Oscillation	
P40-P43	: Port 4	$\overline{MAR}$	: Reference Integration Control	MFT A/D mode
P50-P53	: Port 5			
P60-P63	: Port 6	$\overline{MAI}$	: Integration Control	
P70-P73	: Port 7	$\overline{MAZ}$	: Autozero Control	
P80-P83	: Port 8	$\overline{MAT}$	: External Comparate Timing Input	
P90-P93	: Port 9			
P100-P103	: Port 10	PPO	: Programmable Pulse Output	
P110-P113	: Port 11		⋯ MFT timer mode	
KR0-KR7	: Key Return	AN0-AN7	: Analog Input	
$\overline{SCK}$	: Serial Clock	AV_{REF+}	: Analog Reference (+)	
SI	: Serial Input	AB_{REF-}	: Analog Reference (–)	
SO	: Serial Output	AV_{DD}	: Analog V_{DD}	
SB0, SB1	: Serial Bus	AV_{SS}	: Analog V_{SS}	
$\overline{RESET}$	: Reset Input	V_{DD}	: Positive Power Supply	
TI0	: Timer Input	V_{SS}	: Ground	
PTO0	: Programmable Timer Output	MD0-MD3	: Mode Selection	
BUZ	: Buzzer Clock	V_{PP}	: Programming/Verifying Power Supply	
PCL	: Programmable Clock			

Remark MFT: Multifunction Timer

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins (1/2)

Pin Name	Input/Output	Alternate Function	Function	8-Bit I/O	When Reset	Input/Output Circuit Type Note 1
P00	Input	INT4	4-bit input port (PORT0). Internal pull-up resistors can be specified in 3-bit units for the P01 to P03 pins by software.	No	Input	Ⓑ
P01	Input/Output	$\overline{SCK}$				Ⓕ - A
P02	Input/Output	SO/SB0				Ⓕ - B
P03	Input/Output	SI/SBI				Ⓜ - C
P10	Input	INT0	With noise elimination function	No	Input	Ⓑ - C
P11		INT1	4-bit input port (PORT1). Internal pull-up resistors can be specified in 4-bit units by software.			
P12		INT2				
P13		TI0				
P20	Input/Output	PTO0	4-bit input/output port (PORT2). Internal pull-up resistors can be specified in 4-bit units by software.	No	Input	E - B
P21		PPO				
P22		PCL				
P23		BUZ				
P30 Note 2	Input/Output	MD0	Programmable 4-bit input/output port (PORT3). This port can be specified for input/output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	No	Input	E - B
P31 Note 2		MD1				
P32 Note 2		MD2				
P33 Note 2		MD3				
P40-P43 Note 2	Input/Output		N-ch open-drain 4-bit input/output port (PORT4). Withstands up to 10 V. Data input/output pin for writing and verifying of program memory (PROM) (lower 4 bits).	Yes	Input	M - A
P50-P53 Note 2	Input/Output		N-ch open-drain 4-bit input/output port (PORT5). Withstands up to 10 V. Data input/output pin for writing and verifying of program memory (PROM) (upper 4 bits).		Input	M - A

Notes 1. Circles indicate Schmitt-triggerred inputs.

2. Can directly drive LEDs.

1.1 Port Pins (2/2)

Pin Name	Input/Output	Alternate Function	Function	8-Bit I/O	When Reset	Input/Output Circuit Type Note 1
P60	Input/Output	KR0	Programmable 4-bit input/output port (PORT6). Internal pull-up resistors can be specified in 4-bit units by software.	Yes	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/Output	KR4	4-bit input/output port (PORT7). Internal pull-up resistors can be specified in 4-bit units by software.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				
P80-P83	Input/Output	—	4-bit input/output port (PORT8). Internal pull-up resistors can be specified in 4-bit units by software.	No	Input	E - B
P90-P93	Input/Output	—	4-bit input/output port (PORT9). Internal pull-up resistors can be specified in 4-bit units by software.		Input	E - D
P100	Input/Output	$\overline{\text{MAR}}$	N-ch open-drain 4-bit input/output port (PORT10). Withstands up to 10 V in open-drain mode.	No	Input	M -A
P101		$\overline{\text{MAI}}$				
P102		$\overline{\text{MAZ}}$				
P103		$\overline{\text{MAT}}$				
P110	Input	AN0	4-bit input/output port (PORT11).		Input	Y
P111		AN1				
P112		AN2				
P113		AN3				

Note Circles indicate schmitt-triggerred inputs.

1.2 Non-Port Pins (1/2)

Pin Name	Input/Output	Alternate Function	Function	8-Bit I/O	When Reset	Input/Output Circuit Type Note 1
TI0	Input	P13	External event pulse input pin to timer/event counter		Input	Ⓑ - C
PTO0	Input/Output	P20	Timer/event counter output pin		Input	E - B
PCL	Input/Output	P22	Clock output pin		Input	E - B
BUZ	Input/Output	P23	Fixed frequency output pin (for buzzer or for trimming the system clock)		Input	E - B
$\overline{SCK}$	Input/Output	P01	Serial clock input/output pin		Input	Ⓕ- A
SO/SB0	Input/Output	P02	Serial data output pin Serial bus input/output pin		Input	Ⓕ- B
SI/SB1	Input/Output	P03	Serial data output pin Serial bus input/output pin		Input	Ⓜ- C
INT4	Input	P00	Edge detection vectored interrupt input pin (Either rising or falling edge detection is effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input pin (Detection edge can be selected)		Input	Ⓑ - C
INT1		P11				
INT2	Input	P12	Edge detection testable input pin (rising edge detection)		Input	Ⓑ - C
KR0-KR3	Input/Output	P60-P63	Testable input/output pin (parallel falling edge detection)		Input	Ⓕ - A
KR4-KR7	Input/Output	P70-P73	Testable input/output pin (parallel falling edge detection)		Input	Ⓕ - A
$\overline{MAR}$	Input/Output	P100	In integral A/D converter mode of MFT	Reverse integration signal output pin	Input	M - A
$\overline{MAI}$	Input/Output	P101		Integration signal output pin	Input	M - A
$\overline{MAZ}$	Input/Output	P102		Auto zero signal output pin	Input	M - A
$\overline{MAT}$	Input/Output	P103		Comparator input pin	Input	M - A
PPO	Input/Output	P21	In timer mode of MFT	Timer pulse output pin	Input	E - B

Note Circles indicate Schmitt-triggerred inputs.

Remark MFT: Multifunction timer

1.2 Non-Port Pins (2/2)

Pin Name	Input/Output	Alternate Function	Function		When Reset	Input/Output Circuit Type Note 1
AN0-AN3	Input	P110-P113	Pins only for A/D converter	8-bit analog input pin.	—	Y
AN4-AN7		—				Y - A
AV_{REF+}	Input	—		Reference voltage input pin (AV_{DD} side).	—	Z - A
AV_{REF-}	Input	—		Reference voltage input pin (AV_{SS} side).	—	Z - A
AV_{DD}	—	—		Positive power supply pin.	—	—
AV_{SS}	—	—		GND potential pin.	—	—
X1, X2	Input	—	Crystal or ceramic resonator connection for main system clock generation. To use external clock, input the external clock to X1 and its reverse phase to X2.		—	—
XT1, XT2	Input	—	Crystal or ceramic resonator connection for subsystem clock generation. To use external clock, input the external clock to XT1 and its reverse phase to XT2. XT1 can be used as a 1-bit input (test) pin.		—	—
$\overline{RESET}$	Input	—	System reset input pin.		—	Ⓑ
MD0/MD3	Input/Output	P30-P33	Mode selection pins in program memory (PROM) write/verify mode.		Input	E - B
V_{PP} Note 2	—	—	Program voltage application pin in program memory (PROM) write/verify mode. At normal operation, connect the pin to V_{DD} directly. In the PROM write/verify mode, apply +12.5 V.		—	—
V_{DD}	—	—	Positive power supply pin.		—	—
V_{SS}	—	—	GND potential pin.		—	—

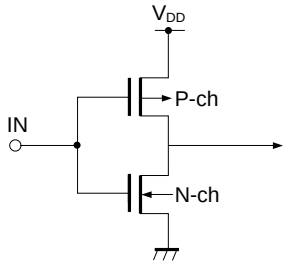
Notes 1. Circles indicate schmitt trigger inputs.

2. If the V_{PP} pin is not connected directly to the V_{DD} pin at normal operation, the μPD75P036 does not operate normally.

1.3 Pin Input/Output Circuits

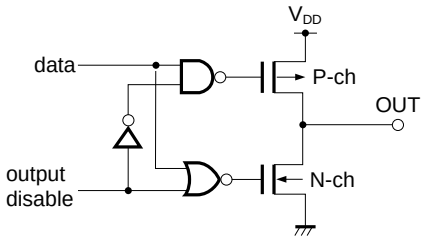
The following shows a simplified input/output circuit diagram for each pin of the μPD75P036.

TYPE A (for TYPE E - B)



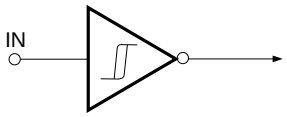
CMOS-level input buffer

TYPE D (for TYPE E - B, F - A)



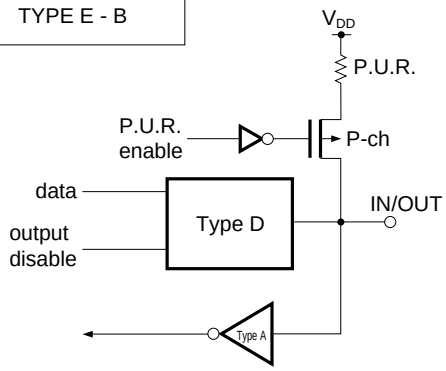
Push-pull output that can be set in an output high-impedance state (both P-ch and N-ch are off)

TYPE B



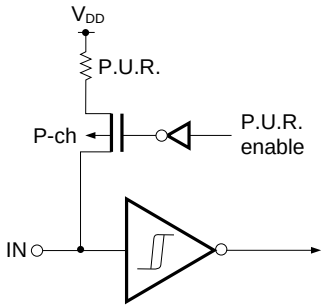
Schmitt-triggerred input with hysteresis characteristics

TYPE E - B



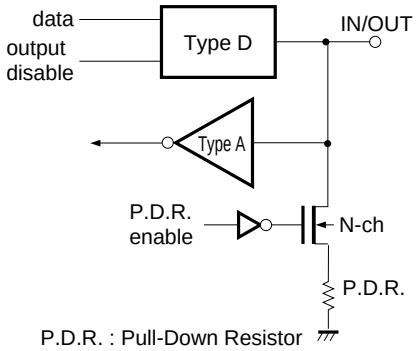
P.U.R. : Pull-Up Resistor

TYPE B - C



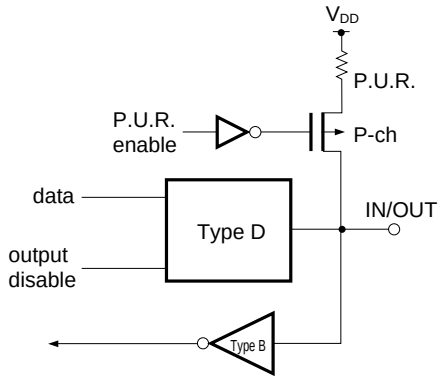
P.U.R. : Pull-Up Resistor

TYPE E - D



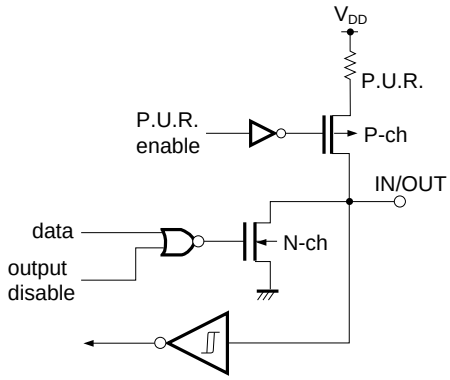
P.D.R. : Pull-Down Resistor

TYPE F - A



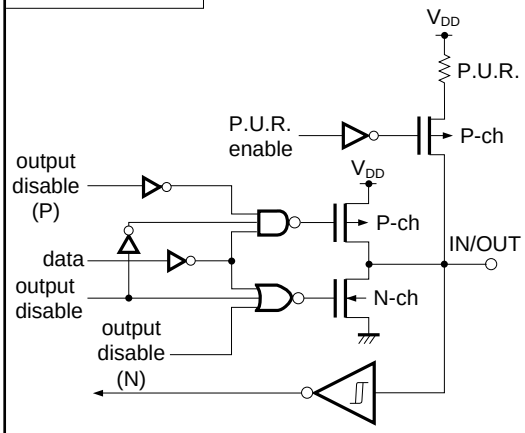
P.U.R. : Pull-Up Resistor

TYPE M - C



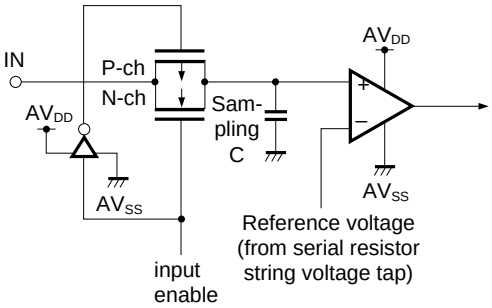
P.U.R. : PullUp Resistor

TYPE F - B

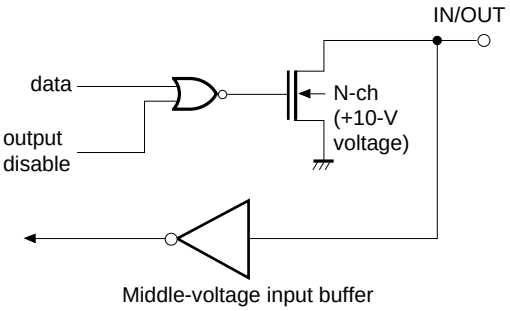


P.U.R. : Pull-Up Resistor

TYPE Y



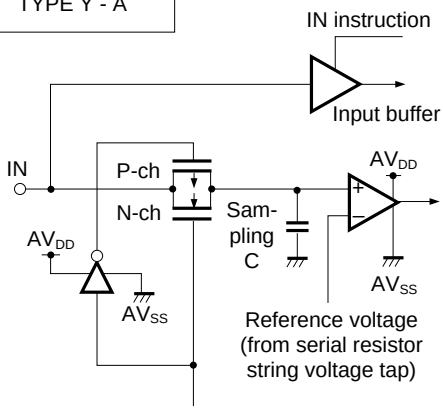
TYPE M - A

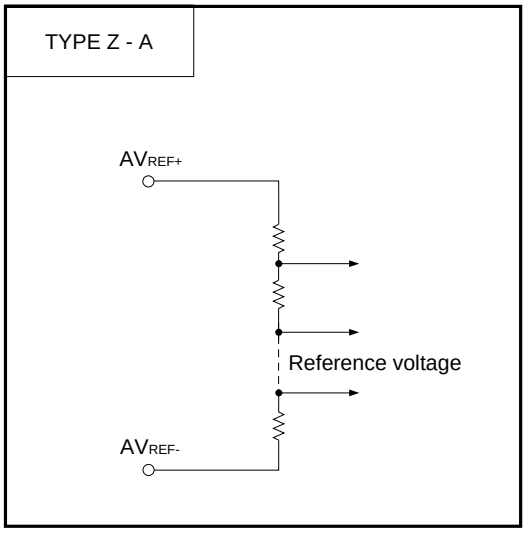


Middle-voltage input buffer (withstands up to + 10 V)

P.U.R. : Pull-Up Resistor

TYPE Y - A




TYPE Z - A
AVREF+
Reference voltage
AVREF-

1.4 Recommended Connection of Unused Pins ★

Pin Name	Recomended Connecting Method
P00/INT4	Connect to V_{SS}.
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}.
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}.
P13/TI0	
P20/PTO0	Input state: Independently connect to V_{SS} or V_{DD} via a resistor. Output state: Leave Open.
P21/PPO	
P22/PCL	
P23/BUZ	
P30/MD0-P33/MD3	
P40-P43	
P50-P53	
P60/KR0-P63/KR3	
P70/KR4-P73/KR7	
P80-P83	
P90-P93	
P100/$\overline{MAR}$	
P101/$\overline{MAI}$	
P102/$\overline{MAZ}$	
P103/$\overline{MAT}$	
P110/AN0-P113/AN3	Connect to V_{SS} or V_{DD}.
AN4-AN7	
AV_{REF+}	Connect to V_{SS}.
AV_{REF-}	
AV_{SS}	
AV_{DD}	Connect to V_{DD}.
XT1	Connect to V_{SS} or V_{DD}.
XT2	Leave Open.
V_{PP}	Connect directly to V_{DD}.

2. MEMORY

2.1 Differences between μPD75P036 and μPD75028/75036

The μPD75P036 is a microcontroller provided by replacing the μPD75028's on-chip mask ROM with one-time PROM or EPROM. Capacity of program memory and data memory are different, but CPU function and internal hardware are identical. Table 2-1 shows the differences between the μPD75P036 and μPD75028/75036. Users should fully consider these differences especially when debugging or producing an application system on an experimental basis by using the PROM version and then mass-producing the system using the mask ROM version.

For details about the CPU function and the internal hardware, refer to **μPD75028 User's Manual (IEM-1280)**.

★ **Table 2-1. Differences between μPD75P036 and μPD75028/75036**

Item		μPD75P036	μPD75028	μPD75036
Program memory		One-time PROM/EPROM	Mask ROM	
		0000H-3F7FH (16256 x 8 bits)	0000H-1F7FH (8064 x 8 bits)	0000H-3F7FH (16256 x 8 bits)
Data memory		000H-3FFH (1024 x 4 bits)	000H-1FFH (512 x 4 bits)	000H-3FFH (1024 x 4 bits)
Pull-up resistor	Ports 0-3, 6-8	Can be specified by software.		
	Ports 4, 5, 10	Not provided	Can be connected by mask option	
Pull-down resistor	Port 9	Can be specified by software.		
XT1 feedback resistor		Provided on-chip	Can be disconnected by mask option	
Supply voltage		V_{DD} = 2.7 to 6.0 V		
Pin connection	Pin 16 (SDIP)	V_{PP}	Internally connected	
	Pin 25 (QFP)			
	Pins 60-63 (SDIP)	P33/MD3-P30/MD0	P33-P30	
	Pins 5-8 (QFP)			
Electrical specifications		Supply current and operating temperature ranges differ between μPD75P036 and μPD75028/75036. For details, refer to the electrical specifications described in Data Sheet of each model.		
Others		Noise immunity and noise radiation differ because circuit complexity and mask layout are different.		

Caution The noise immunity and noise radiation differ between the PROM and mask ROM versions. To replace the PROM version with the mask ROM version in the course of experimental production to mass production, evaluate your system by using the CS version (not ES) of the mask ROM version.

2.2 Program Memory (ROM) ··· 16256 words x 8 bits

The program memory is a 16256-word x 8-bit PROM and stores programs, table data, etc.

The program memory is accessed by referencing the program counter contents. Table data can be referenced by executing a table look-up instruction (MOVT).

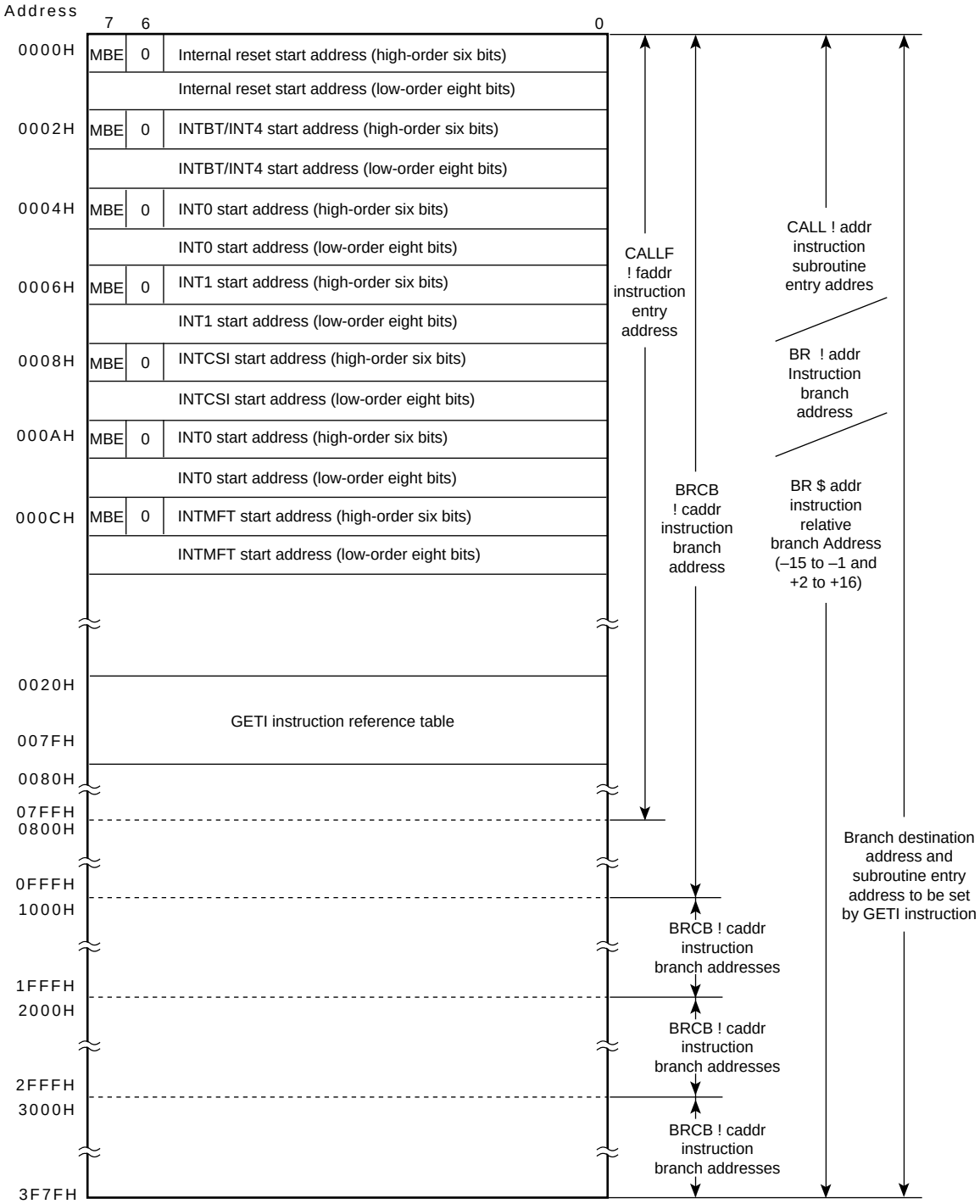
Figure 2-1 shows the address range in which a branch can be taken by branch instructions and subroutine call instructions. A relative branch instruction (BR $addr) enables a branch to addresses [PC value –15 to –1, +2 to +16] regardless of block boundaries.

Program memory addresses are 0000H-3F7FH and the following addresses are assigned to special purposes: (All areas except 0000H or 0001H can be used as normal program memory.)

- Addresses 0000H-0001H
  Vector table into which the program start address and MBE setting value when the $\overline{\text{RESET}}$ signal is generated are written.
  Processing at reset is started at any desired address.
- Addresses 0002H-000DH
  Vector table into which the program start address and MBE setting value when each vectored interrupt is generated are written.
  Interrupt servicing can be started at any desired address.
- Addresses 0020H-007FH
  Table area referenced by the GETI instruction[Note].

Note The GETI instruction is provided to execute any 2-byte or 3-byte instruction or two 1-byte instructions as a 1-byte instruction; it is used to reduce the number of program steps.

Figure 2-1. Program Memory Map



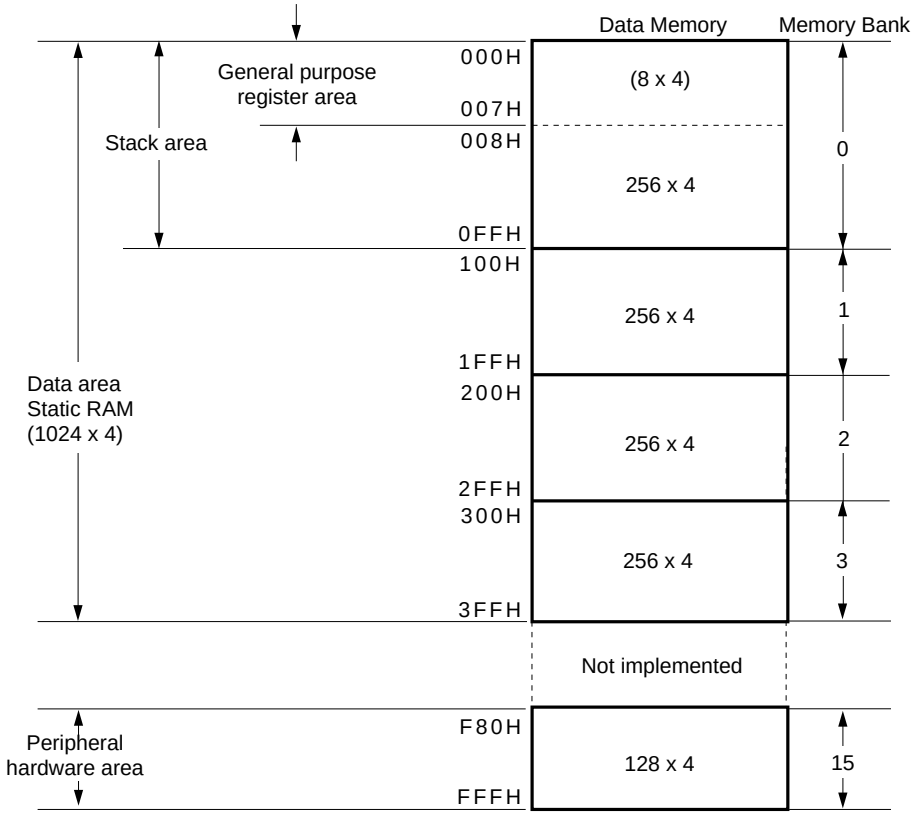
2.3 Data Memory (RAM)

The data memory consists of a data area and a peripheral hardware area as shown in Figure 2-2.

The data memory consists of banks, each consisting of 256 words x 4 bits, and the following memory banks can be used:

- Memory banks 0-3 (data area)
- Memory bank 15 (peripheral hardware area)

Figure 2-2. Data Memory Map



(1) Data area

The data area consists of static RAM and is used to store process data and as stack memory when a (subroutine) or an interrupt is executed. Even when CPU operation is stopped in the standby mode, the memory contents can be retained for hours with battery backup, etc. The data area is manipulated by executing memory manipulation instructions.

The static RAM is mapped each 256 x 4 bits in memory banks 0-3. Bank 0 is mapped as a data area; it can also be used as a general purpose register area (000H-007H) and a stack area (000H-0FFH).

One address of the static RAM consists of four bits; however it can be manipulated in 8-bit units by executing 8-bit memory manipulation instructions and bit-wise by executing bit manipulation instructions. To execute an 8-bit memory manipulation instruction, specify an even address.

(a) General purpose register area

Can be handled by executing general purpose register and memory manipulation instructions. A maximum of eight 4-bit registers can be used. The portions of the eight general purpose registers not used by a program can be used as a data area or stack area.

(b) Stack area

Is set by an instruction and can be used as a save area when a subroutine is executed or interrupt servicing is performed.

(2) Peripheral hardware area

The peripheral hardware area is mapped in addresses F80H-FFFH of memory bank 15.
Like the static memory, the peripheral hardware area is handled by executing memory manipulation instructions. However, the bit units in which the peripheral hardware can be manipulated vary depending on the address. Addresses in which the peripheral hardware is not mapped do not contain data memory and cannot be accessed.

3. WRITING AND VERIFYING PROM (PROGRAM MEMORY)

The program memory incorporated in the μPD75P036 is a 16256 x 8-bit electrically writable PROM. The pins as listed in the table given below are used for write and verification of the PROM. No address is input; instead, an address is updated by inputting a clock from the X1 pin.

Pin Name	Function
V_{PP}	Applies voltage when program memory is written/verified (normally, at V_{DD} potential)
X1, X2	These pins input clock that updates address when program memory is written/verified. To X2 pin, input X1's signal reverse phase.
MD0-MD3 (P30-P33)	These pins select operation mode when program memory is written/verified.
P40-P43 (Lower 4) P50-P53 (Upper 4)	These pins input/output 8-bit data when program memory is written/verified.
V_{DD}	Power supply voltage application pin. Apply 2.7 to 6.0 V to this pin during normal operation and 6 V when program memory is written/verified.

Cautions 1. Always cover the erasure window of the μPD75P036KG with an opaque film except when the contents of the EPROM are erased. ★

2. The one-time PROM version μPD75P036CW/GC is not equipped with a window, and therefore, the contents of the program memory of this model cannot be erased by exposing it to ultraviolet rays.

3.1 Operation Modes For Writing/Verifying Program Memory

When +6V is applied to the V_{DD} pin of the μPD75P036 with +12.5V applied to the V_{PP} pin, the μPD75P036 is set in the program memory write/verify mode. In this mode, the following operation modes can be set by using the MD0-MD3 pins. At this time, all remaining pins are set to the V_{SS} potential with pull-down resistors.

Operating Mode Specification						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

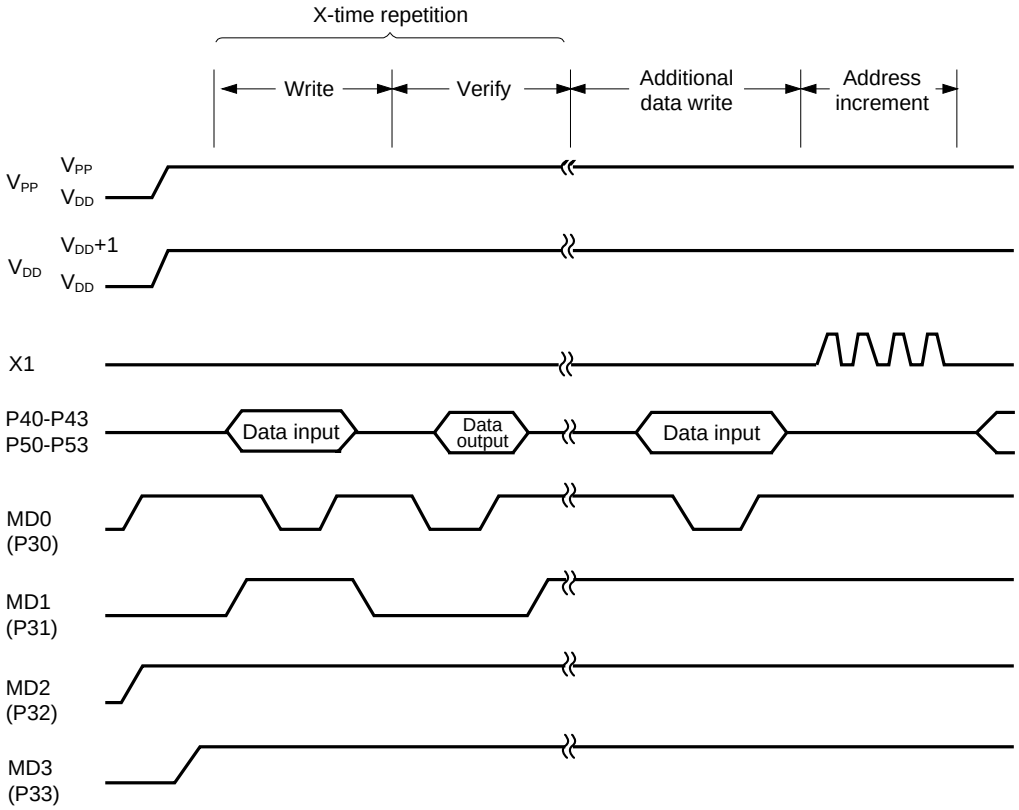
x: L or H

3.2 Program Memory Write Procedure

The program memory write procedure is as follows. High-speed program memory write is possible.

(1) Connect the unused pins to V_{SS} via pull-down resistors. The X1 pin must be low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Set program inhibit mode.
(9) Set verify mode. If data has been written connectly, proceed to step (10). If data has not yet been written, repeat steps (7) to (9).
(10) Write additional data for (the number of times data was written (X) in steps (7) to (9)) times 1 ms.
(11) Set program inhibit mode.
(12) Supply a pulse to the X1 pin four times to update the program memory address by 1.
(13) Repeat steps (7) to (12) to the last address.
(14) Set program memory address 0 clear mode.
(15) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power supply.

Steps (2) to (12) are illustrated below.

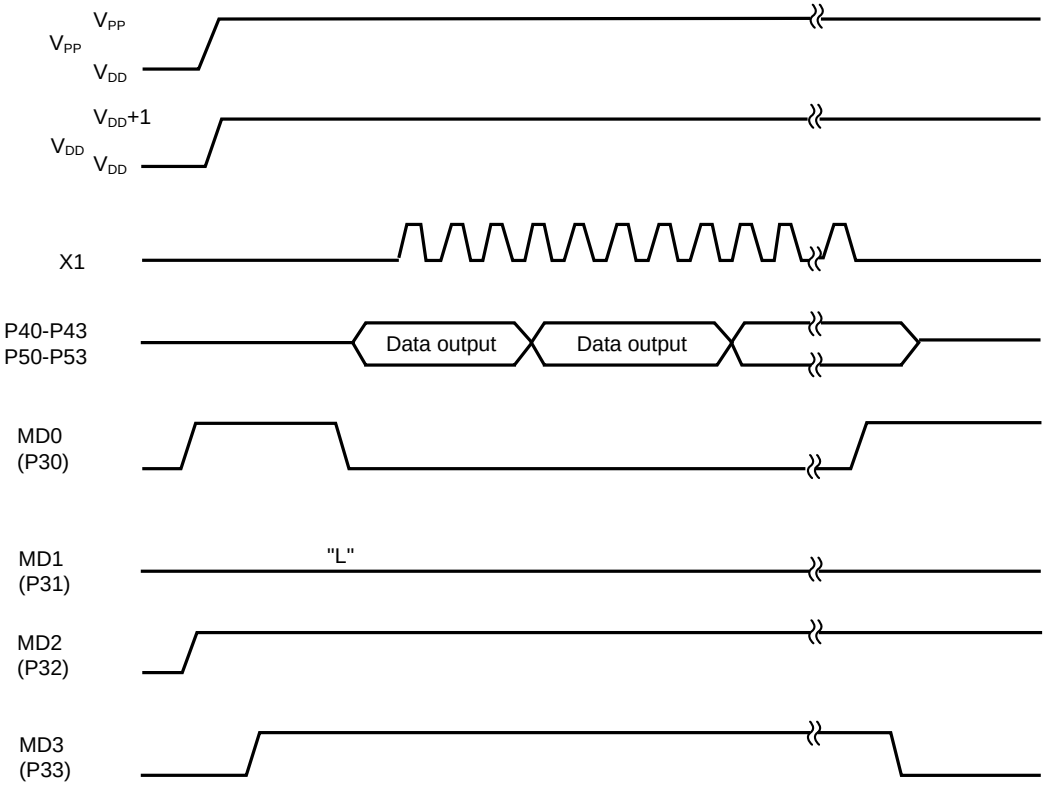


3.3 Program Memory Read Procedure

The μPD 75P036 program memory contents can be read in the following procedure. Read operation should be performed in the verify mode.

(1) Connect the unused pins to V_{SS} via pull-down resistors. The X1 pin must be low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Set verify mode. Data of each address is sequentially output each time a clock pulse is input to the X1 pin four times.
(8) Set program inhibit mode.
(9) Set program memory address 0 clear mode.
(10) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power supply.

Steps (2) to (9) are illustrated below.



★ **3.4 Erasure (μPD75P036KG only)**

The contents of the data programmed to the μPD75P036 can be erased by exposing the window to ultraviolet rays.

The wavelength of the ultraviolet rays used to erase the contents is about 250 nm, and the quantity of the ultraviolet rays necessary for complete erasure is 15 W•s/cm^2 (= ultraviolet ray intensity x erasure time).

When a commercially available ultraviolet ray lamp (wavelength: 254 nm, intensity: 12 mW/cm^2) is used, about 15 to 20 minutes is required.

Cautions 1. The contents of the program memory may be erased if the μPD75P036 is exposed for a long time to direct sunlight or a fluorescent light. To protect the contents from being erased, mask the window with the opaque film. NEC attaches quality-tested opaque film to the UV EPROM products for shipping.

2. To erase the memory contents, the distance between the ultraviolet ray lamp and the μPD75P036 should be 2.5 cm or less.

Remark The time required for erasure changes depending on the degradation of the ultraviolet ray lamp and the surface condition (dirt) of the window.

4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V ★
Input voltage	V_{I1}	Other than ports 4, 5, or 10		–0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5 and 10	Open-drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD}+0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		All pins		–30	mA
Output current, low	I_{OL} Note	Ports 0, 3, 4 and 5	peak value	30	mA
		Per pin	r.m.s. value	15	mA
		Other than ports	peak value	20	mA
		0, 3, 4 and 5	r.m.s. value	5	mA
		Per pin			
		Total for ports 0, 3-9, 11	peak value	170	mA
			r.m.s. value	120	mA
		Total for 0, 2, 10	peak value	30	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +70	°C
Storage temperature	T_{stg}			–65 to +150	°C

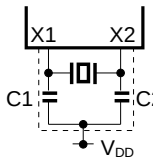
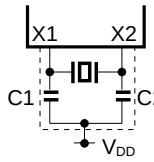
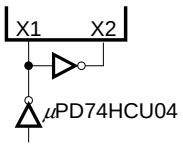
Note r.m.s. values should be calculated as follows: [r.m.s. value] = [peak value] x $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded. ★

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			15	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillator Characteristics (T_A = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Constants	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	2.0		5.0 Note 3	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscilaltion frequency (f_X) Note 1		2.0	4.19	5.0 Note 3	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) Note 1		2.0		5.0 Note 3	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		100		250	ns

Notes 1. The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator. For instruction execution time, refer to AC Characteristics.

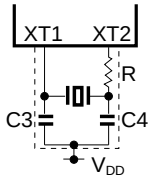
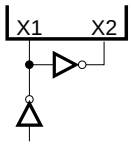
2. Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range or the STOP mode has been released.

3. When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

★ **Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

Subsystem Clock Oscillator Characteristics (T_A = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Constants	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_X) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		X1 input frequency (f_X) Note 1		32		100	kHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		5		15	μs

Notes 1. The oscillation frequency and XT1 input frequency are indicated only to express the characteristics of the oscillator. For instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Cautions When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity: ★

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock circuit is influenced by noise more easily than the main system clock oscillation circuit. When using th subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC Characteristics (T_A = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Ports 2, 3, 8, 9, 11		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5, 10	Open-drain	0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD}–0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Ports 2 to 5, 8 to 11		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1, XT2		0		0.4	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage, low	V_{OL}	Ports 3, 4, 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0, 1	Open-drain Pull-up Resistor ≥ 1 kΩ			0.2V_{DD}	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 9 V	Ports 4, 5, 10 (Open-drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Input leakage current, high	I_{LOH1}	V_O = V_{DD}				3	μA
	I_{LOH2}	V_O = 9 V	Ports 4, 5, 10 (Open-drain)			20	μA
Input leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Internal pull-up resistor	R_{UI}	Ports 0, 1, 2, 3, 6, 7, 8 (except P00) V_I = V_{DD}	V_{DD} = 5.0 V ± 10 %	15	40	80	kΩ
			V_{DD} = 3.0 V ± 10 %	30		300	kΩ
Internal pull-down resistor	R_D	Port 9 V_I = V_{DD}	V_{DD} =5.0 V ± 10 %	10	40	70	kΩ
			V_{DD} = 3.0 V ± 10 %	10		60	kΩ

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD1}	4.19 MHz Crystal oscillator [Note 2] C1 = C2 = 22 pF	V_{DD} = 5 V ± 10% [Note 3]			4.5	14	mA
			V_{DD} = 3 V ± 10% [Note 4]			0.9	3	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ± 10%		700	2100	μA
				V_{DD} = 3 V ± 10%		300	900	μA
	I_{DD3}	32.768 kHz Crystal oscillator [Note 5]	Operating mode	V_{DD} = 3 V ± 10%		100	300	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ± 10%		20	60	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ± 10%			0.5	20	μA
			V_{DD} = 3 V ± 10%			0.1	10	μA
				T_A = 25°C		0.1	5	μA
	I_{DD6}	32.768 kHz Crystal oscillator STOP mode	V_{DD} = 3 V ± 10% [Note 6]			5	15	μA

Notes 1. Currents for the internal pull-up resistor are not included.

2. Including when the subsystem clock is operated.

3. High-speed mode operation (when processor clock control register (PCC) is set to 0011).

4. Low-speed mode operation (when PCC is set to 0000).

5. When operated with the subsystem clock by setting the system clock control register (SCC) to SCC3 = 1 and SCC0 = 0 to stop the main system clock operation.

6. When subsystem clock is operated by executing STOP instruction during main system clock operation.

AC CHARACTERISTICS (T_A = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

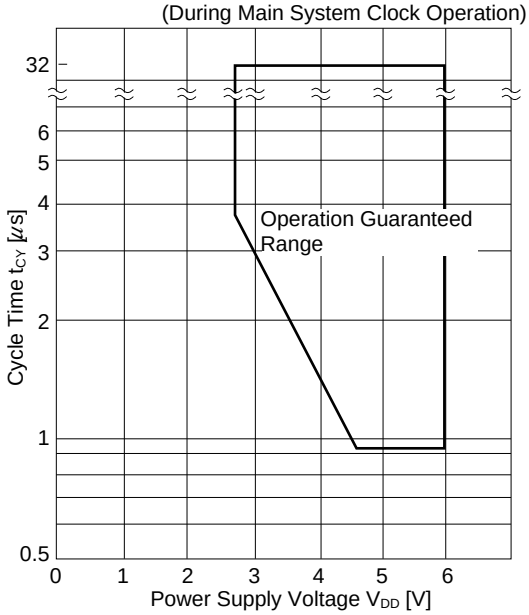
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note 1 (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.95		32	μs
				3.8		32	μs
		Operating on subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high-, low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high-, low-level widths	t_{INTH}, t_{INTL}	INT0		**Note 2**			μs
		INT1, 2, 4		10			μs
		KR0 - 7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC). The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2. $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}

(During Main System Clock Operation)



SERIAL TRANSFER OPERATION

Two-Wire and Three-Wire Serial I/O Modes ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit	
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns	
				3800			ns	
$\overline{SCK}$ high-, low-level widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		(t_{KCY1}/2)–50			ns	
	t_{KH1}			(t_{KCY1}/2)–150			ns	
SI setup time (to $\overline{SCK}$ ↓)	t_{SIK1}			150			ns	
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI1}			400			ns	
SO output delay time from $\overline{SCK}$ ↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		250	ns	★
				0		1000	ns	★

Two-Wire and Three-Wire Serial I/O Modes ($\overline{SCK}$: external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit	
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns	
				3200			ns	
$\overline{SCK}$ high-, low-level widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns	
	t_{KH2}			1600			ns	
SI setup time (to $\overline{SCK}$ ↓)	t_{SIK2}			100			ns	
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}			400			ns	
SO output delay time from $\overline{SCK}$ ↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns	★
				0		1000	ns	★

Note R_L and C_L are load resistance and load capacitance of the SO output line.

SBI Mode ($\overline{SCK}$: internal clock output (master))

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-/low-level widths	t_{KL3}	V_{DD} = 4.5 to 6.0 V		(t_{KCY3}/2)–50			ns
	t_{KH3}			(t_{KCY3}/2)–150			ns
SB0, 1 Setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SB0}$, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

SBI Mode ($\overline{SCK}$: external clock output (master))

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level widths	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are load resistance and load capacitance of the SO output line.

A/D Converter (T_A = –40 to +70°C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Absolute accuracy Note 1		2.5 V ≤ AV_{REF+} ≤ AV_{DD}	–10 ≤ T_A ≤ 70 °C			±1.5	LSB
			–40 ≤ T_A ≤ –10 °C			±2.0	LSB
Conversion time Note 2	t_{CONV}					168/f_x	μs
Sampling time Note 3	t_{SAMP}					44/f_x	μs
Analog input voltage	V_{IAN}			AV_{REF-}		AV_{REF+}	V
Analog supply voltage	AV_{DD}			2.5		V_{DD}	V
Reference input voltage Note 4	AV_{REF+}	2.5 V ≤ (AV_{REF+}) – (AV_{REF-})		2.5		AV_{DD}	V
Reference input voltage Note 4	AV_{REF-}	2.5 V ≤ (AV_{REF+}) – (AV_{REF-})		0		1.0	V
Analog input high impedance	R_{AN}				1000		MΩ
AV_{REF} current	AI_{REF}				0.35	2.0	mA

Notes 1. Absolute accuracy from which quantization error (±1/2 LSB) is removed.

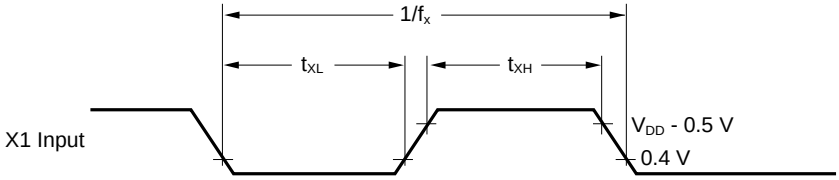
2. Time until conversion end (EOC = 1) after conversion start instruction execution (40.1 μs: Operation at fx = 4.19 MHz).

3. Time until sampling end after conversion start instruction execution (10.5 μs: Operation at fx = 4.19 MHz).

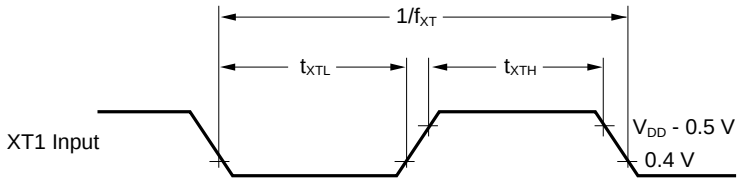
4. (AV_{REF+}) – (AB_{REF-}) should be 2.5 V or more.

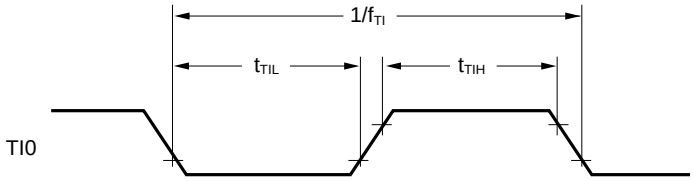
AC Timing Test Point (excluding X1 and XT1 inputs)

Clock Timing



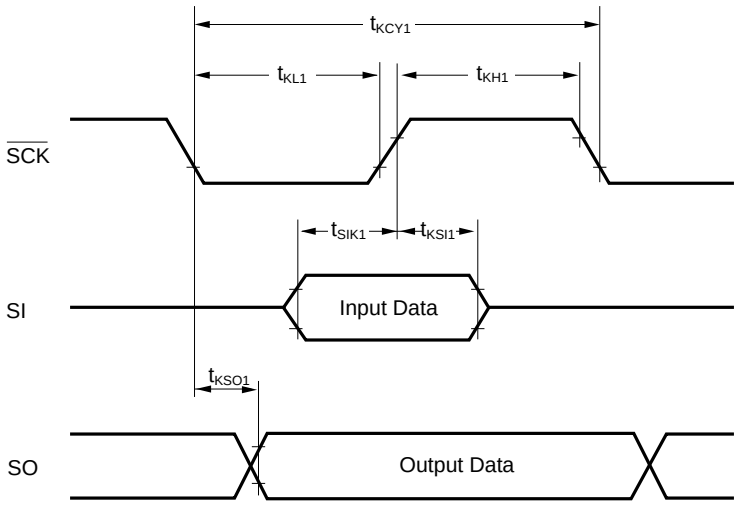
TI0 Timing



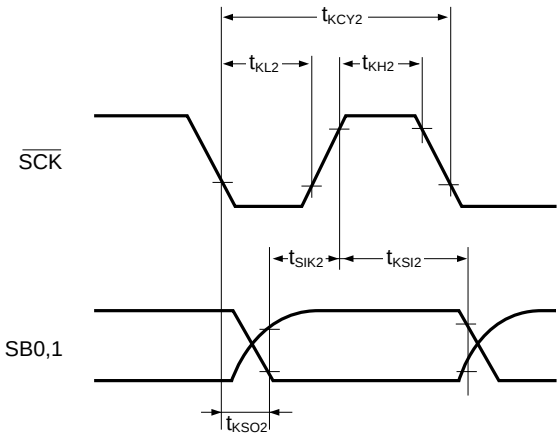


Serial Transfer Timing

Three-Wire Serial I/O Mode:

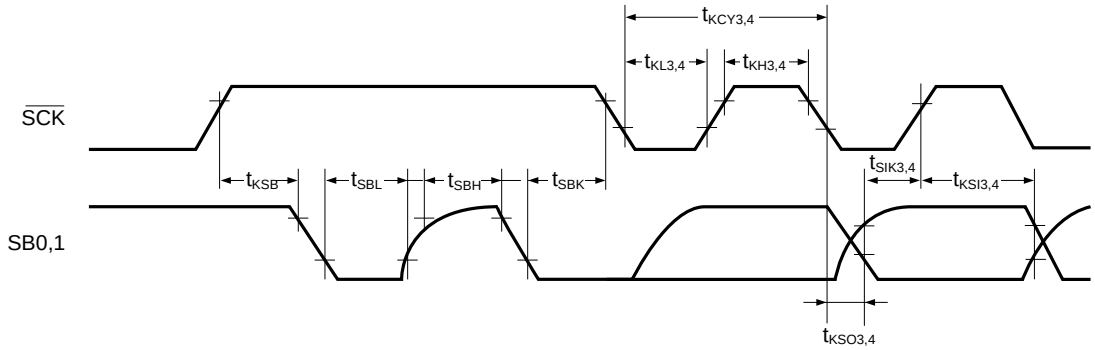


Two-Wire Serial I/O Mode:

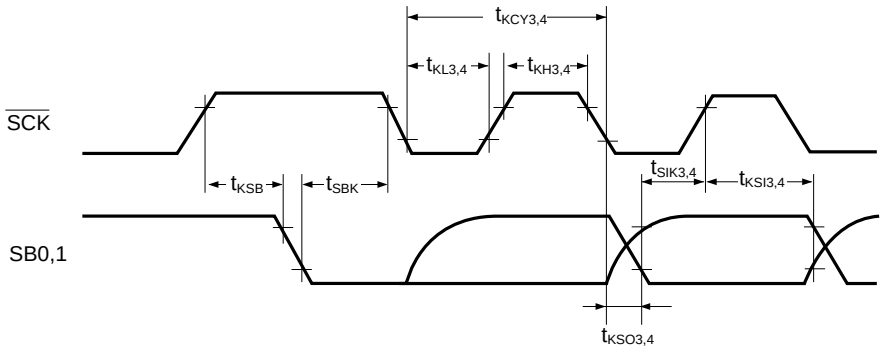


Serial Transfer Timing

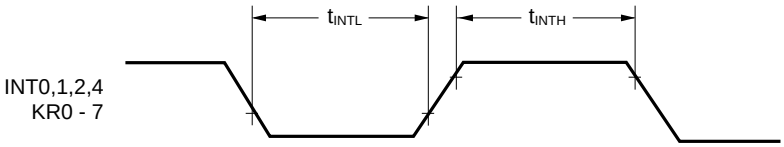
Bus Release Signal Transfer



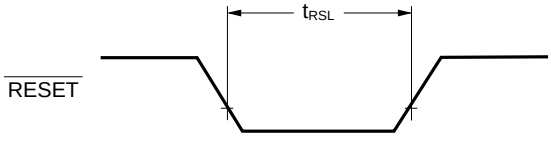
Command Signal Transfer



Interrupt Input Timing



$\overline{RESET}$ Input Timing



Data Memory STOP Mode: Low-voltage Data Retention Characteristics (T_A = –40 to +70 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current Note 1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_x$		ms
		Released by interrupt		**Note 3**		ms

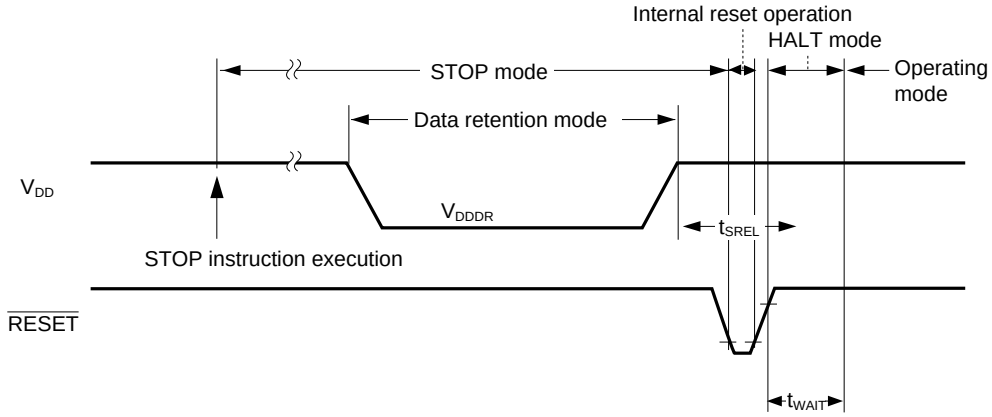
Notes 1. Does not include current in the internal pull-up resistor

2. The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

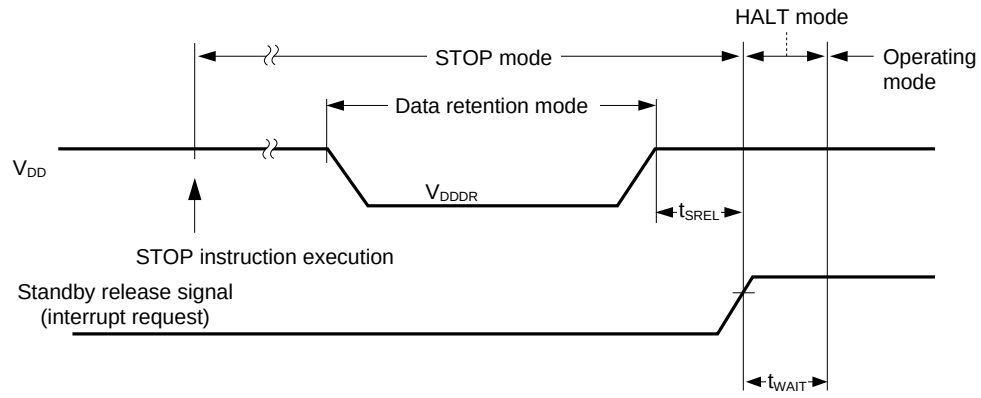
3. Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_x = 4.19 MHz
—	0	0	0	$2^{20}/f_x$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_x$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_x$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_x$ (approx. 1.95 ms)

Data Retention Timing (releasing STOP mode by RESET)



Data Retention Timing (standby release signal: releasing STOP mode by interrupt)



★ **DC Programming Characteristics** (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Other than X1 or X2	0.7V_{DD}		V_{DD}	V
	V_{IH2}	X1 and X2	V_{DD}–0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Other than X1 or X2	0		0.3V_{DD}	V
	V_{IL2}	X1 and X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage, high	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Output voltage, low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. V_{PP} must not exceed +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP} and disconnect it after V_{PP}.

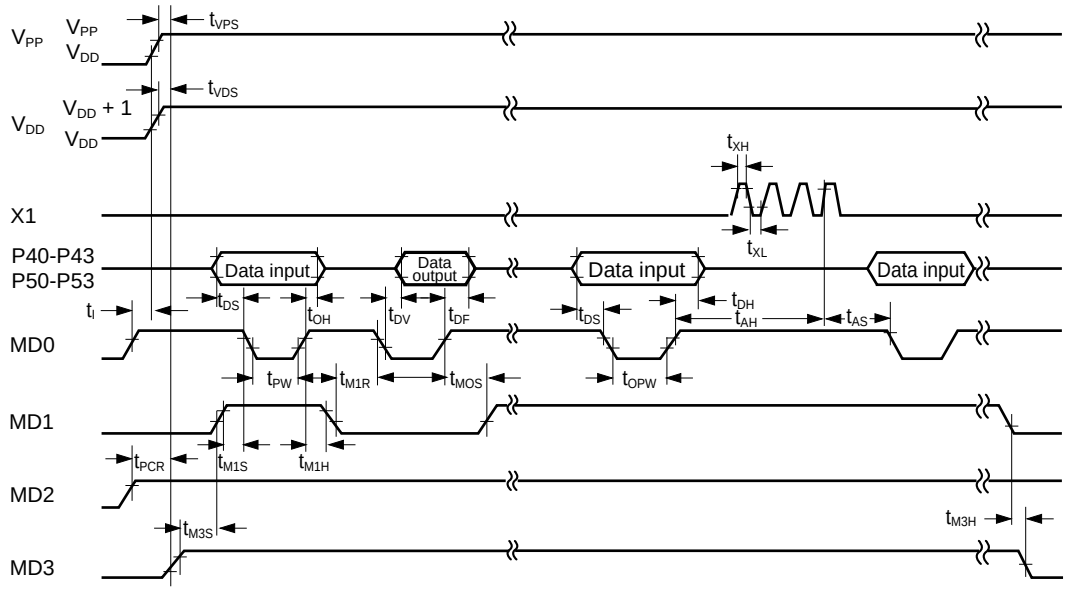
★ **AC Programming Characteristics** (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time **Note 2** (to MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time **Note 2** (from MD0 ↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0 ↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD0 ↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initialized program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1 ↑)	t_{MOS}	t_{CES}		2			μs
Data output delay time from MD0 ↓	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0 ↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-/low-level width	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode set time	t_I	—		2			μs
MD3 setup time (to MD1 ↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1 ↓)	t_{M3H}	—		2			μs
MD3 setup time (from MD0 ↓)	t_{M3SR}	—	When data is read from program memory	2			μs
Address **Note 2** to data output delay time	t_{DAD}	t_{ACC}	When data is read from program memory	2			μs
Address **Note 2** to data output hold time	t_{HAD}	t_{OH}	When data is read from program memory	0		130	ns
MD3 hold time (from MD0 ↑)	t_{M3HR}	—	When data is read from program memory	2			μs
Data output float delay time from MD3 ↓	t_{DFR}	—	When data is read from program memory	2			μs

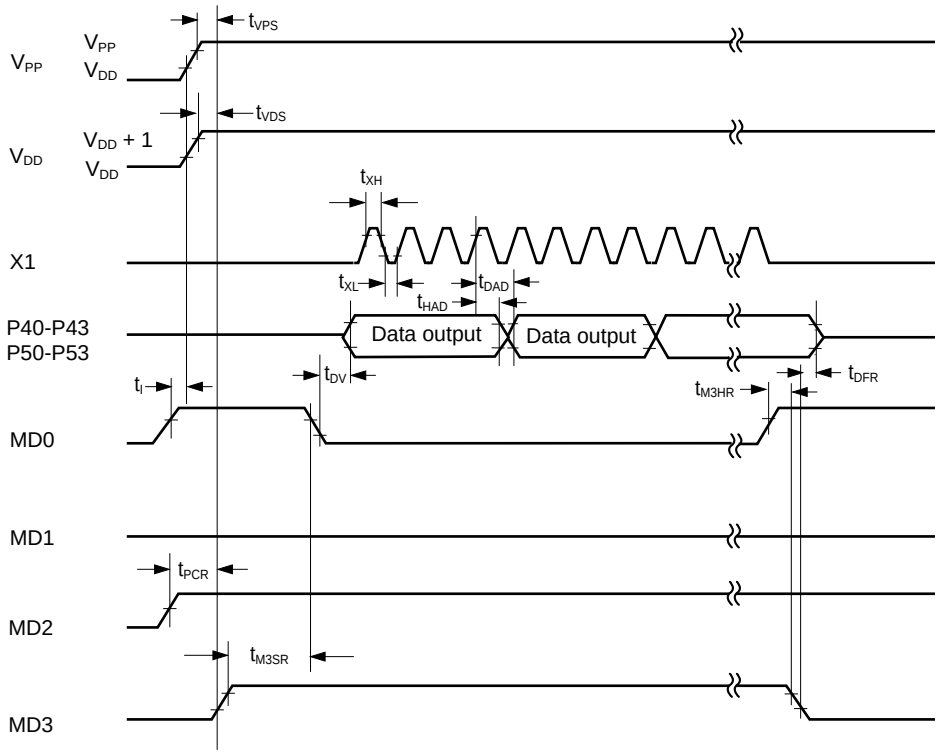
Notes 1. These symbols are correspond to μPD27C256A symbols.

2. The internal address signal is incremented by 1 at the rising edge of fourth X1 input. The internal address is not connected to any pin.

Program Memory Write Timing ★

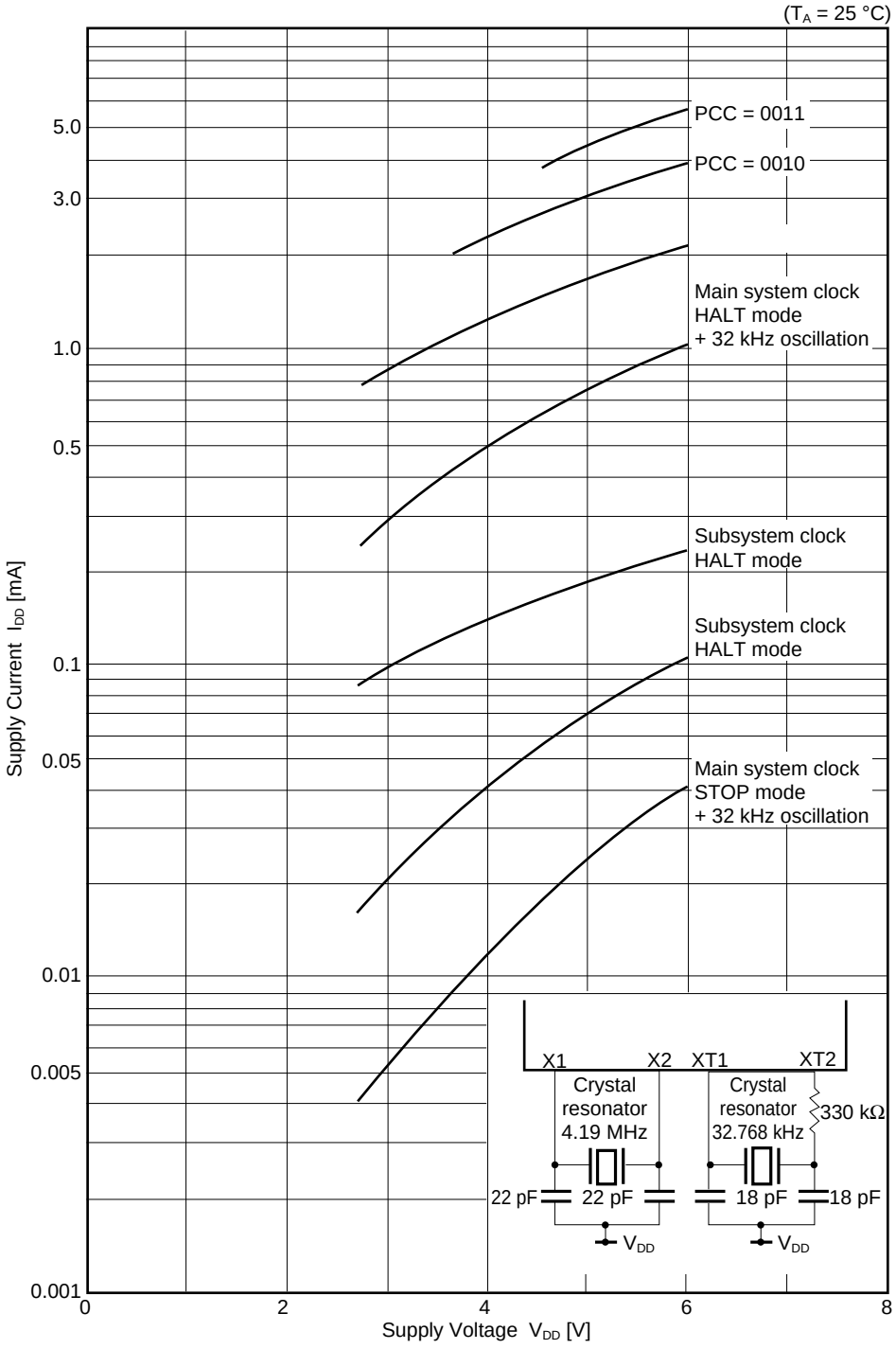


Program Memory Read Timing ★

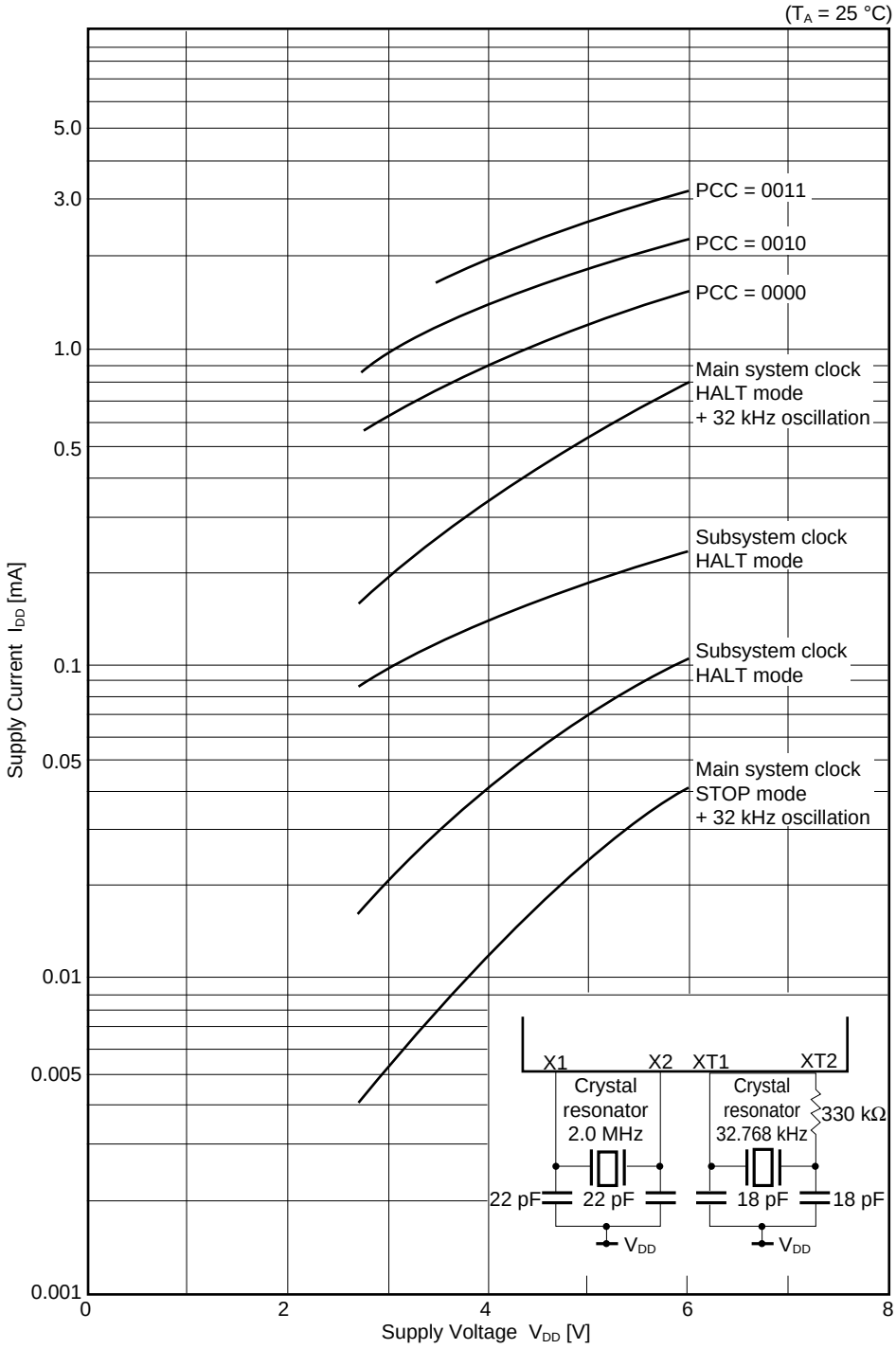


★ 5. CHARACTERISTIC CURVES (REFERENCE VALUES)

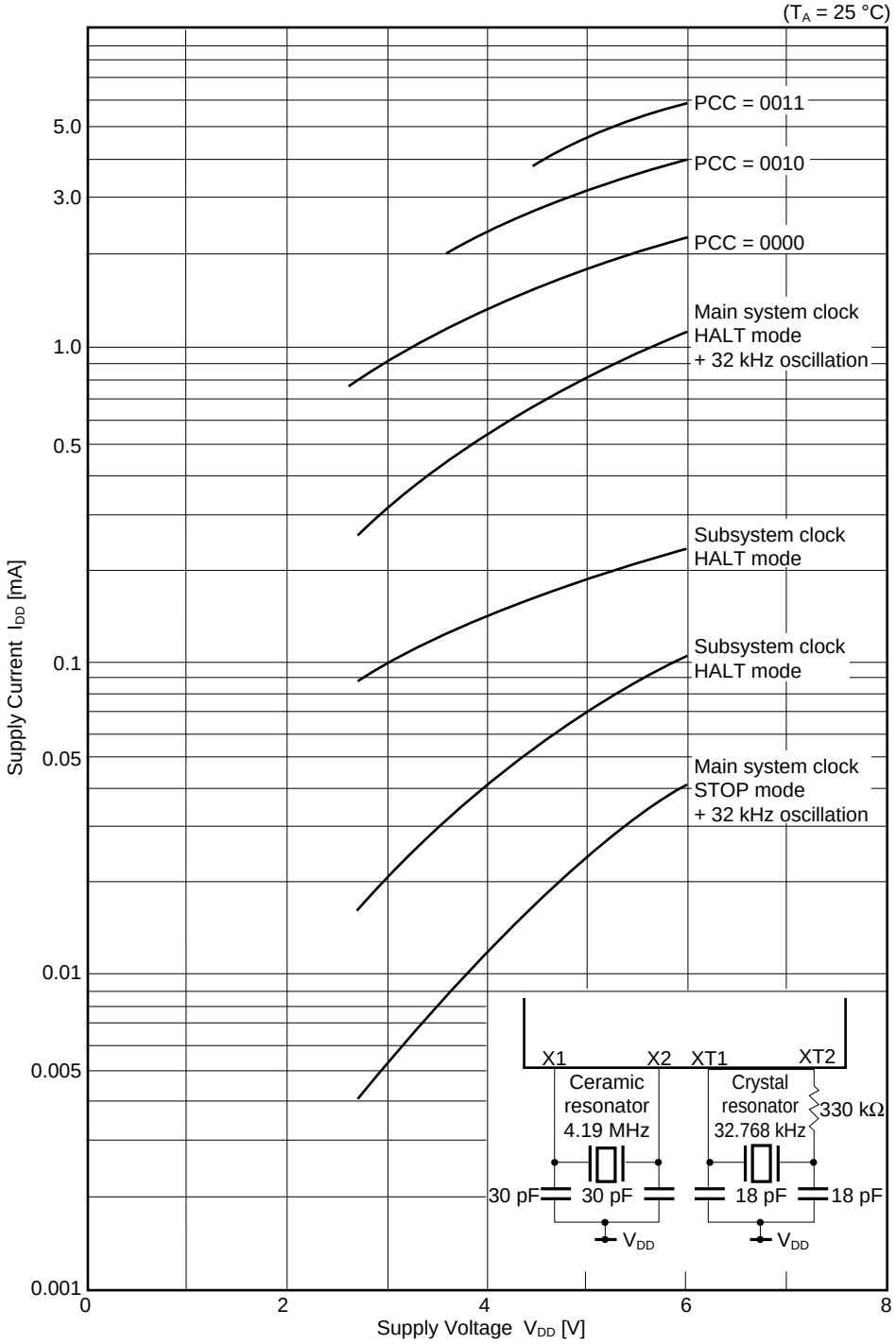
I_{DD} vs V_{DD} (4.19-MHz Main System Clock, Crystal Resonator)



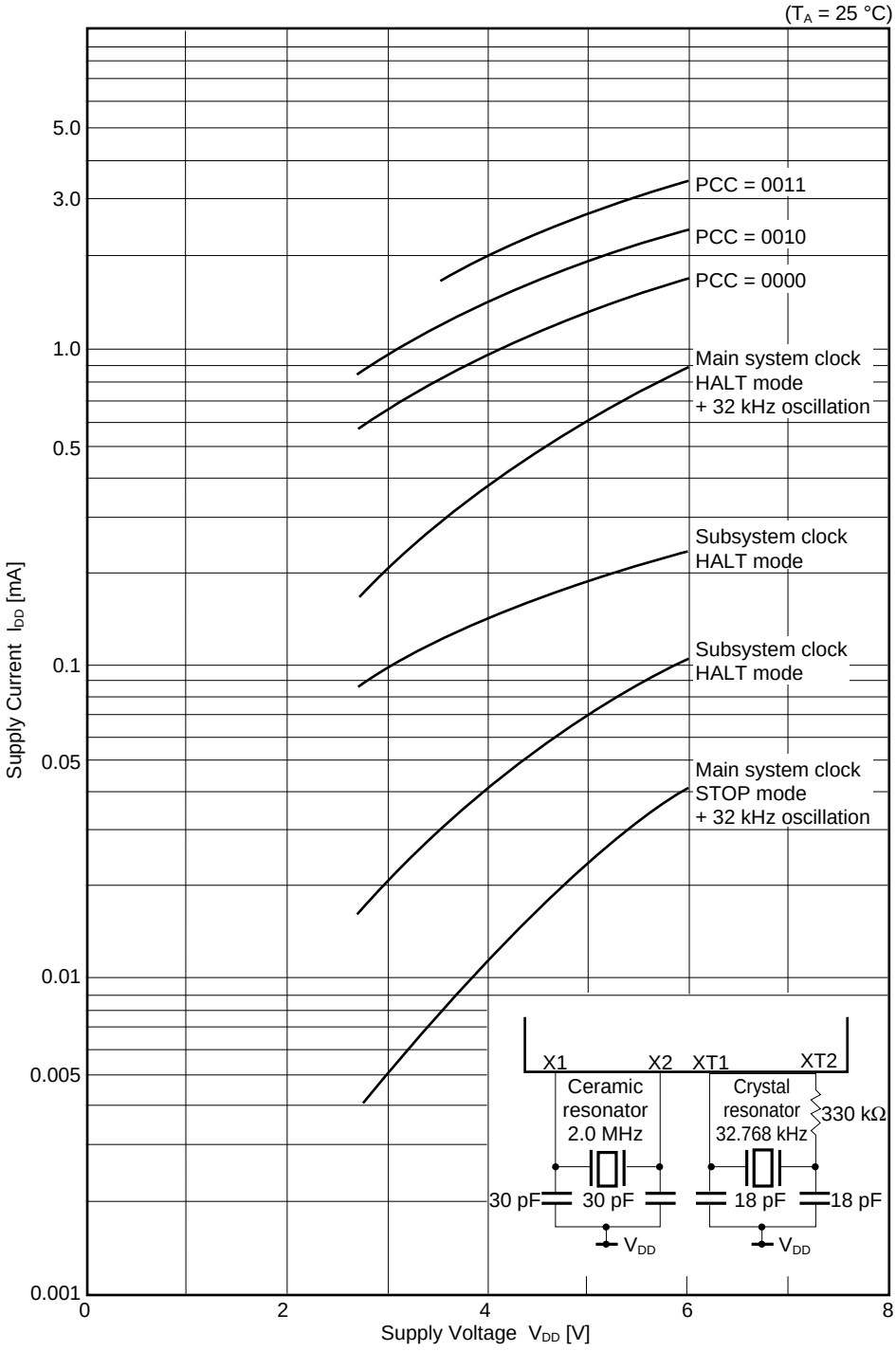
I_{DD} vs V_{DD} (2.0-MHz Main System Clock, Crystal Resonator)



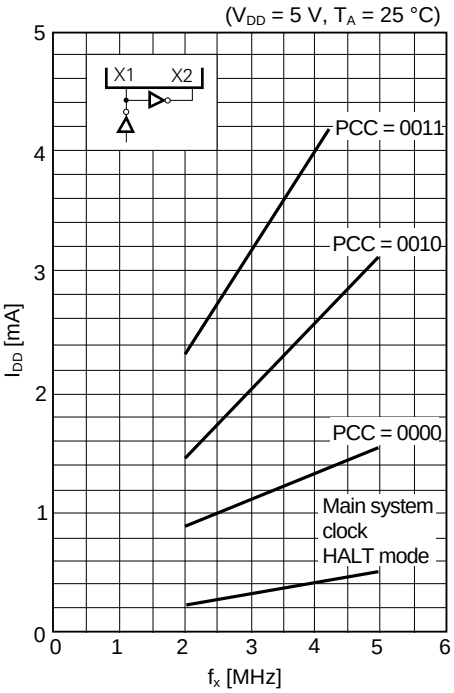
I_{DD} vs V_{DD} (4.19-MHz Main System Clock, Ceramic Resonator)



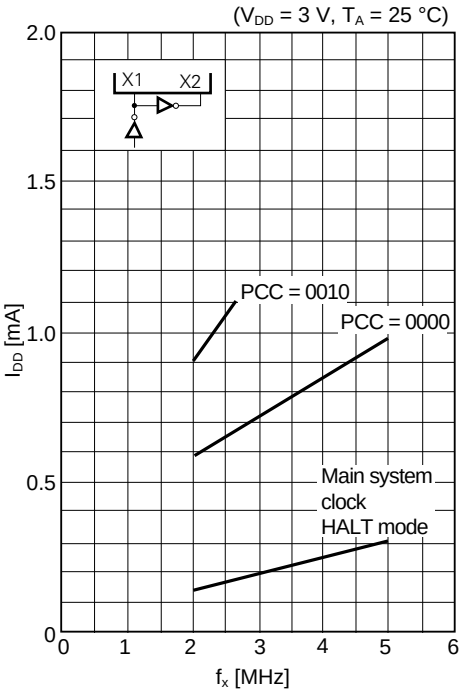
I_{DD} vs V_{DD} (20-MHz Main System Clock, Ceramic Resonator)



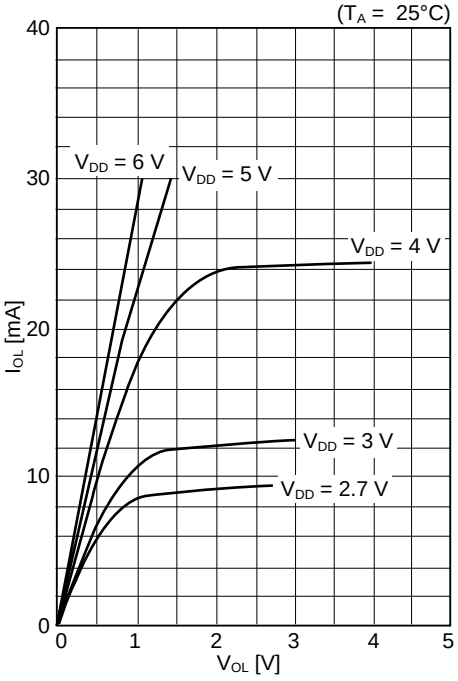
I_{DD} vs f_x



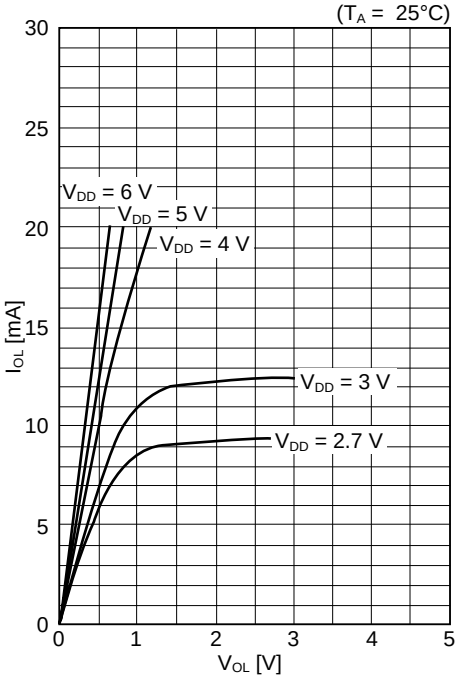
I_{DD} vs f_x



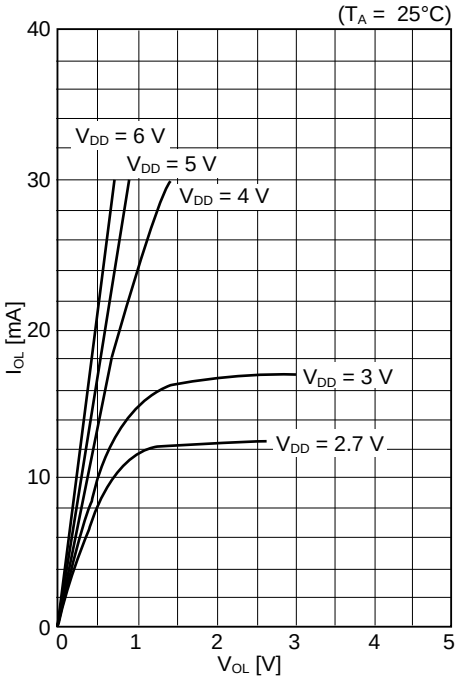
I_{OL} vs V_{OL} (Port 0)



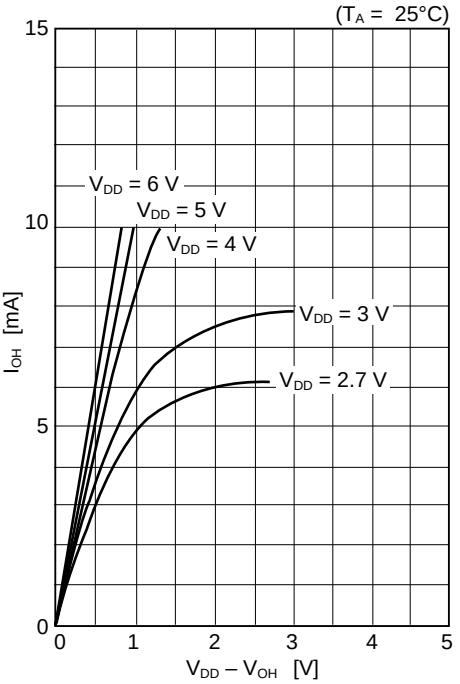
I_{OL} vs V_{OL} (Ports 2, 6 to 10)



I_{OL} vs V_{OL} (Ports 3 to 5)

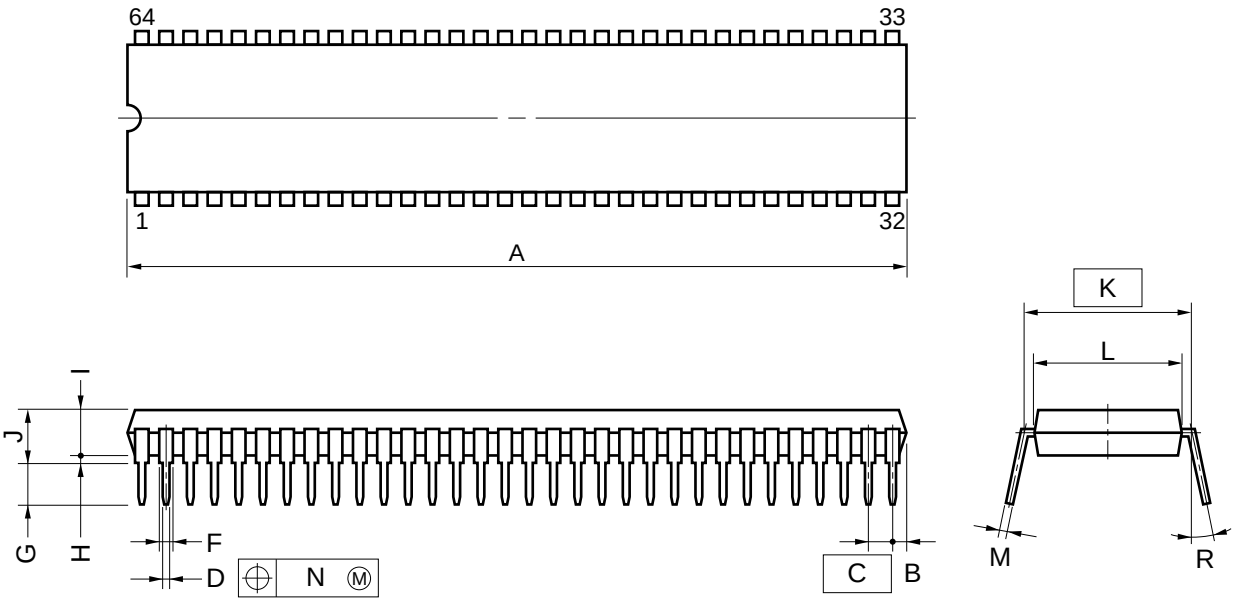


I_{OH} vs V_{DD}–V_{OH}



6. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



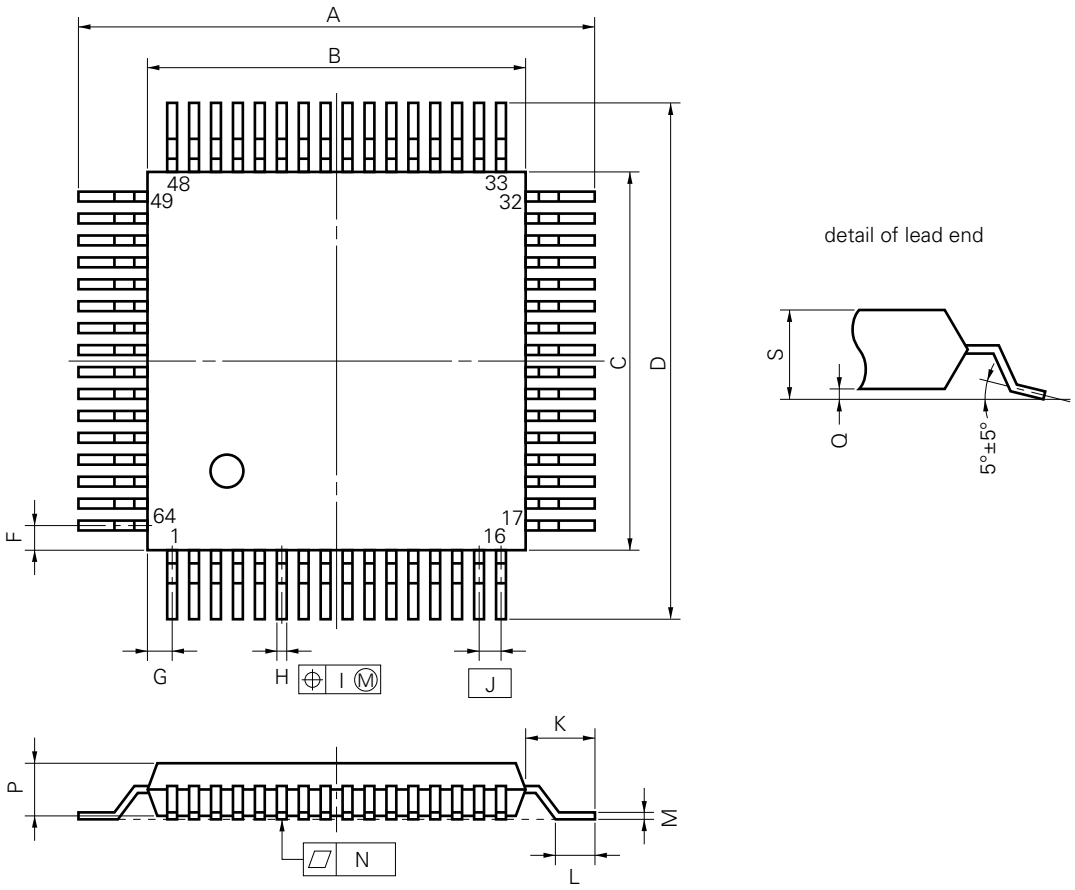
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



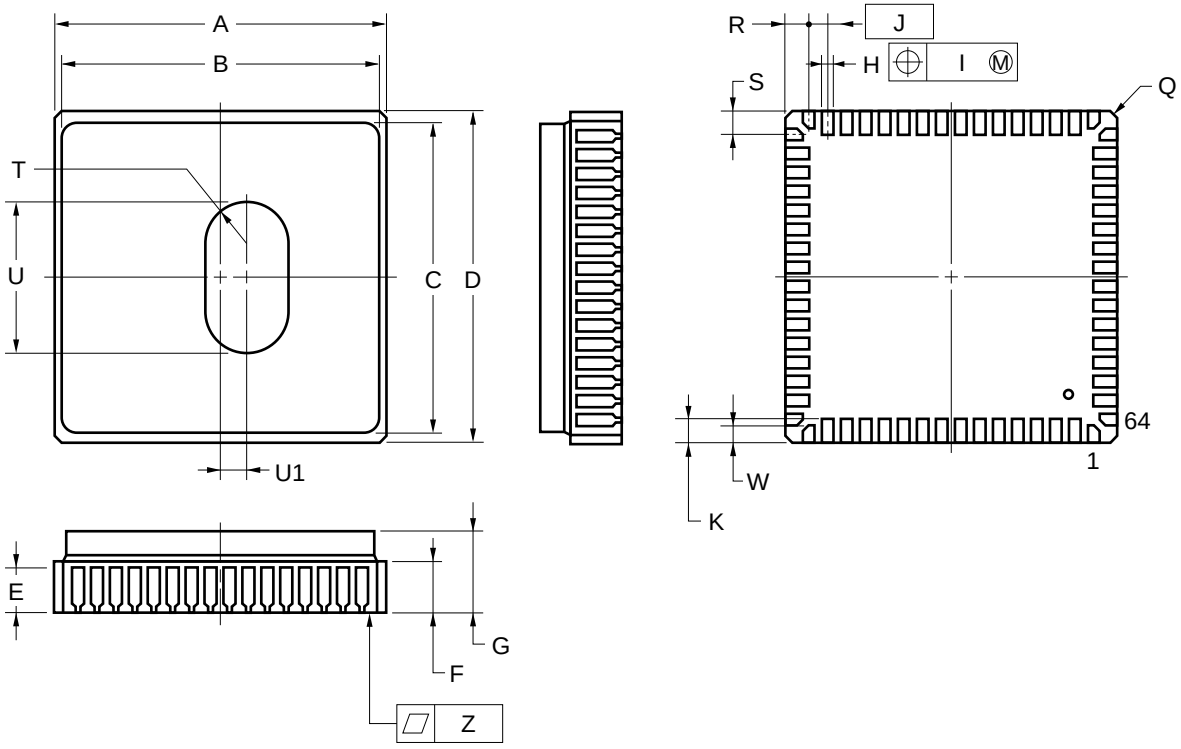
P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

★ 64 PIN CERAMIC WQFN



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.8±0.25	$0.543^{+0.011}_{-0.010}$
B	13.0	0.512
C	12.4	0.488
D	13.8±0.25	$0.543^{+0.011}_{-0.010}$
E	1.94	0.076
F	2.14	0.084
G	3.56 MAX.	0.141 MAX.
H	0.51±0.1	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.15	0.039±0.006
Q	C 0.3	C 0.012
R	0.9	0.035
S	0.9	0.035
T	R 1.5	R 0.059
U	6.0	0.236
U1	1.0	0.039
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

X64KG-80A-1

7. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD75P036 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document **"Semiconductor Devices Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 7-1. Soldering Conditions for Surface Mount Devices

μPD75P036GC-AB8: 64-pin plastic QFP (14 x 14 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Code
Wave soldering	Soldering bath temperature: 260°C max., Time: 10 seconds max., Number of times: 1, Maximum number of days: 2 days[Note], (thereafter, 16 hours of prebaking is required at 125°C), Preheating temperature: 120°C max. (package surface temperature).	WS60-162-1
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (210°C min.), Number of times: 1, Maximum number of days: 2 days[Note] (thereafter, 16 hours of prebaking is required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 1, Maximum number of days: 2 days[Note] (thereafter, 16 hours of prebaking is required at 125°C)	VP15-162-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note Number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

Caution Do not use different soldering methods together (except the partial heating method).

Table 7-2. Soldering Conditions for Through-hole Devices

μPD75P036CW: 64-pin Plastic Shrink DIP (750 mils)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Soldering bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)

Caution Apply wave soldering only to the lead part and be careful so as not to bring solder into direct contact with the device body.

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are readily available to support development of systems using μPD75P03s:

Hardware	IE-75000-R Note 1 IE-75001-R	In-circuit emulator for 75K series
	IE-75000-R-EM Note 2	Emulation board for IE-75000-R and IE-75001-R
	EP-75028CW-R	Emulation prove for μPD75P036CW
	EP-75028GC-R	Emulation prove for μPD75P036GC. Provided with 64-pin conversion socket.
	EV-9200GC-64	EV-9200G-80 used for μPD75P036GC/75P036KG
	PG-1500	PROM programmer
	PA-75P036CW	PROM programmer adapter used for μPD75P036CW. It is connected to PG-1500.
	PA-75P036GC	PROM programmer adapter used for μPD75P036GC. It is connected to PG-1500.
Software	IE control program	Host machine
	PG-1500 controller	• PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A Note 3)
	RA75X relocatable assembler	• IBM PC/AT™ (Refer to document **OS for IBM PC**)

Notes 1. For maintenance purpose only

2. Not provided with IE-75001-R

3. Ver.5.00/5.00A has a task swap function, but this function cannot be used with these software.

Remark Please refer to the **75X SERIES SELECTION GUIDE (IF-1027)** for information on third party development tools.

OS for IBM PC

The following OS are supported for IBM PC.

OS	Version
PC DOS™	Ver. 3.1 to Ver. 6.3 J6.1/V Note to 16.3/V Note
MS-DOS	Ver. 5.0 to Ver. 6.2 5.0/V Note to J6.2/V Note
IBM DOS™	J5.02/V Note

Note Supported only English mode.

Caution Ver. 5.0 or later has a task swap function, but this function cannot be used with these software.

APPENDIX B. RELATED DOCUMENTS ★

Please use this document in conjunction with the following.
Related document may be "Preliminary." However, in this document, "Preliminary" is not indicated.

Device Document

Title	Document Number	
	Japanese	English
μPD75P036 Data Sheet (This document)	IC-7914	IC-2967
μPD75028 User's Manual	IEU-694	IEU-1280
μPD75028 Instruction List	IEM-5511	—
μPD75028 Application Note — Basics	IEA-689	IEA-1277
75X series Selection Guide	IF-151	IF-1027

Development Tool Document

Title			Document Number	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75000-R-EM User's Manual		EEU-673	EEU-1294
	EP-75028CW-R User's Manual		EEU-697	EEU-1314
	IE-75028GC-R User's Manual		EEU-692	EEU-1306
	PG-1500 User'ss Manual		EEU-651	EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual	PC-9800 series (MS-DOS) based	EEU-704	Scheduled
		IBM PC series (PC DOS) based	EEU-5008	EEU-1291

Other Document

Title	Number	
	Japanese	English
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer-Related Product Guide — Third Party Products	MEI-604	—

Caution The contents of the documents listed above are subject to change without prior notice to user's. Make sure to use the latest edition when starting design.

NOTES FOR CMOS DEVICES

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input lelvel may be generated due to noise, etc., hence causing mulfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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