# IAM-20380HT

## High Performance Automotive Grade2 3-axis Gyroscope

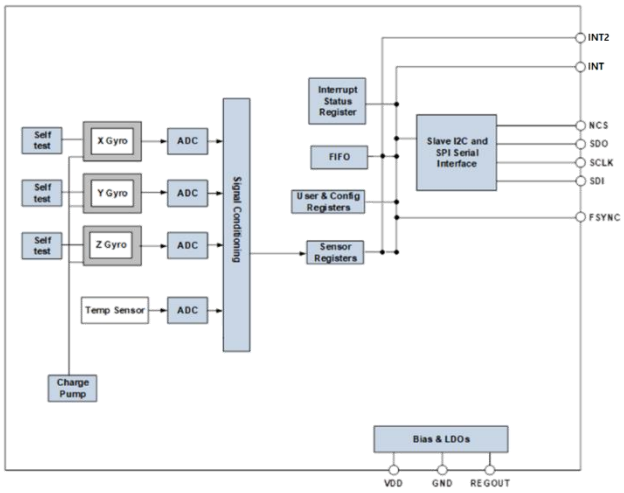
## GENERAL DESCRIPTION

The IAM-20380HT is a grade2 3-axis gyroscope MotionTracking device for Automotive non-safety applications in a thin 3x3x0.75mm$^3$ (16-pin LGA) package. It also features a 4096-byte FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. IAM-20380HT, with its 3-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The gyroscope has a programmable full-scale range of ±250 dps, ±500 dps, ±1000 dps and ±2000 dps. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and two programmable interrupts. The device features I$^2$C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

## BLOCK DIAGRAM




## APPLICATIONS

IAM-20380HT address a wide range of Automotive applications, including but not limited to:

- Navigation Systems Aids for Dead Reckoning
- Lift Gate Motion Detection
- Accurate Location for Vehicle to Vehicle and Infrastructure
- View Camera Stabilization and Vision Systems
- Head-up display (HUD) and augmented reality HUD
- Car Alarm
- Telematics
- Insurance Vehicle Tracking

## ORDERING INFORMATION

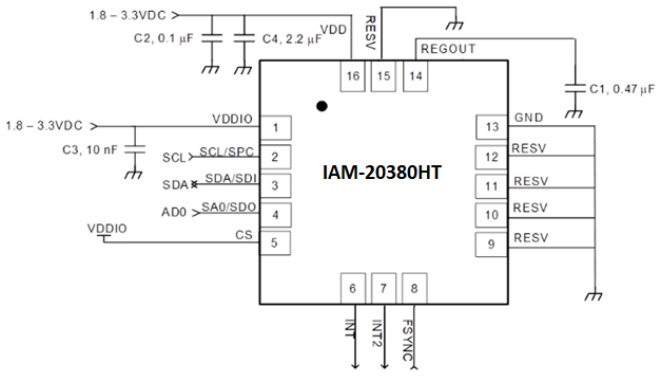
| PART | AXES | TEMP RANGE | PACKAGE | MSL* |
|---|---|---|---|---|
| IAM-20380HT† | X, Y, Z | -40°C to +105°C | 16-Pin LGA | 3 |

†Denotes RoHS and Green-compliant package
* Moisture sensitivity level of the package

## FEATURES

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250dps, ±500dps, ±1000dps, and ±2000dps, integrated 16-bit ADCs.
- User-programmable digital filters for gyroscope and temperature sensor
- Embedded Self-test
- Two interrupt lines
- Reliability testing performed according to AEC–Q100: PPAP and qualification report available upon request
- Final test at -40°C, 25°C, and +105°C

## TYPICAL OPERATING CIRCUIT




### LONGEVITY COMMITMENT

To provide the best service for customers developing products with a long-life cycle we have designed and engineered products with longevity in mind. These products are designed for harsher environments and are tested and manufactured to higher accuracy and stability. https://invensense.tdk.com/longevity/



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# 1 INTRODUCTION

## 1.1 PURPOSE AND SCOPE

This document is a product specification, providing description, specifications, and design related information on the IAM-20380HT Automotive MotionTracking device. The device is housed in a thin 3x3x0.75 mm$^3$ 16-pin LGA package.

## 1.2 PRODUCT OVERVIEW

The IAM-20380HT is a 3-axis MotionTracking device for Automotive non-safety applications, that features a 3-axis gyroscope in a thin 3x3x0.75 mm$^3$ (16-pin LGA) package. It also features a 4096-byte FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. IAM-20380HT, with its 3-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The gyroscope has a programmable full-scale range of ±250 dps, ±500 dps, ±1000 dps, and ±2000 dps. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I$^2$C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using either I$^2$C at 400 kHz or SPI at 8 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, TDK-InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75 mm$^3$ (16-pin LGA), to provide a very small yet high-performance. The device provides high robustness by supporting 10,000*g* shock reliability.

## 1.3 APPLICATIONS

- Navigation Systems Aids for Dead Reckoning
- Lift Gate Motion Detections
- Accurate Location for Vehicle to Vehicle and Infrastructure
- View Camera Stabilization and Vision Systems
- Head-up display (HUD) and augmented reality HUD
- Car Alarm
- Telematics
- Insurance Vehicle Tracking

# 2 FEATURES

## 2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the IAM-20380HT includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250 dps, ±500 dps, ±1000 dps and ±2000 dps and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

## 2.2 ADDITIONAL FEATURES

The IAM-20380HT includes the following additional features:

- Thinnest LGA package for automotive applications: 3x3x0.75 $mm^3$ (16-pin LGA)
- 4096-byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope and temperature sensor
- 10,000*g* shock tolerant
- 400 kHz Fast Mode $I^2C$ for communicating with all registers
- 8 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

# 3 ELECTRICAL CHARACTERISTICS

## 3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, $T_A$ = 25°C, Full Scale = 2000dps, Low-Noise Mode enabled unless otherwise noted.

All Zero-rate output, sensitivity, and noise specifications include board soldering effects, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **GYROSCOPE SENSITIVITY** | | | | | | |
| Full-Scale Range | FS_SEL=0 | | ±250 | | dps | 3 |
| | FS_SEL=1 | | ±500 | | dps | 3 |
| | FS_SEL=2 | | ±1000 | | dps | 3 |
| | FS_SEL=3 | | ±2000 | | dps | 3 |
| Gyroscope ADC Word Length | | | 16 | | bits | 3 |
| Sensitivity Scale Factor | FS_SEL=0 | | 131 | | LSB/(dps) | 3 |
| | FS_SEL=1 | | 65.5 | | LSB/(dps) | 3 |
| | FS_SEL=2 | | 32.8 | | LSB/(dps) | 3 |
| | FS_SEL=3 | | 16.4 | | LSB/(dps) | 3 |
| Nonlinearity | Best fit straight line; 25°C | | ±0.1 | | % | 1 |
| Cross-Axis Sensitivity | 25°C | | ±1 | | % | 1 |
| **ZERO-RATE OUTPUT (ZRO)** | | | | | | |
| ZRO Tolerance | All axes, 25°C | | ±0.8 | | dps | 1,2 |
| ZRO Variation Over Temperature | All axes, -40°C to +105°C | | ±1.0 | | dps | 1,2 |
| **GYROSCOPE NOISE PERFORMANCE** | | | | | | |
| Rate Noise Spectral Density | 25°C, initial, Noise BW = 306 Hz, VDD = VDDIO = 1.8V | | 0.005 | | dps/√Hz | 1,4 |
| Gyroscope Mechanical Frequencies | | | 27 | | KHz | 2 |
| Low Pass Filter Response | Programmable Range | 5 | | 250 | Hz | 3 |
| Gyroscope Start Up Time | From Sleep mode, 25°C | | 35 | 50 | ms | 1 |
| Output Data Rate | Programmable, Normal (Filtered) mode | 4 | | 8000 | Hz | 1 |

**Table 1. Gyroscope Specifications**

**Notes**:

1. Based on characterization data on a limited number of parts.
2. Tested in production at component level. Over temperature tests are performed at 25°C, 105°C, and/or -40°C.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.

## 3.2 ELECTRICAL SPECIFICATIONS

### 3.2.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, $T_A$ = 25°C, Low-Noise Mode enabled unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGES** | | | | | | |
| VDD | | 1.71 | 1.8 | 3.6 | V | 1 |
| VDDIO | | 1.71 | 1.8 | 3.6 | V | 1 |
| **SUPPLY CURRENTS & BOOT TIME** | | | | | | |
| Normal Mode | 3-axis Gyroscope | | 2.6 | | mA | 1 |
| Full-Chip Sleep Mode | | | 6 | | µA | 1 |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Temperature Range | Performance parameters are not applicable beyond Specified Temperature Range | -40 | | +105 | °C | 1,2 |

**Table 2. D.C. Electrical Characteristics**

**Notes**:

1. Based on characterization data on a limited number of parts.
2. Based on qualification.

### 3.2.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SUPPLIES** | | | | | | |
| Supply Ramp Time ($T_{RAMP}$) | Monotonic ramp. Ramp rate is 10% to 90% of the final value | 0.01 | | 100 | ms | 1 |
| **TEMPERATURE SENSOR** | | | | | | |
| Operating Range | Ambient | -40 | | 105 | °C | 1 |
| Room Temperature Offset | 25°C | | 0 | | °C | 1 |
| Sensitivity | Untrimmed | | 326.8 | | LSB/°C | 1 |
| **POWER-ON RESET** | | | | | | |
| Supply Ramp Time ($T_{RAMP}$) | Valid power-on RESET | 0.01 | | 100 | ms | 1 |
| Start-up time for register read/write | From power-up | | 11 | 100 | ms | 1 |
| | From sleep | | | 5 | ms | 1 |
| **I²C ADDRESS** | SA0 = 0<br>SA0 = 1 | | 1101000<br>1101001 | | | |
| **DIGITAL INPUTS (FSYNC, SA0, SPC, SDI, CS)** | | | | | | |
| $V_{IH}$, High Level Input Voltage | | 0.7*VDDIO | | | V | 1 |
| $V_{IL}$, Low Level Input Voltage | | | | 0.3*VDDIO | V | |
| $C_I$, Input Capacitance | | | < 10 | | pF | |
| **DIGITAL OUTPUT (SDO, INT)** | | | | | | |
| $V_{OH}$, High Level Output Voltage | $R_{LOAD}$=1 MΩ; | 0.9*VDDIO | | | V | 1 |
| $V_{OL1}$, LOW-Level Output Voltage | $R_{LOAD}$=1 MΩ; | | | 0.1*VDDIO | V | |
| $V_{OL.INT}$, INT Low-Level Output Voltage | OPEN=1, 0.3 mA sink Current | | | 0.1 | V | |
| Output Leakage Current | OPEN=1 | | 100 | | nA | |
| $t_{INT}$, INT Pulse Width | LATCH_INT_EN=0 | | 50 | | µs | |
| **I²C I/O (SCL, SDA)** | | | | | | |
| $V_{IL}$, LOW Level Input Voltage | | -0.5V | | 0.3*VDDIO | V | 1 |
| $V_{IH}$, HIGH-Level Input Voltage | | 0.7*VDDIO | | VDDIO + 0.5V | V | |
| $V_{hys}$, Hysteresis | | | 0.1*VDDIO | | V | |
| $V_{OL}$, LOW-Level Output Voltage | 3 mA sink current | 0 | | 0.4 | V | |
| $I_{OL}$, LOW-Level Output Current | $V_{OL}$=0.4V<br>$V_{OL}$=0.6V | | 3<br>6 | | mA<br>mA | |
| Output Leakage Current | | | 100 | | nA | |
| $t_{of}$, Output Fall Time from $V_{IHmax}$ to $V_{ILmax}$ | $C_b$ bus capacitance in pf | 20+0.1$C_b$ | | 300 | ns | |

| INTERNAL CLOCK SOURCE | | | | | | |
|---|---|---|---|---|---|---|
| Sample Rate | FCHOICE_B=1,2,3 SMPLRT_DIV=0 | | 32 | | kHz | 2 |
| | FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0 | | 8 | | kHz | 2 |
| | FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0 | | 1 | | kHz | 2 |
| Clock Frequency Initial Tolerance | CLK_SEL=0, 6 or gyro inactive; 25°C | -5 | | +5 | % | 1 |
| | CLK_SEL=1,2,3,4,5 and gyro active; 25°C | -1 | | +1 | % | 1 |
| Frequency Variation over Temperature | CLK_SEL=0,6 or gyro inactive | -10 | | +10 | % | 1 |
| | CLK_SEL=1,2,3,4,5 and gyro active | -1 | | +1 | % | 1 |

**Table 3. A.C. Electrical Characteristics**

**Notes**:
1. Based on characterization data on a limited number of parts.
2. Guaranteed by design.

### 3.2.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| SERIAL INTERFACE | | | | | | |
| SPI Operating Frequency, All Registers Read/Write | Low Speed Characterization | | 100 ±10% | | kHz | 1 |
| | High Speed Characterization | | 1 | 8 | MHz | 1, 2 |
| SPI Modes | | | Modes 0 and 3 | | | |
| $I^2C$ Operating Frequency | All registers, Fast-mode | | | 400 | kHz | 1 |
| | All registers, Standard-mode | | | 100 | kHz | 1 |

**Table 4. Other Electrical Specifications**

**Notes**:
1. Based on characterization data on a limited number of parts.
2. SPI clock duty cycle between 45% and 55% should be used for 8-MHz operation.

## 3.3 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, $T_A$ = 25°C, unless otherwise noted.

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **I²C TIMING** | **I²C FAST-MODE** | | | | | |
| $f_{SCL}$, SCL Clock Frequency | | | | 400 | kHz | 1 |
| $t_{HD.STA}$, (Repeated) START Condition Hold Time | | 0.6 | | | µs | 1 |
| $t_{LOW}$, SCL Low Period | | 1.3 | | | µs | 1 |
| $t_{HIGH}$, SCL High Period | | 0.6 | | | µs | 1 |
| $t_{SU.STA}$, Repeated START Condition Setup Time | | 0.6 | | | µs | 1 |
| $t_{HD.DAT}$, SDA Data Hold Time | | 0 | | | µs | 1 |
| $t_{SU.DAT}$, SDA Data Setup Time | | 100 | | | ns | 1 |
| $t_r$, SDA and SCL Rise Time | $C_b$ bus cap. from 10 to 400 pF | 20+0.1$C_b$ | | 300 | ns | 1 |
| $t_f$, SDA and SCL Fall Time | $C_b$ bus cap. from 10 to 400 pF | 20+0.1$C_b$ | | 300 | ns | 1 |
| $t_{SU.STO}$, STOP Condition Setup Time | | 0.6 | | | µs | 1 |
| $t_{BUF}$, Bus Free Time Between STOP and START Condition | | 1.3 | | | µs | 1 |
| $C_b$, Capacitive Load for each Bus Line | | | < 400 | | pF | 1 |
| $t_{VD.DAT}$, Data Valid Time | | | | 0.9 | µs | 1 |
| $t_{VD.ACK}$, Data Valid Acknowledge Time | | | | 0.9 | µs | 1 |

**Table 5. I²C Timing Characteristics**

**Notes**:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

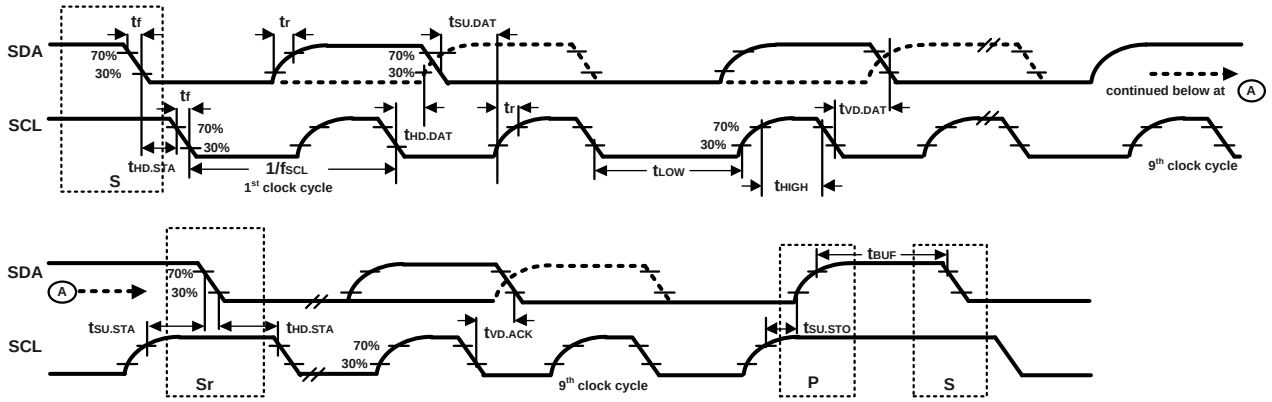



**Figure 1. I²C Bus Timing Diagram**

## 3.4 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, $T_A$ = 25°C, unless otherwise noted.

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **SPI TIMING** | | | | | | |
| $f_{SPC}$, SPC Clock Frequency | | | | 8 | MHz | 1 |
| $t_{LOW}$, SPC Low Period | | 56 | | | ns | 1 |
| $t_{HIGH}$, SPC High Period | | 56 | | | ns | 1 |
| $t_{SU.CS}$, CS Setup Time | | 2 | | | ns | 1 |
| $t_{HD.CS}$, CS Hold Time | | 63 | | | ns | 1 |
| $t_{SU.SDI}$, SDI Setup Time | | 3 | | | ns | 1 |
| $t_{HD.SDI}$, SDI Hold Time | | 7 | | | ns | 1 |
| $t_{VD.SDO}$, SDO Valid Time | $C_{load}$ = 20 pF | | | 40 | ns | 1 |
| $t_{HD.SDO}$, SDO Hold Time | $C_{load}$ = 20 pF | 6 | | | ns | 1 |
| $t_{DIS.SDO}$, SDO Output Disable Time | | | | 20 | ns | 1 |
| $t_{Fall}$, SCLK Fall Time | | | | 6.5 | ns | 2 |
| $t_{Rise}$, SCLK Rise Time | | | | 6.5 | ns | 2 |

**Table 6. SPI Timing Characteristics (8 MHz Operation)**

**Notes**:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.
2. Based on other parameter values.

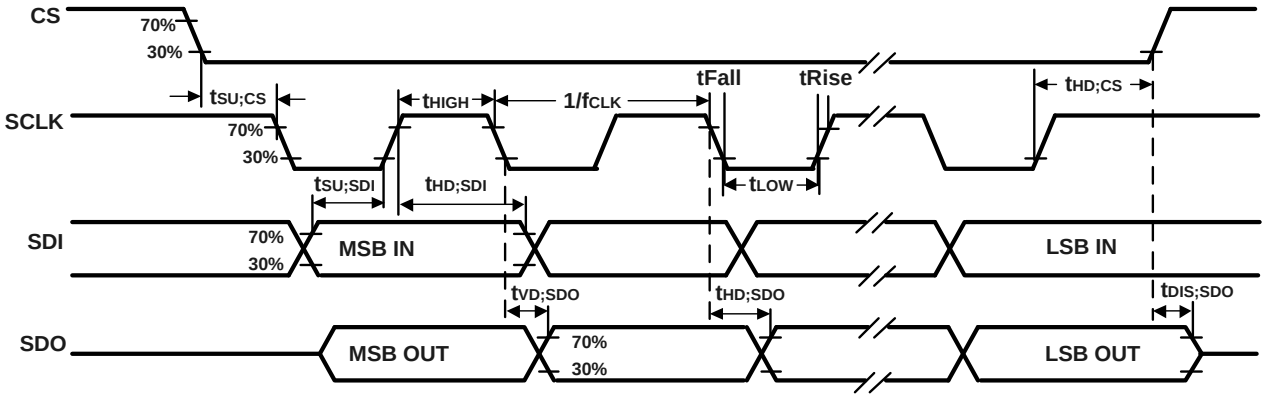



**Figure 2. SPI Bus Timing Diagram**

## 3.5 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

| PARAMETER | RATING |
|---|---|
| Supply Voltage, VDD | -0.5V to 4V |
| Supply Voltage, VDDIO | -0.5V to 4V |
| REGOUT | -0.5V to 2V |
| Input Voltage Level (SA0, FSYNC, SCL, SDA) | -0.5V to VDDIO + 0.5V |
| Acceleration (Any Axis, unpowered) | 10,000*g* for 0.2ms |
| Temperature Range | -40°C to 105°C |
| Storage Temperature Range | -40°C to 125°C |
| Electrostatic Discharge (ESD) Protection | 2 kV (HBM);<br>750V (CDM corner pins)<br>500V (CDM all other pins) |
| Latch-up | JEDEC Class II (2),125°C<br>±100 mA |
| Ultrasonic excitation (cleaning/welding/…) | Not allowed |

**Table 7. Absolute Maximum Ratings**

## 3.6 THERMAL INFORMATION

| THERMAL METRIC | DESCRIPTION | VALUE |
|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 84.58 °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7 °C/W |

**Table 8. Thermal Information**

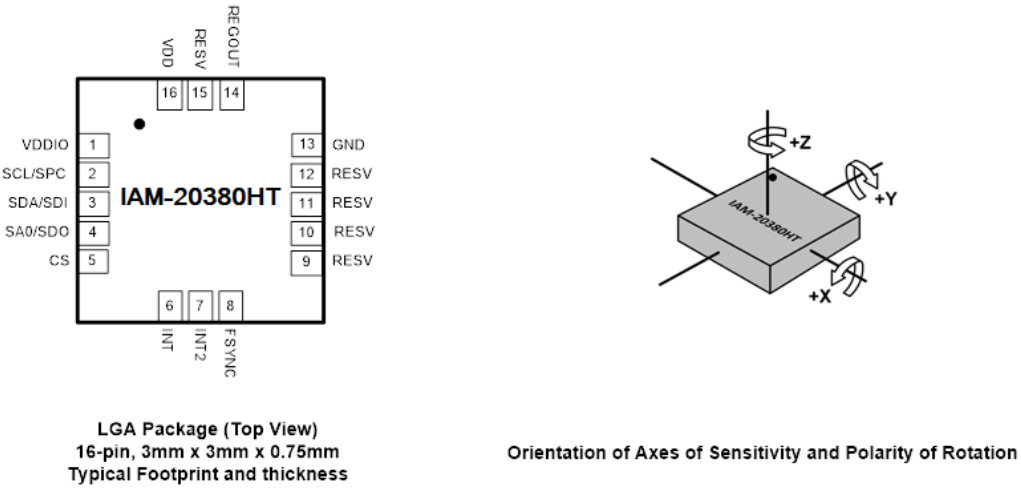
# 4 APPLICATIONS INFORMATION

## 4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

| PIN NUMBER | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 1 | VDDIO | Digital I/O supply voltage |
| 2 | SCL/SPC | I²C serial clock (SCL); SPI serial clock (SPC) |
| 3 | SDA/SDI | I²C serial data (SDA); SPI serial data input (SDI) |
| 4 | SA0/SDO | I²C slave address LSB (SA0); SPI serial data output (SDO) |
| 5 | CS | Chip select (0 = SPI mode; 1 = I²C mode) |
| 6 | INT | Interrupt digital output (push-pull or open-drain) |
| 7 | INT2 | Second Interrupt digital output (push-pull or open-drain) |
| 8 | FSYNC | Synchronization digital input (optional). Connect to GND if unused |
| 9 | RESV | Reserved. Connect to GND |
| 10 | RESV | Reserved. Connect to GND |
| 11 | RESV | Reserved. Connect to GND |
| 12 | RESV | Reserved. Connect to GND |
| 13 | GND | Connect to GND |
| 14 | REGOUT | Regulator filter capacitor connection |
| 15 | RESV | Reserved. Connect to GND |
| 16 | VDD | Power Supply |

**Table 9. Signal Descriptions**

**Note**: VDD, VDDIO, SCL/SPC and CS pins must be correctly managed at power-up to guarantee proper IAM-20380HT start-up. Please refer to sections 4.17.1 and 4.17.2 for detailed power-up instructions.




LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75mm
Typical Footprint and thickness

Orientation of Axes of Sensitivity and Polarity of Rotation

**Figure 3. Pin out Diagram for IAM-20380HT 3.0x3.0x0.75mm³ LGA**

## 4.2 TYPICAL OPERATING CIRCUIT

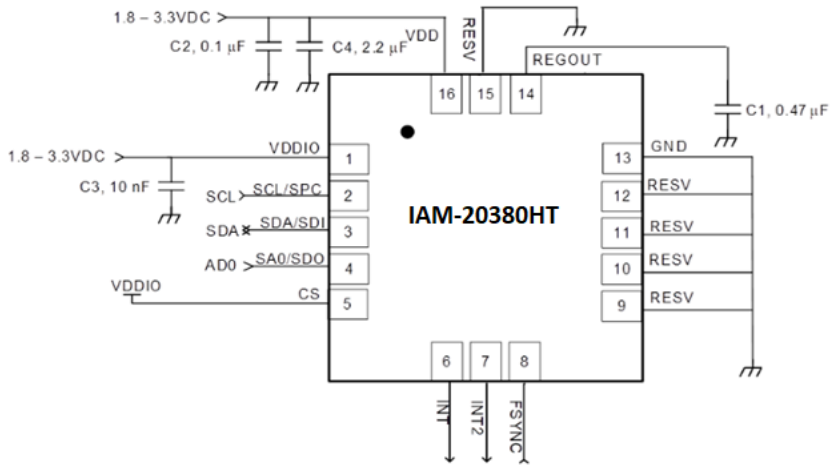



**Figure 4. IAM-20380HT LGA Application Schematic**

**Note**: $I^2C$ lines are open drain and pullup resistors (e.g. 10 kΩ) are required.

## 4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

| COMPONENT | LABEL | SPECIFICATION | QUANTITY |
|---|---|---|---|
| REGOUT Capacitor | C1 | X7R, 0.47 µF ±10% | 1 |
| VDD Bypass Capacitors | C2 | X7R, 0.1 µF ±10% | 1 |
| | C4 | X7R, 2.2 µF ±10% | 1 |
| VDDIO Bypass Capacitor | C3 | X7R, 10 nF ±10% | 1 |

**Table 10. Bill of Materials**

## 4.4 BLOCK DIAGRAM

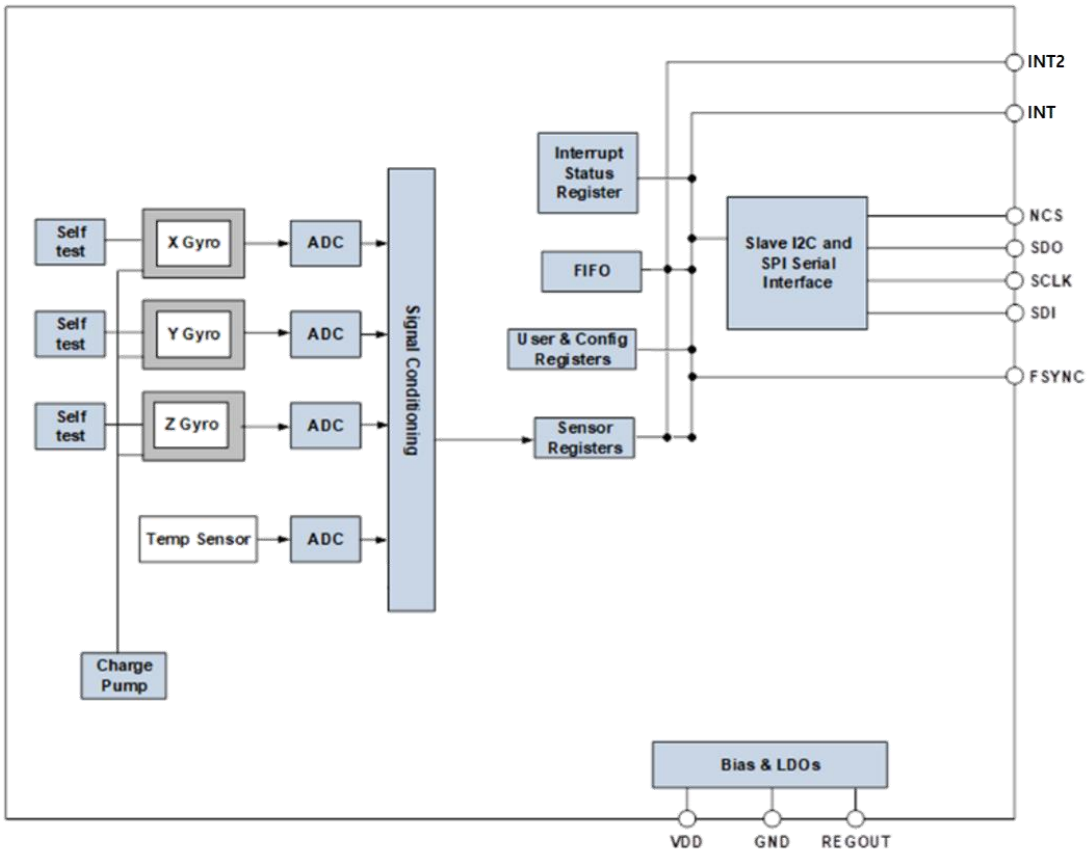



**Figure 5. IAM-20380HT Block Diagram**

## 4.5 OVERVIEW

The IAM-20380HT is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Primary $I^2C$ and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Two independent Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

## 4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The IAM-20380HT consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

## 4.7 I²C AND SPI SERIAL COMMUNICATIONS INTERFACES

The IAM-20380HT communicates to a system processor using either a SPI or an I²C serial interface. The IAM-20380HT always acts as a slave when communicating to the system processor. The LSB of the I²C slave address is set by pin 4 (SA0).

### 4.7.1 IAM-20380HT Solution Using I²C Interface

In Figure 6, the system processor is an I²C master to the IAM-20380HT.

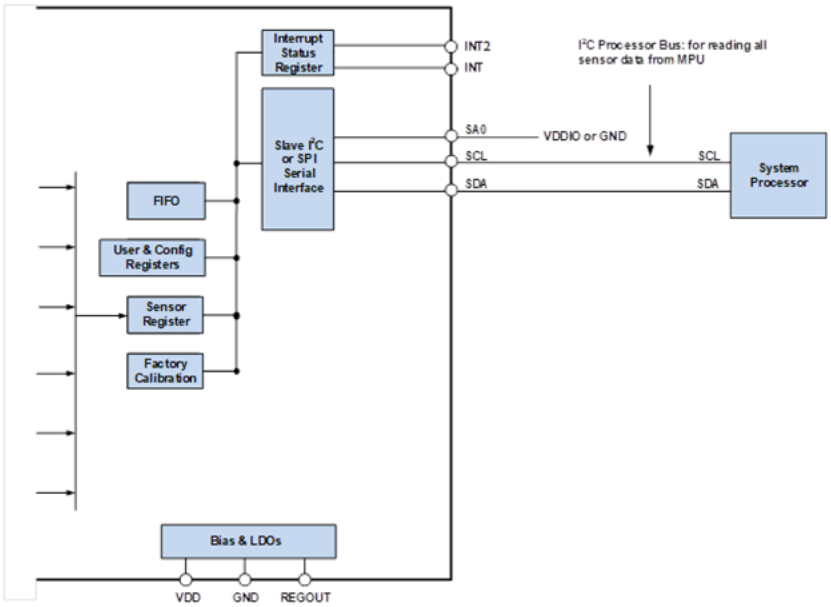



**Figure 6. IAM-20380HT Solution Using I²C Interface**

### 4.7.2 IAM-20380HT Solution Using SPI Interface

In Figure 7, the system processor is an SPI master to the IAM-20380HT. Pins 2, 3, 4, and 5 are used to support the SPC, SDI, SDO, and CS signals for SPI communications.

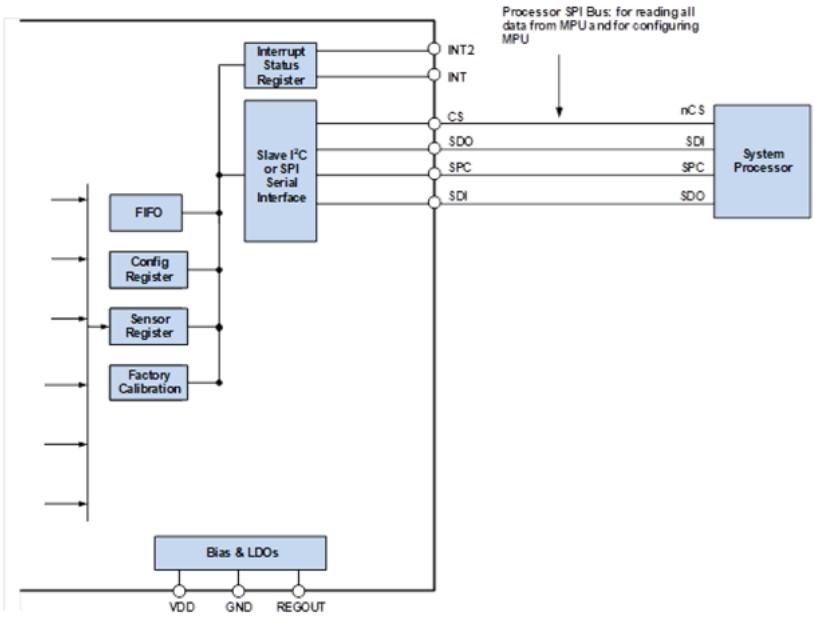



**Figure 7. IAM-20380HT Solution Using SPI Interface**

## 4.8 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope self-test registers (registers 27).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

## 4.9 CLOCKING

The IAM-20380HT has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

## 4.10 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read anytime.

## 4.11 FIFO

The IAM-20380HT contains a 4096-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data are written into the FIFO. Possible choices include gyro data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data are available.

## 4.12 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are new data are available to be read (from the FIFO and Data registers), FIFO overflow. The interrupt status can be read from the Interrupt Status register.

## 4.13 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the IAM-20380HT die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

## 4.14 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IAM-20380HT. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

## 4.15 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

## 4.16 STANDARD POWER MODES

Table 11 lists the user-accessible power modes for IAM-20380HT.

| MODE | NAME | GYRO |
|---|---|---|
| 1 | Sleep Mode | Off |
| 2 | Standby Mode | Drive On |
| 3 | Low-Noise Mode | On |
| 4 | Low-Power Mode | Duty-Cycled |

**Table 11. Standard Power Modes for IAM-20380HT**

**Notes:**

1. Power consumption for individual modes can be found in section 3.2.1.

## 4.17 SENSOR INITIALIZATION AND BASIC CONFIGURATION

The basic configuration of the IAM-20380HT includes the following steps:

- Power-up sequence
- Sensor initialization and clock source selection
- Digital interface access test
- Output data rate (i.e. sampling frequency) selection
- Full scale range selection
- Filter frequency selection
- Power mode selection

### 4.17.1 Power-up sequence

When applying VDD, the power voltage ramp is detected and a power-on-reset sequence is triggered inside the component. During this phase the device starts operating and internal logic levels are defined. For proper component initialization the power-up should be performed with both CS and SCL/SPC low, ensuring that CS and SCL pins are not in an

undetermined state during the VDD ramp. If starting in $I^2C$ mode (CS at logic high), power-up should be performed with SCL/SPC low. Power-up with SCL/SPC high is not a supported case and must be avoided.

It is worth noting that if the I/O pins (e.g. CS, SCL/SPC) are between $V_{IL}$ and $V_{IH}$ when the power-on-reset sequence is triggered, their value is undetermined and the internal logic levels may not be properly defined. It should also be noted that $V_{IL}$ and $V_{IH}$ are related to VDDIO and their value changes at power-up according to the applied VDDIO voltage ramp.

Power-up sequences that do not respect the conditions above may not lead to proper digital interface initialization. In this case a preliminary soft reset operation (PWR_MGMT_1 register set 0x81) must be performed to reset the digital interface, as soon as both VDD and VDDIO are stable at their final voltage. Since the digital interface may not be properly initialized, the device may not provide the acknowledge signal if the $I^2C$ protocol is used.

### 4.17.2 Sensor Initialization and Clock Source Selection

When power-up sequence is completed (as per section 4.17.1), a soft reset is required to initialize the sensor and let the IAM-20380HT select the best clock source. The soft reset must be performed by setting the register PWR_MGMT_1 (address 0x6B) to 0x81 (see section 9.22), prior to registers initialization.

Soft reset must be performed as first operation after the power-up sequence to ensure the proper component registers setting.
Correct WHO_AM_I value is ensured only after the soft reset has been completed.

### 4.17.3 Digital interface access test

When soft reset is completed, make sure the component registers access can be done as expected. WHO_AM_I (address 0x75) register can be used for this purpose to verify the identity of the device.

### 4.17.4 Output Data Rate Selection

To set the output data rate (ODR) to the desired frequency, select the sample rate divider by setting the register SMPLRT_DIV (address 0x19) to the desired value (see section 0). For instance, to set the output data rate to 100 Hz, write 0x09 into SMPLRT_DIV.

### 4.17.5 Full-Scale Range Selection

To set the FSR of the gyroscope, set the register GYRO_CONFIG (address 0x1B) to the desired value (see section 9.10). For instance, to set the FSR of the gyroscope to 250 dps, write 0x00 into GYRO_CONFIG.

### 4.17.6 Filter Selection

To set the corner frequency of the DLPF of the gyroscope, set the register CONFIG (address 0x1A) to the desired value (see section 0). For instance, to set the corner frequency of the DLPF of the gyroscope to 10 Hz, write 0x05 into CONFIG.

### 4.17.7 Power mode selection

To set desired power modes for IAM-20380HT (see section 4.16).

# 5 PROGRAMMABLE INTERRUPTS

The IAM-20380HT has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

| INTERRUPT NAME | MODULE |
|---|---|
| FIFO Overflow | FIFO |
| Data Ready | Sensor Registers |

**Table 12. Table of Interrupt Sources**

# 6 DIGITAL INTERFACE

## 6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the IAM-20380HT can be accessed using either I²C at 400 kHz or SPI at 8 MHz. SPI operates in four-wire mode.

| PIN NUMBER | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 1 | VDDIO | Digital I/O supply voltage. |
| 4 | SA0 / SDO | I²C Slave Address LSB (SA0); SPI serial data output (SDO) |
| 2 | SCL / SPC | I²C serial clock (SCL); SPI serial clock (SPC) |
| 3 | SDA / SDI | I²C serial data (SDA); SPI serial data input (SDI) |

**Table 13. Serial Interface**

**Note**: To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in section 3.2.2.

For further information regarding the I2C_IF_DIS bit, please refer to sections 8 and 9 of this document.

## 6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IAM-20380HT always operates as a slave device when communicating to the system processor, which acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the IAM-20380HT is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin SA0. This allows two IAM-20380HTs to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin SA0 is logic low) and the address of the other should be b1101001 (pin SA0 is logic high).

## 6.3 IC COMMUNICATIONS PROTOCOL

*START (S) and STOP (P) Conditions*

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see Figure 8).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

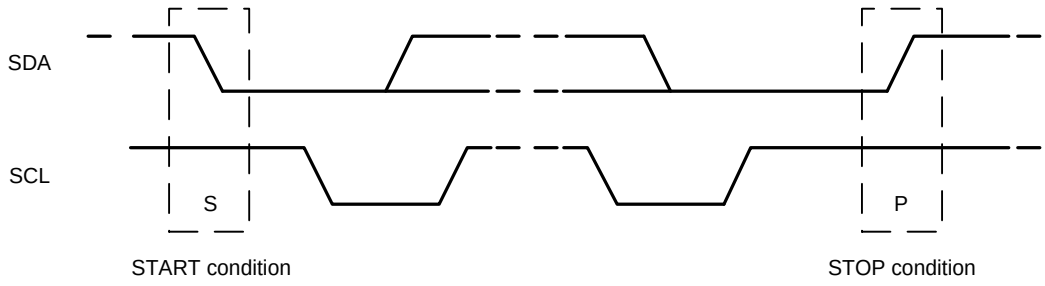



**Figure 8. START and STOP Conditions**

*Data Format / Acknowledge*

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to Figure 9).

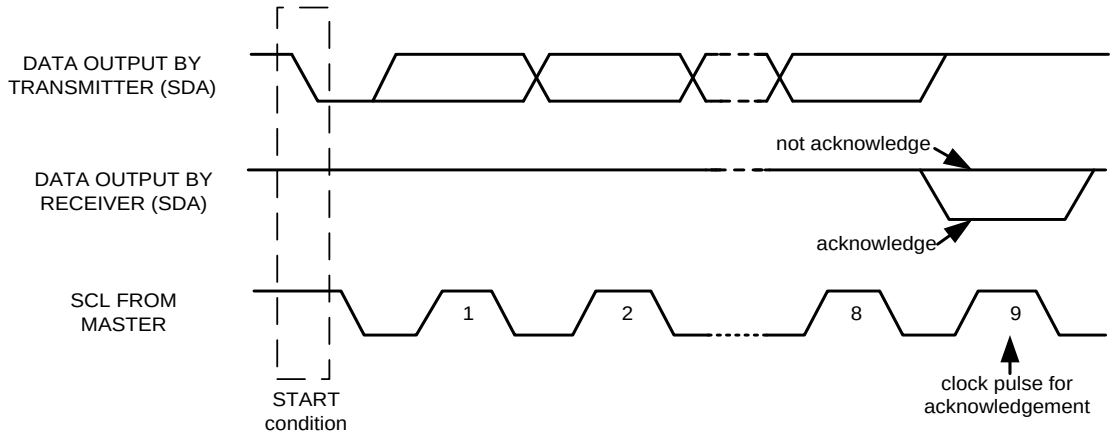



**Figure 9. Acknowledge on the I²C Bus**

*Communications*

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

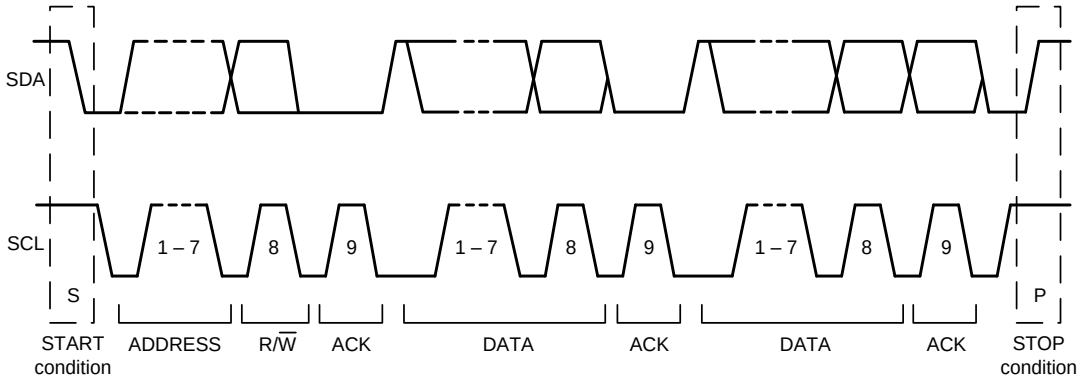



**Figure 10. Complete I²C Data Transfer**

To write the internal IAM-20380HT registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the IAM-20380HT acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the IAM-20380HT acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be

concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the IAM-20380HT automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

*Single-Byte Write Sequence*

| Master | S | AD+W | | RA | | DATA | | P |
|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | ACK | |

*Burst Write Sequence*

| Master | S | AD+W | | RA | | DATA | | DATA | | P |
|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | ACK | | ACK | |

To read the internal IAM-20380HT registers, the master sends a start condition, followed by the $I^2C$ address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the IAM-20380HT, the master transmits a start signal followed by the slave address and read bit. As a result, the IAM-20380HT sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9$^{th}$ clock cycle. The following figures show single and two-byte read sequences.

*Single-Byte Read Sequence*

| Master | S | AD+W | | RA | | S | AD+R | | | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | |

*Burst Read Sequence*

| Master | S | AD+W | | RA | | S | AD+R | | | ACK | | NACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | ACK | | ACK | | | ACK | DATA | | DATA | | |

## 6.4 $I^2C$ TERMS

| SIGNAL | DESCRIPTION |
|---|---|
| S | Start Condition: SDA goes from high to low while SCL is high |
| AD | Slave $I^2C$ address |
| W | Write bit (0) |
| R | Read bit (1) |
| ACK | Acknowledge: SDA line is low while the SCL line is high at the 9$^{th}$ clock cycle |
| NACK | Not-Acknowledge: SDA line stays high at the 9$^{th}$ clock cycle |
| RA | IAM-20380HT internal register address |
| DATA | Transmit or received data |
| P | Stop condition: SDA going from low to high while SCL is high |

**Table 14. $I^2C$ Terms**

## 6.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The IAM-20380HT always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SPC), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

*SPI Operational Features*

1. Data are delivered MSB first and LSB last
2. Data are latched on the rising edge of SPC
3. Data should be transitioned on the falling edge of SPC
4. The maximum frequency of SPC is 8 MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data are two or more bytes:

*SPI Address format*

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| R/W | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

*SPI Data format*

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

6. Supports Single or Burst Read/Writes.

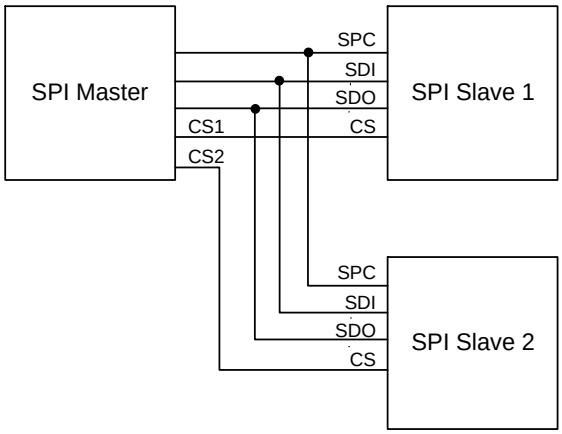



**Figure 11. Typical SPI Master/Slave Configuration**

# 7 SERIAL INTERFACE CONSIDERATIONS

## 7.1 IAM-20380HT SUPPORTED INTERFACES

The IAM-20380HT supports $I^2C$ communications on its serial interface.

The IAM-20380HT's I/O logic levels are set to be VDDIO.

Figure 12 depicts a sample circuit of IAM-20380HT. It shows the relevant logic levels and voltage connections.

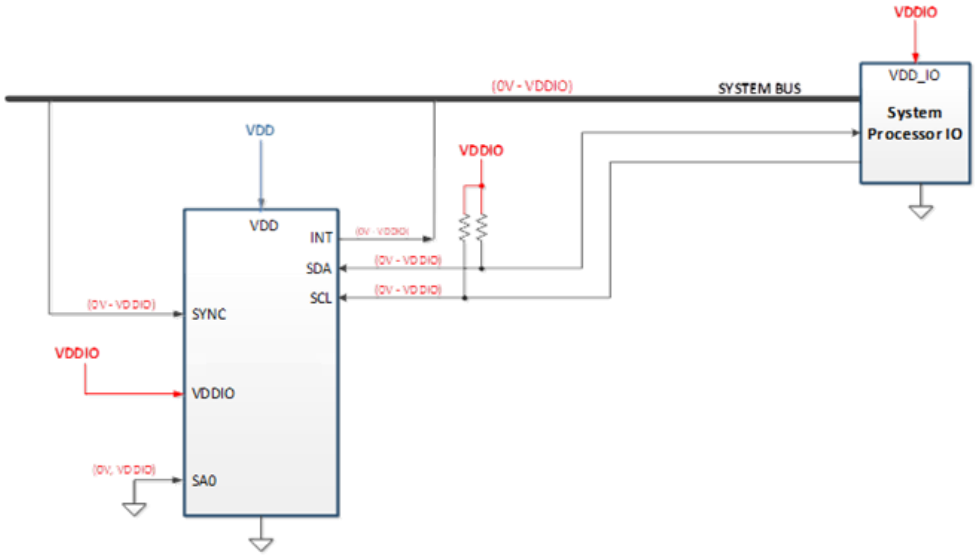



**Figure 12. I/O Levels and Connections**

# 8 REGISTER MAP

The following table lists the register map for the IAM-20380HT.

| Addr (Hex) | Addr (Dec.) | Register Name | Serial I/F | Accessible (writable) in Sleep Mode | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 00 | SELF_TEST_X_GYRO | R/W | N | XG_ST_DATA[7:0] | | | | | | | |
| 01 | 01 | SELF_TEST_Y_GYRO | R/W | N | YG_ST_DATA[7:0] | | | | | | | |
| 02 | 02 | SELF_TEST_Z_GYRO | R/W | N | ZG_ST_DATA[7:0] | | | | | | | |
| 13 | 19 | XG_OFFS_USRH | R/W | N | X_OFFS_USR [15:8] | | | | | | | |
| 14 | 20 | XG_OFFS_USRL | R/W | N | X_OFFS_USR [7:0] | | | | | | | |
| 15 | 21 | YG_OFFS_USRH | R/W | N | Y_OFFS_USR [15:8] | | | | | | | |
| 16 | 22 | YG_OFFS_USRL | R/W | N | Y_OFFS_USR [7:0] | | | | | | | |
| 17 | 23 | ZG_OFFS_USRH | R/W | N | Z_OFFS_USR [15:8] | | | | | | | |
| 18 | 24 | ZG_OFFS_USRL | R/W | N | Z_OFFS_USR [7:0] | | | | | | | |
| 19 | 25 | SMPLRT_DIV | R/W | N | SMPLRT_DIV[7:0] | | | | | | | |
| 1A | 26 | CONFIG | R/W | N | - | FIFO_MODE | EXT_SYNC_SET[2:0] | | | DLPF_CFG[2:0] | | |
| 1B | 27 | GYRO_CONFIG | R/W | N | XG_ST | YG_ST | ZG_ST | FS_SEL [1:0] | | - | FCHOICE_B[1:0] | |
| 1D | 29 | FIFO_SIZE_CONFIG | R/W | N | FIFO_SIZE[1:0] | | - | | | | | |
| 1E | 30 | LP_MODE_CFG | R/W | N | GYRO_CYCLE | G_AVGCFG[2:0] | | | - | | | |
| 23 | 35 | FIFO_EN | R/W | N | TEMP_FIFO_EN | XG_FIFO_EN | YG_FIFO_EN | ZG_FIFO_EN | - | | | |
| 36 | 54 | FSYNC_INT | R/C | N | FSYNC_INT | - | | | | | | |
| 37 | 55 | INT_PIN_CFG | R/W | Y | INT_LEVEL | INT_OPEN | LATCH_INT_EN | INT_RD_CLEAR | FSYNC_INT_LEVEL | FSYNC_INT_MODE_EN | - | INT2_EN |
| 38 | 56 | INT_ENABLE | R/W | Y | - | | | FIFO_OFLOW_EN | - | GDRIVE_INT_EN | - | DATA_RDY_INT_EN |
| 3A | 58 | INT_STATUS | R/C | N | - | | | FIFO_OFLOW_INT | - | GDRIVE_INT | - | DATA_RDY_INT |
| 41 | 65 | TEMP_OUT_H | R | N | TEMP_OUT[15:8] | | | | | | | |
| 42 | 66 | TEMP_OUT_L | R | N | TEMP_OUT[7:0] | | | | | | | |
| 43 | 67 | GYRO_XOUT_H | R | N | GYRO_XOUT[15:8] | | | | | | | |
| 44 | 68 | GYRO_XOUT_L | R | N | GYRO_XOUT[7:0] | | | | | | | |
| 45 | 69 | GYRO_YOUT_H | R | N | GYRO_YOUT[15:8] | | | | | | | |
| 46 | 70 | GYRO_YOUT_L | R | N | GYRO_YOUT[7:0] | | | | | | | |
| 47 | 71 | GYRO_ZOUT_H | R | N | GYRO_ZOUT[15:8] | | | | | | | |
| 48 | 72 | GYRO_ZOUT_L | R | N | GYRO_ZOUT[7:0] | | | | | | | |
| 68 | 104 | SIGNAL_PATH_RESET | R/W | N | - | | | | | | | TEMP_RST |
| 6A | 106 | USER_CTRL | R/W | N | - | FIFO_EN | - | I2C_IF_DIS | - | FIFO_RST | - | SIG_COND_RST |
| 6B | 107 | PWR_MGMT_1 | R/W | Y | DEVICE_RESET | SLEEP | - | GYRO_STANDBY | TEMP_DIS | CLKSEL[2:0] | | |
| 6C | 108 | PWR_MGMT_2 | R/W | Y | FIFO_LP_EN | - | - | - | - | STBY_XG | STBY_YG | STBY_ZG |
| 72 | 114 | FIFO_COUNTH | R | N | - | | | FIFO_COUNT[12:8] | | | | |
| 73 | 115 | FIFO_COUNTL | R | N | FIFO_COUNT[7:0] | | | | | | | |
| 74 | 116 | FIFO_R_W | R/W | N | FIFO_DATA[7:0] | | | | | | | |
| 75 | 117 | WHO_AM_I | R | N | WHOAMI[7:0] | | | | | | | |

**Table 15. Register Map**

**Note:** Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables, register names are in capital letters, while register values are in capital letters and italicized. For example, the GYRO_XOUT_H register (Register 67) contains the 8 most significant bits, *GYRO_XOUT[15:8]*, of the 16-bit X-Axis gyroscope measurement, *GYRO_XOUT*.

The reset value is 0x00 for all registers other than the registers below:

- Self-test registers 0, 1, 2, contain pre-programmed values
- Register 107, PWR_MGMT_1 = 0x01
- Register 117, WHO_AM_I: (default value is reported in section 9.26)

# 9 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the IAM-20380HT.

**Note**: The device will come up in 3-axis Low-Noise Mode upon power-up.

## 9.1 REGISTERS 0 TO 2 – GYROSCOPE SELF-TEST REGISTERS

**Register Name: SELF_TEST_X_GYRO, SELF_TEST_Y_GYRO, SELF_TEST_Z_GYRO**

**Type: READ/WRITE**

**Register Address: 00, 01, 02 (Decimal); 00, 01, 02 (Hex)**

| REGISTER | BIT | NAME | FUNCTION |
|---|---|---|---|
| SELF_TEST_X_GYRO | [7:0] | XG_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |
| SELF_TEST_Y_GYRO | [7:0] | YG_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |
| SELF_TEST_Z_GYRO | [7:0] | ZG_ST_DATA[7:0] | The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user. |

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}\right) + 1$$

## 9.2 REGISTER 19 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: XG_OFFS_USRH**

**Register Type: READ/WRITE**

**Register Address: 19 (Decimal); 13 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | X_OFFS_USR[15:8] | Bits 15 to 8 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 9.3 REGISTER 20 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: XG_OFFS_USRL**

**Register Type: READ/WRITE**

**Register Address: 20 (Decimal); 14 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | X_OFFS_USR[7:0] | Bits 7 to 0 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 9.4 REGISTER 21 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: YG_OFFS_USRH**

**Register Type: READ/WRITE**

**Register Address: 21 (Decimal); 15 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | Y_OFFS_USR[15:8] | Bits 15 to 8 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 9.5 REGISTER 22 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: YG_OFFS_USRL**

**Register Type: READ/WRITE**

**Register Address: 22 (Decimal); 16 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | Y_OFFS_USR[7:0] | Bits 7 to 0 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 9.6 REGISTER 23 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: ZG_OFFS_USRH**

**Register Type: READ/WRITE**

**Register Address: 23 (Decimal); 17 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | Z_OFFS_USR[15:8] | Bits 15 to 8 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 9.7 REGISTER 24 – GYRO OFFSET ADJUSTMENT REGISTER

**Register Name: ZG_OFFS_USRL**

**Register Type: READ/WRITE**

**Register Address: 24 (Decimal); 18 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | Z_OFFS_USR[7:0] | Bits 7 to 0 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. |

## 9.8 REGISTER 25 – SAMPLE RATE DIVIDER

**Register Name: SMPLRT_DIV**

**Register Type: READ/WRITE**

**Register Address: 25 (Decimal); 19 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | SMPLRT_DIV[7:0] | Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate.<br>**Note**: This register is only effective when FCHOICE_B register bits are 2'b00, and (0 < DLPF_CFG < 7).<br>This is the update rate of the sensor register:<br>SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV)<br>Where INTERNAL_SAMPLE_RATE = 1 kHz |

## 9.9 REGISTER 26 – CONFIGURATION

**Register Name: CONFIG**

**Register Type: READ/WRITE**

**Register Address: 26 (Decimal); 1A (Hex)**

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>[7]</td><td>-</td><td>Always set to 0</td></tr>
<tr><td>[6]</td><td>FIFO_MODE</td><td>When set to '1', when the FIFO is full, additional writes will not be written to FIFO.<br>When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.</td></tr>
<tr><td>[5:3]</td><td>EXT_SYNC_SET[2:0]</td><td>Enables the FSYNC pin data to be sampled.
<table>
<tr><th>EXT_SYNC_SET</th><th>FSYNC bit location</th></tr>
<tr><td>0</td><td>function disabled</td></tr>
<tr><td>1</td><td>TEMP_OUT_L[0]</td></tr>
<tr><td>2</td><td>GYRO_XOUT_L[0]</td></tr>
<tr><td>3</td><td>GYRO_YOUT_L[0]</td></tr>
<tr><td>4</td><td>GYRO_ZOUT_L[0]</td></tr>
<tr><td>5</td><td>RESERVED</td></tr>
<tr><td>6</td><td>RESERVED</td></tr>
<tr><td>7</td><td>RESERVED</td></tr>
</table>
FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.</td></tr>
<tr><td>[2:0]</td><td>DLPF_CFG[2:0]</td><td>For the DLPF to be used, FCHOICE_B[1:0] is 2'b00.<br>See Table 16.</td></tr>
</table>

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in Table 16.

| FCHOICE_B | | DLPF_CFG | Gyroscope | | | Temperature Sensor |
|---|---|---|---|---|---|---|
| <1> | <0> | | 3-dB BW (Hz) | Noise BW (Hz) | Rate (kHz) | 3-dB BW (Hz) |
| X | 1 | X | 8173 | 8595.1 | 32 | 4000 |
| 1 | 0 | X | 3281 | 3451.0 | 32 | 4000 |
| 0 | 0 | 0 | 250 | 306.6 | 8 | 4000 |
| 0 | 0 | 1 | 176 | 177.0 | 1 | 188 |
| 0 | 0 | 2 | 92 | 108.6 | 1 | 98 |
| 0 | 0 | 3 | 41 | 59.0 | 1 | 42 |
| 0 | 0 | 4 | 20 | 30.5 | 1 | 20 |
| 0 | 0 | 5 | 10 | 15.6 | 1 | 10 |
| 0 | 0 | 6 | 5 | 8.0 | 1 | 5 |
| 0 | 0 | 7 | 3281 | 3451.0 | 8 | 4000 |

**Table 16. Gyroscope and Temperature Sensor Data Rates and Bandwidths (Low-Noise Mode)**

## 9.10 REGISTER 27 – GYROSCOPE CONFIGURATION

**Register Name: GYRO_CONFIG**

**Register Type: READ/WRITE**

**Register Address: 27 (Decimal); 1B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | XG_ST | X Gyro self-test |
| [6] | YG_ST | Y Gyro self-test |
| [5] | ZG_ST | Z Gyro self-test |
| [4:3] | FS_SEL[1:0] | Gyro Full Scale Select:<br>00 = ±250 dps<br>01= ±500 dps<br>10 = ±1000 dps<br>11 = ±2000 dps |
| [2] | - | Reserved |
| [1:0] | FCHOICE_B[1:0] | Used to bypass DLPF as shown in Table 16 above. |

## 9.11 REGISTER 29 – FIFO SIZE CONFIGURATION

**Register Name: FIFO_SIZE_CONFIG**

**Register Type: READ/WRITE**

**Register Address: 29 (Decimal); 1D (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:6] | FIFO_SIZE[1:0] | Specifies FIFO size according to the following:<br>0 = 512 Byte<br>1 = 1 kByte<br>2 = 2 kByte<br>3 = 4 kByte |
| [5:0] | - | RESERVED |

## 9.12 REGISTER 30 – LOW POWER MODE CONFIGURATION

**Register Name: LP_MODE_CFG**

**Register Type: READ/WRITE**

**Register Address: 30 (Decimal); 1E (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | GYRO_CYCLE [1] | When set to '1' gyroscope or 3-axis are duty-cycled. Default setting is '0' |
| [6:4] | G_AVGCFG[2:0] | Gyroscope averaging filter settings when GYRO_CYCLE is set to '1'. Default setting is '000' |
| [3:0] | - | RESERVED |

To reduce gyroscope power consumption, GYRO_CYCLE should be set to '1'. When GYRO_CYCLE is set to '1' gyroscope is duty-cycled and performance are reduced compared to Low-Noise mode. When GYRO_CYCLE is set to '1' gyroscope filter configuration is determined by G_AVGCFG[2:0] that sets the averaging filter configuration, gyroscope filter is not dependent on DLPF_CFG[2:0]. Table 17 shows some example configurations when GYRO_CYCLE is set to '1'.

| **FCHOICE_B** | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| **G_AVGCFG** | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| **Averages** | | 1x | 2x | 4x | 8x | 16x | 32x | 64x | 128x |
| **Ton (ms)** | | 1.73 | 2.23 | 3.23 | 5.23 | 9.23 | 17.23 | 33.23 | 65.23 |
| **Noise BW (Hz)** | | 650.8 | 407.1 | 224.2 | 117.4 | 60.2 | 30.6 | 15.6 | 8.0 |
| **Noise (dps rms) TYP [1] Based on 0.008 dps/√Hz** | | 0.20 | 0.16 | 0.12 | 0.09 | 0.06 | 0.04 | 0.03 | 0.02 |
| **SMPLRT_DIV** | **ODR (Hz)** | **Current Consumption (mA) TYP [1]** | | | | | | | |
| 255 | 3.9 | 1.3 | 1.3 | 1.3 | 1.3 | 1.4 | 1.4 | 1.5 | 1.8 |
| 99 | 10.0 | 1.3 | 1.3 | 1.4 | 1.4 | 1.5 | 1.6 | 1.9 | 2.5 |
| 64 | 15.4 | 1.4 | 1.4 | 1.4 | 1.5 | 1.6 | 1.8 | 2.2 | N/A |
| 32 | 30.3 | 1.4 | 1.4 | 1.5 | 1.6 | 1.8 | 2.2 | N/A | |
| 19 | 50.0 | 1.5 | 1.5 | 1.6 | 1.8 | 2.1 | 2.8 | | |
| 9 | 100.0 | 1.6 | 1.7 | 1.9 | 2.2 | 3.0 | N/A | | |
| 7 | 125.0 | 1.7 | 1.8 | 2.0 | 2.5 | N/A | | | |
| 4 | 200.0 | 1.9 | 2.1 | 2.5 | N/A | | | | |
| 3 | 250.0 | 2.1 | 2.3 | 2.7 | | | | | |
| 2 | 333.3 | 2.3 | 2.6 | N/A | | | | | |
| 1 | 500.0 | 2.9 | N/A | | | | | | |

**Table 17. Example Configurations for Gyroscope when GYRO_CYCLE = 1**

**Notes**:

1. Not tested in production, not guaranteed

## 9.13 REGISTER 35 – FIFO ENABLE

**Register Name: FIFO_EN**

**Register Type: READ/WRITE**

**Register Address: 35 (Decimal); 23 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | TEMP_FIFO_EN | 1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled. |
| [6] | XG_FIFO_EN | 1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled. |
| [5] | YG_FIFO_EN | 1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled.<br>**Note**: Enabling any one of the bits corresponding to the Gyros or Temp data paths, data are buffered into the FIFO even though that data path is not enabled. |
| [4] | ZG_FIFO_EN | 1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby.<br>0 – Function is disabled |
| [3:0] | - | Reserved. |

## 9.14 REGISTER 54 – FSYNC INTERRUPT STATUS

**Register Name: FSYNC_INT**

**Register Type: READ to CLEAR**

**Register Address: 54 (Decimal); 36 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | FSYNC_INT | This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read. |

## 9.15 REGISTER 55 – INT/INT2 PIN / BYPASS ENABLE CONFIGURATION

**Register Name: INT_PIN_CFG**

**Register Type: READ/WRITE**

**Register Address: 55 (Decimal); 37 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | INT_LEVEL | 1 – The logic level for INT/INT2 pin is active low.<br>0 – The logic level for INT/INT2 pin is active high. |
| [6] | INT_OPEN | 1 – INT/INT2 pin is configured as open drain.<br>0 – INT/INT2 pin is configured as push-pull. |
| [5] | LATCH_INT_EN | 1 – INT/INT2 pin level held until interrupt status is cleared.<br>0 – INT/INT2 pin indicates interrupt pulse's width is 50 µs. |
| [4] | INT_RD_CLEAR | 1 – Interrupt status is cleared if any read operation is performed.<br>0 – Interrupt status is cleared only by reading INT_STATUS register |
| [3] | FSYNC_INT_LEVEL | 1 – The logic level for the FSYNC pin as an interrupt is active low.<br>0 – The logic level for the FSYNC pin as an interrupt is active high. |
| [2] | FSYNC_INT_MODE_EN | When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by F*SYNC_INT_LEVEL*. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt. |
| [1] | - | Reserved. |
| [0] | INT2_EN | When INT2_EN = 0, all of the interrupts appear on the INT pin, and INT2 interrupt pin is unused. When INT2_EN = 1, all interrupts except for data ready appear on the INT2 pin, and data ready interrupt appears on the INT interrupt pin. |

## 9.16 REGISTER 56 – INTERRUPT ENABLE

**Register Name: INT_ENABLE**

**Register Type: READ/WRITE**

**Register Address: 56 (Decimal); 38 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:5] | - | Reserved |
| [4] | FIFO_OFLOW_EN | 1 – Enables a FIFO buffer overflow to generate an interrupt.<br>0 – Function is disabled. |
| [3] | - | Reserved. |
| [2] | GDRIVE_INT_EN | Gyroscope Drive System Ready interrupt enable. |
| [1] | - | Reserved. |
| [0] | DATA_RDY_INT_EN | Data ready interrupt enable. |

Data ready interrupt is always generated on INT pin. All the other interrupts signals are generated on INT pin if INT2_EN bit is set to 0 or on INT2 pin if INT2_EN bit is set to 1.

## 9.17 REGISTER 58 – INTERRUPT STATUS

**Register Name: INT_STATUS**

**Register Type: READ to CLEAR**

**Register Address: 58 (Decimal); 3A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:5] | - | Reserved |
| [4] | FIFO_OFLOW_INT | This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read. |
| [3] | - | Reserved. |
| [2] | GDRIVE_INT | Gyroscope Drive System Ready interrupt |
| [1] | - | Reserved. |
| [0] | DATA_RDY_INT | This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read. |

## 9.18 REGISTERS 65 AND 66 – TEMPERATURE MEASUREMENT

**Register Name: TEMP_OUT_H**

**Register Type: READ only**

**Register Address: 65 (Decimal); 41 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | TEMP_OUT[15:8] | High byte of the temperature sensor output. |

**Register Name: TEMP_OUT_L**

**Register Type: READ only**

**Register Address: 66 (Decimal); 42 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | TEMP_OUT[7:0] | Low byte of the temperature sensor output<br>**TEMP_degC** = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 25degC |

## 9.19 REGISTERS 67 TO 72 – GYROSCOPE MEASUREMENTS

**Register Name: GYRO_XOUT_H**

**Register Type: READ only**

**Register Address: 67 (Decimal); 43 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_XOUT[15:8] | High byte of the X-Axis gyroscope output. |

**Register Name: GYRO_XOUT_L**

**Register Type: READ only**

**Register Address: 68 (Decimal); 44 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_XOUT[7:0] | Low byte of the X-Axis gyroscope output.<br>**GYRO_XOUT =** Gyro_Sensitivity * X_angular_rate<br>Nominal Conditions: FS_SEL = 0, Gyro_Sensitivity = 131 LSB/(dps) |

**Register Name: GYRO_YOUT_H**

**Register Type: READ only**

**Register Address: 69 (Decimal); 45 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_YOUT[15:8] | High byte of the Y-Axis gyroscope output. |

**Register Name: GYRO_YOUT_L**

**Register Type: READ only**

**Register Address: 70 (Decimal); 46 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_YOUT[7:0] | Low byte of the Y-Axis gyroscope output.<br>**GYRO_YOUT =** Gyro_Sensitivity * Y_angular_rate<br>Nominal Conditions: FS_SEL = 0, Gyro_Sensitivity = 131 LSB/(dps) |

**Register Name: GYRO_ZOUT_H**

**Register Type: READ only**

**Register Address: 71 (Decimal); 47 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_ZOUT[15:8] | High byte of the Z-Axis gyroscope output. |

**Register Name: GYRO_ZOUT_L**

**Register Type: READ only**

**Register Address: 72 (Decimal); 48 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | GYRO_ZOUT[7:0] | Low byte of the Z-Axis gyroscope output.<br>**GYRO_ZOUT =** Gyro_Sensitivity * Z_angular_rate<br>Nominal Conditions: FS_SEL = 0, Gyro_Sensitivity = 131 LSB/(dps) |

## 9.20 REGISTER 104 – SIGNAL PATH RESET

**Register Name: SIGNAL_PATH_RESET**

**Register Type: READ/WRITE**

**Register Address: 104 (Decimal); 68 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:1] | - | Reserved. |
| [0] | TEMP_RST | Reset temp digital signal path.<br>**Note**: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers. |

## 9.21 REGISTER 106 – USER CONTROL

**Register Name: USER_CTRL**

**Register Type: READ/WRITE**

**Register Address: 106 (Decimal); 6A (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | - | Reserved. |
| [6] | FIFO_EN | 1 – Enable FIFO operation mode.<br>0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register. |
| [5] | - | Reserved. |
| [4] | I2C_IF_DIS | 1 – Disable I²C Slave module and put the serial interface in SPI mode only. |
| [3] | - | Reserved. |
| [2] | FIFO_RST | 1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock. |
| [1] | - | Reserved. |
| [0] | SIG_COND_RST | 1 – Reset all gyro digital signal path and temp digital signal path. This bit also clears all the sensor registers. |

## 9.22 REGISTER 107 – POWER MANAGEMENT 1

**Register Name: PWR_MGMT_1**

**Register Type: READ/WRITE**

**Register Address: 107 (Decimal); 6B (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7] | DEVICE_RESET | 1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done. |
| [6] | SLEEP | When set to 1, the chip is set to sleep mode. Default setting is 0. |
| [5] | - | Reserved |
| [4] | GYRO_STANDBY | When set, the gyro drive and PLL circuitry are enabled, but the sense paths are disabled. This is a power mode that allows quick enabling of the gyros. |
| [3] | TEMP_DIS | When set to 1, this bit disables the temperature sensor. |
| [2:0] | CLKSEL[2:0] | |

| Code | Clock Source |
|---|---|
| 0 | Internal 20 MHz oscillator. |
| 1 | Auto selects the best available clock source – PLL if ready, else use the Internal oscillator |
| 2 | Auto selects the best available clock source – PLL if ready, else use the Internal oscillator |
| 3 | Auto selects the best available clock source – PLL if ready, else use the Internal oscillator |
| 4 | Auto selects the best available clock source – PLL if ready, else use the Internal oscillator |
| 5 | Auto selects the best available clock source – PLL if ready, else use the Internal oscillator |
| 6 | Internal 20 MHz oscillator. |
| 7 | Stops the clock and keeps timing generator in reset. |

**Note**: The default value of CLKSEL[2:0] is 001.

## 9.23 REGISTER 108 – POWER MANAGEMENT 2

**Register Name: PWR_MGMT_2**

**Register Type: READ/WRITE**

**Register Address: 108 (Decimal); 6C (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:3] | - | Reserved |
| [2] | STBY_XG | 1 – X gyro is disabled.<br>0 – X gyro is on. |

| BIT | NAME | FUNCTION |
|---|---|---|
| [1] | STBY_YG | 1 – Y gyro is disabled.<br>0 – Y gyro is on. |
| [0] | STBY_ZG | 1 – Z gyro is disabled.<br>0 – Z gyro is on. |

## 9.24 REGISTERS 114 AND 115 – FIFO COUNT REGISTERS

**Register Name: FIFO_COUNTH**

**Register Type: READ Only**

**Register Address: 114 (Decimal); 72 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:5] | - | Reserved. |
| [4:0] | FIFO_COUNT[12:8] | High Bits; count indicates the number of written bytes in the FIFO.<br>Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL. |

**Register Name: FIFO_COUNTL**

**Register Type: READ Only**

**Register Address: 115 (Decimal); 73 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | FIFO_COUNT[7:0] | Low Bits; count indicates the number of written bytes in the FIFO.<br>**Note**: Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL. |

## 9.25 REGISTER 116 – FIFO READ WRITE

**Register Name: FIFO_R_W**

**Register Type: READ/WRITE**

**Register Address: 116 (Decimal); 74 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | FIFO_DATA[7:0] | Read/Write command provides Read or Write operation for the FIFO. |

Description:

This register is used to read and write data from the FIFO buffer.

Data are written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (Registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data are available. Normal data are precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

## 9.26 REGISTER 117 – WHO AM I

**Register Name: WHO_AM_I**

**Register Type: READ only**

**Register Address: 117 (Decimal); 75 (Hex)**

| BIT | NAME | FUNCTION |
|---|---|---|
| [7:0] | WHOAMI | Register to indicate to user which device is being accessed. |

This register is used to verify the identity of the device. The contents of *WHOAMI* is an 8-bit device ID. The default value of the register is 0xFD. This is different from the $I^2C$ address of the device as seen on the slave $I^2C$ controller by the applications processor. The $I^2C$ address of the IAM-20380HT is 0x68 or 0x69 depending upon the value driven on AD0 pin.

# 10 ASSEMBLY

This section provides general guidelines for assembling TDK-InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

## 10.1 ORIENTATION OF AXES

Figure 13 below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

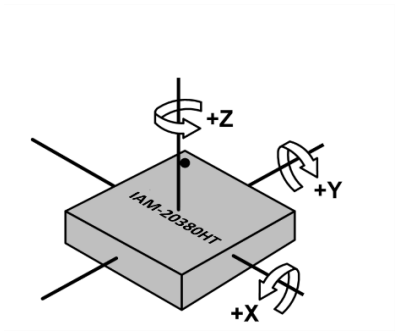



**Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation**

## 10.2 PACKAGE DIMENSIONS

16 Lead LGA 3x3x0.75 mm$^3$ NiAu pad finish.

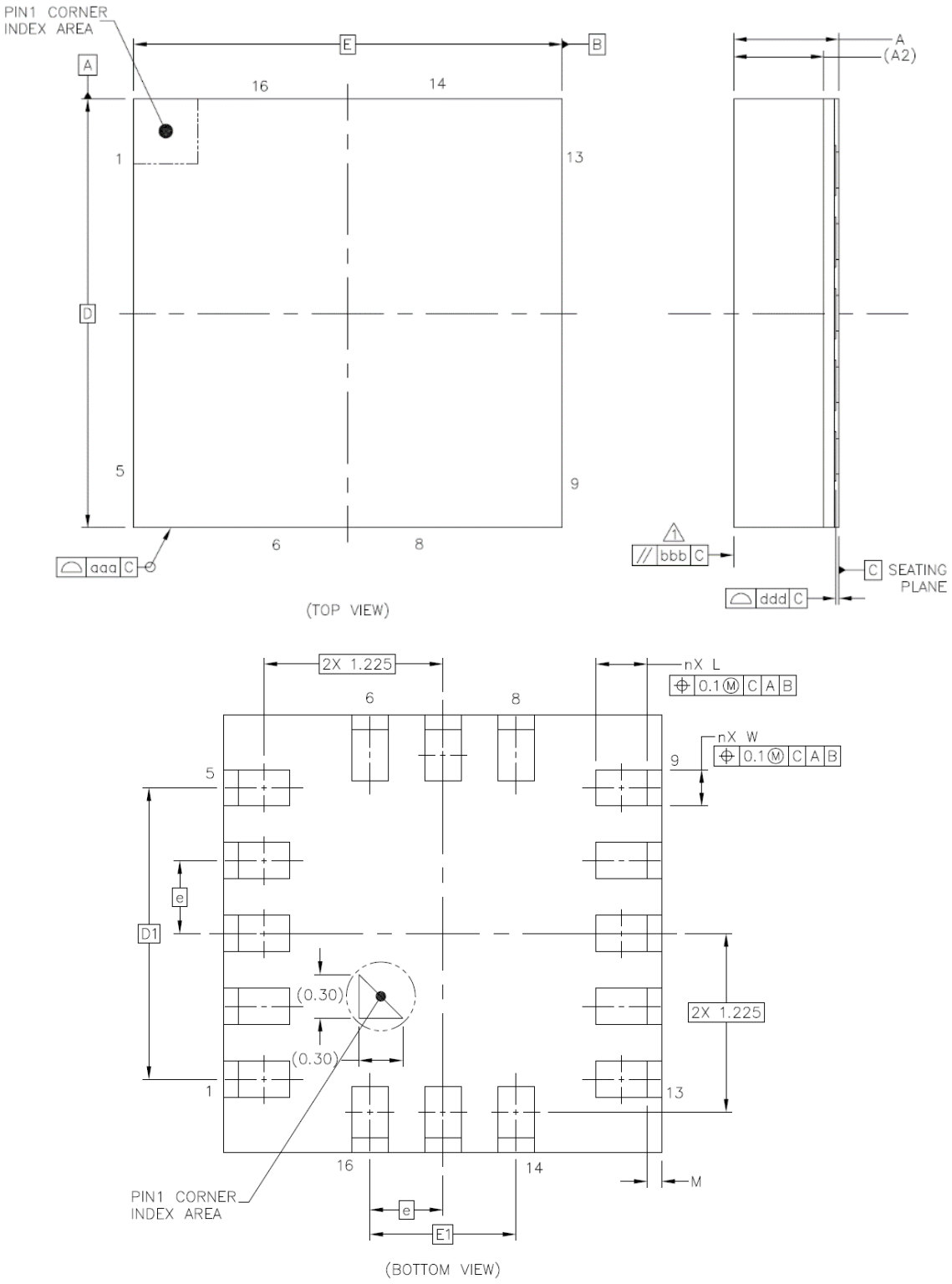



**Figure 14. Package Dimensions**

| | SYMBOLS | DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|---|
| | | MIN | NOM | MAX |
| Total Thickness | A | 0.7 | 0.75 | 0.8 |
| Mold Thickness | A2 | | 0.63 | REF |
| Body Size | D | 2.9 | 3 | 3.1 |
| | E | 2.9 | 3 | 3.1 |
| Lead Width | W | 0.2 | 0.25 | 0.3 |
| Lead Length | L | 0.3 | 0.35 | 0.4 |
| Lead Pitch | e | | 0.5 | BSC |
| Lead Count | n | | 16 | |
| Edge Ball Center to Center | D1 | | 2 | BSC |
| | E1 | | 1 | BSC |
| Body Center to Contact Ball | SD | | --- | BSC |
| | SE | | --- | BSC |
| Ball Width | b | --- | --- | --- |
| Ball Diameter | | | --- | |
| Ball Opening | | | --- | |
| Ball Pitch | e1 | | --- | |
| Ball Count | n1 | | --- | |
| Pre-Solder | | --- | --- | --- |
| Package Edge Tolerance | aaa | | 0.1 | |
| Mold Flatness | bbb | | 0.2 | |
| Coplanarity | ddd | | 0.08 | |
| Ball Offset (Package) | eee | | --- | |
| Ball Offset (Ball) | fff | | --- | |
| Lead Edge to Package Edge | M | 0.05 | 0.1 | 0.15 |

**Table 18. Package Dimensions**

# 11 PART NUMBER PACKAGE MARKING

The part number package marking for IAM-20380HT devices is summarized below:

| PART NUMBER | PART NUMBER PACKAGE MARKING |
|---|---|
| IAM-20380HT | IA238HT |

**Table 19. Part Number Package Marking**

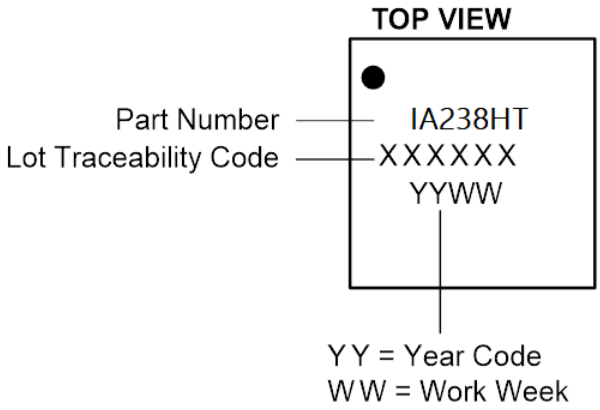



**Figure 15. Part Number Package Marking**

Samples with Part Number Package Marking “IA238HT E” are engineering samples and may have deviations in respect to the specifications and functions reported in the datasheet. Engineering samples are not production-intent parts.

# 12 REFERENCE

Please refer to “InvenSense MEMS Motion Handling and Assembly Guide (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

# 13 REVISION HISTORY

| REVISION DATE | REVISION | DESCRIPTION |
|---|---|---|
| 09/14/2022 | 1.0 | First release |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