DN74LS174 N74LS174

Hex D-type Flip Flops (with Reset)

■ Description

DN74LS174 contains six positive-edge triggered D-type flip-flop circuits with common clock-CP and direct-coupled reset inputs, and independent data-D inputs.

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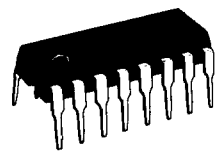

16-pin plastic DIL package

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16-pin Panaflat package (SO-16D)

■ Features

- Positive-edge trigger
- Common clock and direct-coupled reset inputs for all six circuits
- Q output
- Wide operating temperature range (Ta = −20 to +75°C)

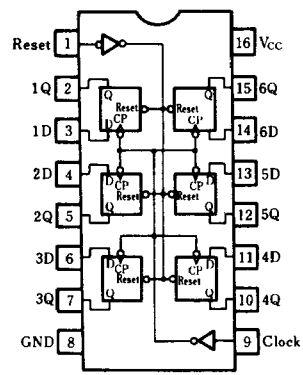
■ Truth tables

Inputs			Outputs
Reset	Clock	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑: Change from LOW to HIGH.
5. Q_0: Q level prior to determination of constant condition input requirement.

Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Clock pulse width		$t_{W\,(CP)}$	20			ns
Reset pulse width		$t_{W\,(Reset)}$	20			ns
Set-up time	Data input	$t_{su\,(D)}$	20			ns
	Reset (non-operating condition)	t_{Reset}	25			ns
Data hold time		$t_{h\,(D)}$	5			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
	V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
	V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Output short circuit current**	I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***	I_{CC}	$V_{CC}=5.25V$			16	26	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

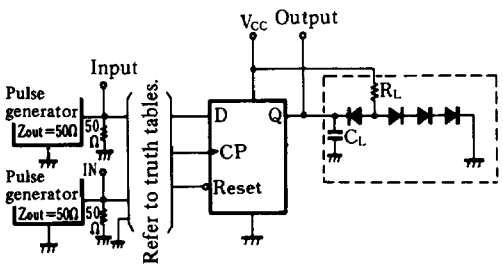
*** Measured with all outputs open and 4.5V applied to all data and reset inputs; clock inputs grounded momentarily, following which they are grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	Q	$C_L=15pF$ $R_L=2k\Omega$	30	40		MHz
Propagation delay time	t_{PHL}	Reset	Q			23	35	ns
	t_{PLH}	Clock	Q			20	30	ns
	t_{PHL}					21	30	ns

※ Switching parameter measurement information

1. Measurement circuit

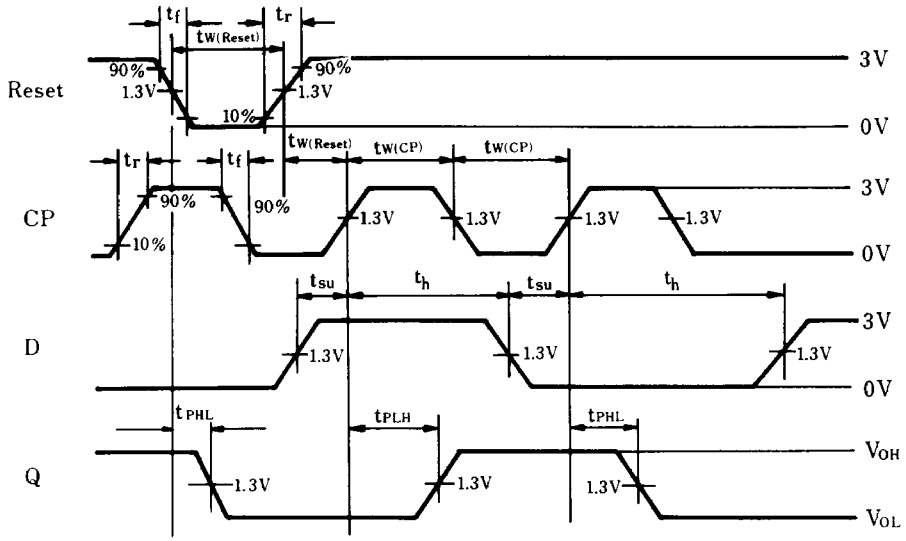


2. Table of measurement requirements

Parameter	Input / Output	Inputs			Outputs
		Reset	Clock	D	Q
f_{max}	CP→Q	4.5V	IN	IN	OUT
t_{PLH}	CP→Q	4.5V	IN	IN	
t_{PHL}	Resct→Q	IN	IN	4.5V	

1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

3.Waveforms



■ Logic diagram