## n FEATURES

- Wide $V_{CC}$ operation voltage : 2.4V ~ 5.5V
- Very low power consumption :
  - $V_{CC}$ = 3.0V Operation current : 18mA (Max.) at 55ns
    2mA (Max.) at 1MHz
    Standby current : 0.02uA (Typ.) at 25°C
  - $V_{CC}$ = 5.0V Operation current : 47mA (Max.) at 55ns
    10mA (Max.) at 1MHz
    Standby current : 0.4uA (Typ.) at 25°C
- High speed access time :
  - -55 55ns (Max.) at $V_{CC}$ : 3.0~5.5V
  - -70 70ns (Max.) at $V_{CC}$ : 2.7~5.5V
- Automatic power down when chip is deselected
- Easy expansion with CE2, CE1 and OE options
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V

## n DESCRIPTION

The BS62LV1027 is a high performance, very low power CMOS Static Random Access Memory organized as 131,072 by 8 bits and operates form a wide range of 2.4V to 5.5V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical CMOS standby current of 0.02uA at 3.0V/25°C and maximum access time of 55ns at 3.0V/85°C.

Easy memory expansion is provided by an active LOW chip enable (CE1), an active HIGH chip enable (CE2), and active LOW output enable (OE) and three-state output drivers.

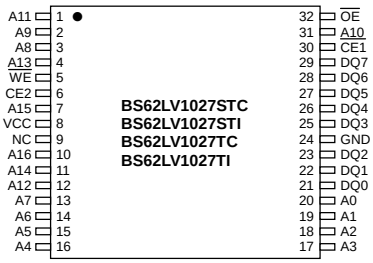
The BS62LV1027 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

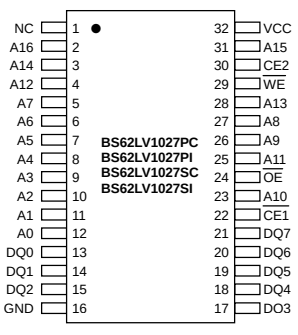
The BS62LV1027 is available in DICE form, JEDEC standard 32 pin 450mil Plastic SOP, 600mil Plastic DIP, 8mmx13.4mm STSOP, 8mmx20mm TSOP and 36-ball BGA package.

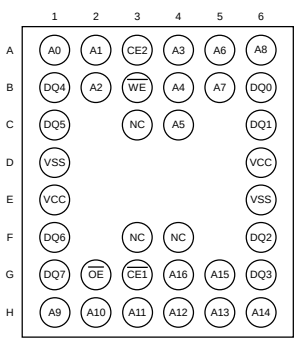
## n POWER CONSUMPTION

| PRODUCT FAMILY | OPERATING TEMPERATURE | POWER DISSIPATION | | | | | | | | PKG TYPE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | STANDBY ($I_{CCSB1}$, Max.) | | Operating ($I_{CC}$, Max.) | | | | | | |
| | | | | $V_{CC}$=5.0V | | | $V_{CC}$=3.0V | | | |
| | | $V_{CC}$=5.0V | $V_{CC}$=3.0V | 1MHz | 10MHz | $f_{Max.}$ | 1MHz | 10MHz | $f_{Max.}$ | |
| BS62LV1027DC | Commercial +0°C to +70°C | 3.0uA | 1.0uA | 9mA | 29mA | 46mA | 1.5mA | 9mA | 17mA | DICE |
| BS62LV1027HC | | | | | | | | | | BGA-36-0608 |
| BS62LV1027PC | | | | | | | | | | PDIP-32 |
| BS62LV1027SC | | | | | | | | | | SOP-32 |
| BS62LV1027STC | | | | | | | | | | STSOP-32 |
| BS62LV1027TC | | | | | | | | | | TSOP-32 |
| BS62LV1027HI | Industrial -40°C to +85°C | 5.0uA | 1.5uA | 10mA | 30mA | 47mA | 2mA | 10mA | 18mA | BGA-36-0608 |
| BS62LV1027PI | | | | | | | | | | PDIP-32 |
| BS62LV1027SI | | | | | | | | | | SOP-32 |
| BS62LV1027STI | | | | | | | | | | STSOP-32 |
| BS62LV1027TI | | | | | | | | | | TSOP-32 |

## n PIN CONFIGURATIONS

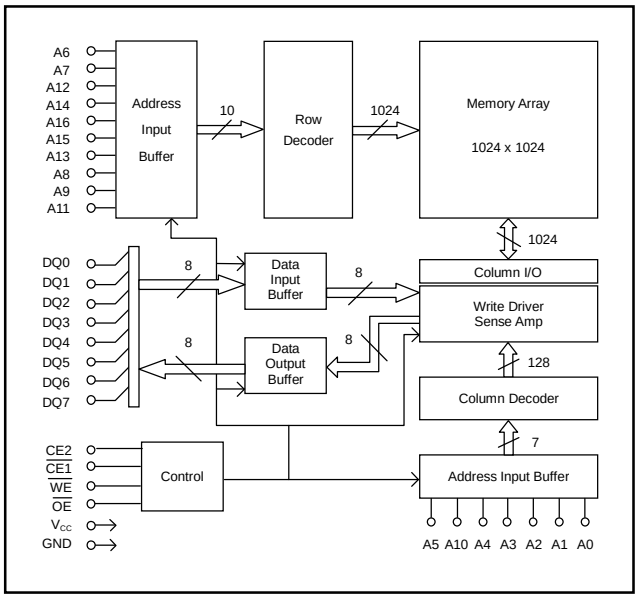



36-ball BGA top view

## n BLOCK DIAGRAM



## n PIN DESCRIPTIONS

| Name | Function |
|---|---|
| **A0-A16 Address Input** | These 17 address inputs select one of the 131,072 x 8-bit in the RAM |
| **$\overline{CE1}$ Chip Enable 1 Input**<br>**CE2 Chip Enable 2 Input** | $\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read form or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected. |
| **$\overline{WE}$ Write Enable Input** | The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location. |
| **$\overline{OE}$ Output Enable Input** | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impendence state when $\overline{OE}$ is inactive. |
| **DQ0-DQ7 Data Input/Output Ports** | There 8 bi-directional ports are used to read data from or write data into the RAM. |
| **$V_{CC}$** | Power Supply |
| **GND** | Ground |

## n TRUTH TABLE

| MODE | $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | I/O OPERATION | $V_{CC}$ CURRENT |
|---|---|---|---|---|---|---|
| Not selected (Power Down) | H | X | X | X | High Z | $I_{CCSB}$, $I_{CCSB1}$ |
| | X | L | X | X | | |
| Output Disabled | L | H | H | H | High Z | $I_{CC}$ |
| Read | L | H | H | L | $D_{OUT}$ | $I_{CC}$ |
| Write | L | H | L | X | $D_{IN}$ | $I_{CC}$ |

## n ABSOLUTE MAXIMUM RATINGS (1)

| SYMBOL | PARAMETER | RATING | UNITS |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5(2) to 7.0 | V |
| $T_{BIAS}$ | Temperature Under Bias | -40 to +125 | $^{O}C$ |
| $T_{STG}$ | Storage Temperature | -60 to +150 | $^{O}C$ |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 20 | mA |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. –2.0V in case of AC pulse width less than 30 ns.

## n OPERATING RANGE

| RANG | AMBIENT TEMPERATURE | $V_{CC}$ |
|---|---|---|
| Commercial | $0^{O}C$ to + $70^{O}C$ | 2.4V ~ 5.5V |
| Industrial | $-40^{O}C$ to + $85^{O}C$ | 2.4V ~ 5.5V |

## n CAPACITANCE (1) ($T_A$ = 25$^{O}$C, f = 1.0MHz)

| SYMBOL | PAMAMETER | CONDITIONS | MAX. | UNITS |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{IO}$ | Input/Output Capacitance | $V_{I/O}$ = 0V | 8 | pF |

1. This parameter is guaranteed and not 100% tested.

## n DC ELECTRICAL CHARACTERISTICS ($T_A$ = -40°C to +85°C)

| PARAMETER NAME | PARAMETER | TEST CONDITIONS | | MIN. | TYP.(1) | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | | | 2.4 | -- | 5.5 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.5(2) | -- | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.2 | -- | $V_{CC}$+0.3(3) | V |
| $I_{IL}$ | Input Leakage Current | $V_{CC}$ = Max, $V_{IN}$ = 0V to $V_{CC}$ | | -- | -- | 1 | uA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max, $\overline{CE1}$= $V_{IH}$, CE2= $V_{IL}$, or $\overline{OE}$ = $V_{IH}$, $V_{I/O}$ = 0V to $V_{CC}$ | | -- | -- | 1 | uA |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ = Max, $I_{OL}$ = 2.0mA | $V_{CC}$=3.0V | -- | -- | 0.4 | V |
| | | | $V_{CC}$=5.0V | | | | |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ = Min, $I_{OH}$ = -1.0mA | $V_{CC}$=3.0V | 2.4 | -- | -- | V |
| | | | $V_{CC}$=5.0V | | | | |
| $I_{CC}$(5) | Operating Power Supply Current | $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$, $I_{DQ}$ = 0mA, f = $f_{Max}$(4) | $V_{CC}$=3.0V | -- | -- | 18 | mA |
| | | | $V_{CC}$=5.0V | -- | -- | 47 | |
| $I_{CC1}$ | Operating Power Supply Current | CE1 = $V_{IL}$, CE2 = $V_{IH}$, $I_{DQ}$ = 0mA, f = 1MHz | $V_{CC}$=3.0V | | | 2 | mA |
| | | | $V_{CC}$=5.0V | | | 10 | |
| $I_{CCSB}$ | Standby Current – TTL | $\overline{CE1}$ = $V_{IH}$, or CE2 = $V_{IL}$, $I_{DQ}$ = 0mA | $V_{CC}$=3.0V | -- | -- | 0.5 | mA |
| | | | $V_{CC}$=5.0V | -- | -- | 1.0 | |
| $I_{CCSB1}$(6) | Standby Current – CMOS | $\overline{CE1}$≧$V_{CC}$-0.2V or CE2≦0.2V, $V_{IN}$≧$V_{CC}$-0.2V or $V_{IN}$≦0.2V | $V_{CC}$=3.0V | -- | 0.02 | 1.5 | uA |
| | | | $V_{CC}$=5.0V | -- | 0.4 | 5.0 | |

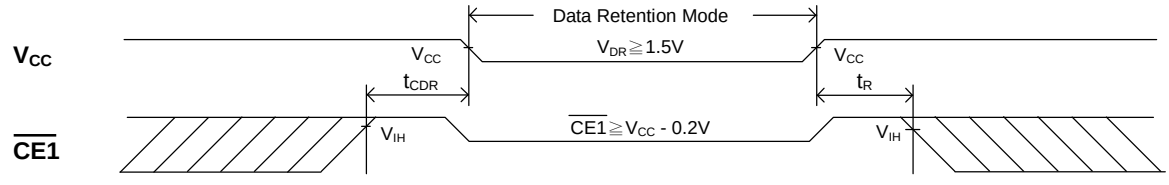
1. Typical characteristics are at $T_A$=25°C and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: $V_{CC}$+1.0V in case of pulse width less than 20 ns.
4. $f_{Max.}$=1/$t_{RC.}$
5. $I_{CC\ (MAX.)}$ is 17mA/46mA at $V_{CC}$=3.0V/5.0V and $T_A$=70°C.
6. $I_{CCSB1(MAX.)}$ is 1.3uA/4.0uA at $V_{CC}$=3.0V/5.0V and $T_A$=70°C.

## n DATA RETENTION CHARACTERISTICS ($T_A$ = -40°C to +85°C)

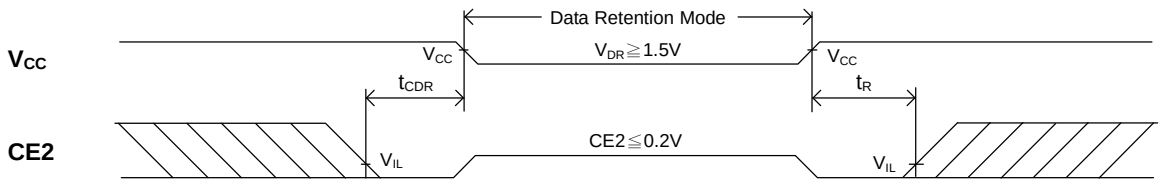
| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | TYP. (1) | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | $\overline{CE1}$≧$V_{CC}$-0.2V or CE2≦0.2V, $V_{IN}$≧$V_{CC}$-0.2V or $V_{IN}$≦0.2V | 1.5 | -- | -- | V |
| $I_{CCDR}$(3) | Data Retention Current | $\overline{CE1}$≧$V_{CC}$-0.2V or CE2≦0.2V, $V_{IN}$≧$V_{CC}$-0.2V or $V_{IN}$≦0.2V | -- | 0.02 | 0.5 | uA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | -- | -- | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$ (2) | -- | -- | ns |

1. $V_{CC}$=1.5V, $T_A$=25°C and not 100% tested.
2. $t_{RC}$ = Read Cycle Time.
3. $I_{CCRD(Max.)}$ is0.3uA at $T_A$=70°C.

## n LOW $V_{CC}$ DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



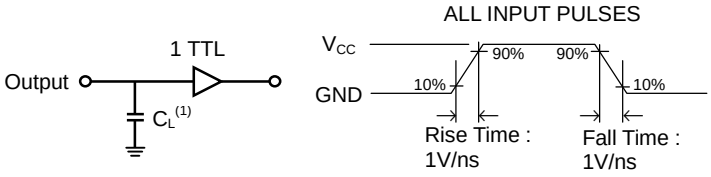
## n LOW $V_{CC}$ DATA RETENTION WAVEFORM (2) (CE2 Controlled)




## n AC TEST CONDITIONS

**(Test Load and Input/Output Reference)**

| | | |
|---|---|---|
| Input Pulse Levels | | Vcc / 0V |
| Input Rise and Fall Times | | 1V/ns |
| Input and Output Timing Reference Level | | 0.5Vcc |
| Output Load | $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{WHZ}$ | $C_L$ = 5pF+1TTL |
| | Others | $C_L$ = 30pF+1TTL |




1. Including jig and scope capacitance.

## n KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | MUST BE STEADY |
| | MAY CHANGE FROM "H" TO "L" | WILL BE CHANGE FROM "H" TO "L" |
| | MAY CHANGE FROM "L" TO "H" | WILL BE CHANGE FROM "L" TO "H" |
| | DON'T CARE ANY CHANGE PERMITTED | CHANGE : STATE UNKNOW |
| | DOES NOT APPLY | CENTER LINE IS HIGH INPEDANCE "OFF" STATE |

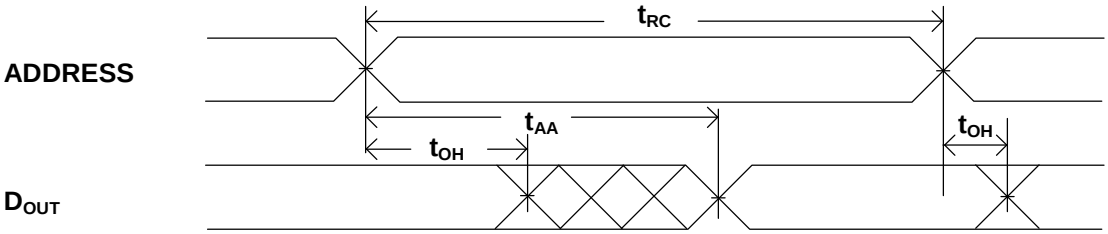
## n AC ELECTRICAL CHARACTERISTICS ($T_A$ = -40°C to +85°C)

### READ CYCLE

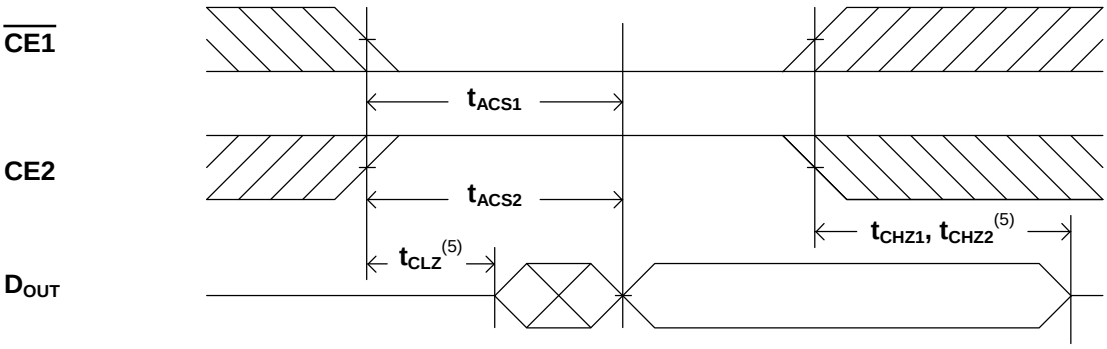
| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | CYCLE TIME : 55ns ($V_{CC}$ = 3.0~5.5V) | | | CYCLE TIME : 70ns ($V_{CC}$ = 2.7~5.5V) | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| $t_{AVAX}$ | $t_{RC}$ | Read Cycle Time | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{AVQX}$ | $t_{AA}$ | Address Access Time | -- | -- | 55 | -- | -- | 70 | ns |
| $t_{E1LQV}$ | $t_{ACS1}$ | Chip Select Access Time ($\overline{CE1}$) | -- | -- | 55 | -- | -- | 70 | ns |
| $t_{E2HQV}$ | $t_{ACS2}$ | Chip Select Access Time (CE2) | -- | -- | 55 | -- | -- | 70 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Valid | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{E1LQX}$ | $t_{CLZ1}$ | Chip Select to Output in Low Z ($\overline{CE1}$) | 10 | -- | -- | 10 | -- | -- | ns |
| $t_{E2HQX}$ | $t_{CLZ2}$ | Chip Select to Output in Low Z (CE2) | 10 | -- | -- | 10 | -- | -- | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable to Output in Low Z | 5 | -- | -- | 5 | -- | -- | ns |
| $t_{E1HQZ}$ | $t_{CHZ1}$ | Chip Deselect to Output in High Z ($\overline{CE1}$) | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{E2LQZ}$ | $t_{CHZ2}$ | Chip Deselect to Output in High Z (CE2) | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{GHQZ}$ | $t_{OHZ}$ | Output Disable to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| $t_{AVQX}$ | $t_{OH}$ | Data Hold from Address Change | 10 | -- | -- | 10 | -- | -- | ns |

## n SWITCHING WAVEFORMS (READ CYCLE)

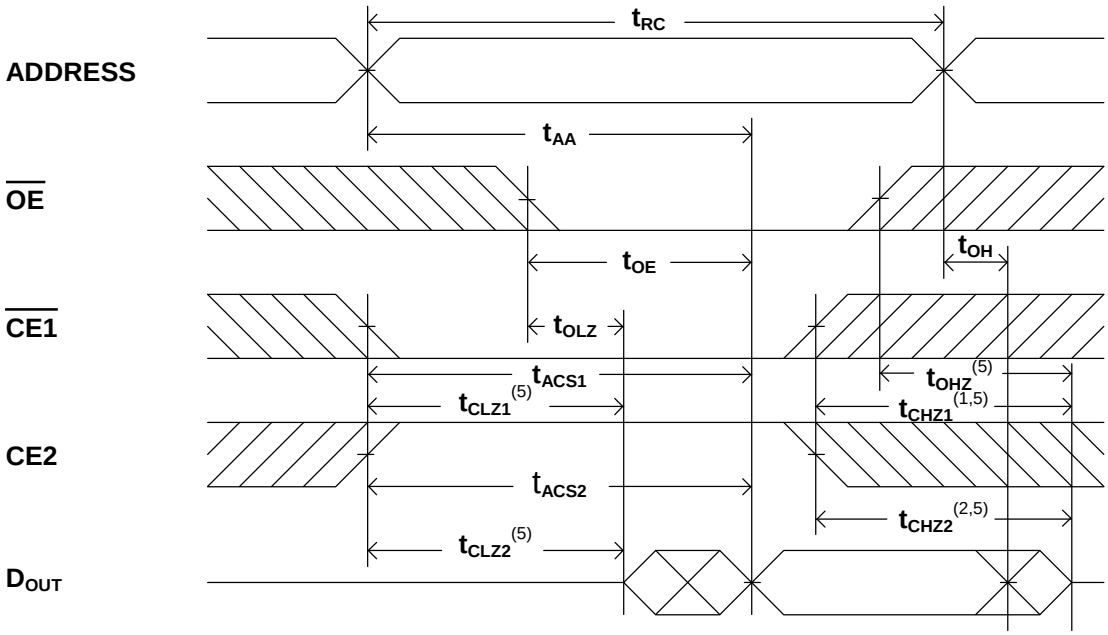
### READ CYCLE 1 (1,2,4)




### READ CYCLE 2 (1,3,4)




### READ CYCLE 3 (1, 4)




NOTES:
1. WE is high in read Cycle.
2. Device is continuously selected when CE1 = $V_{IL}$ and CE2= $V_{IH}$.
3. Address valid prior to or coincident with CE1 transition low and/or CE2 transition high.
4. OE = $V_{IL}$.
5. Transition is measured ± 500mV from steady state with $C_L$ = 5pF.
   The parameter is guaranteed but not 100% tested.

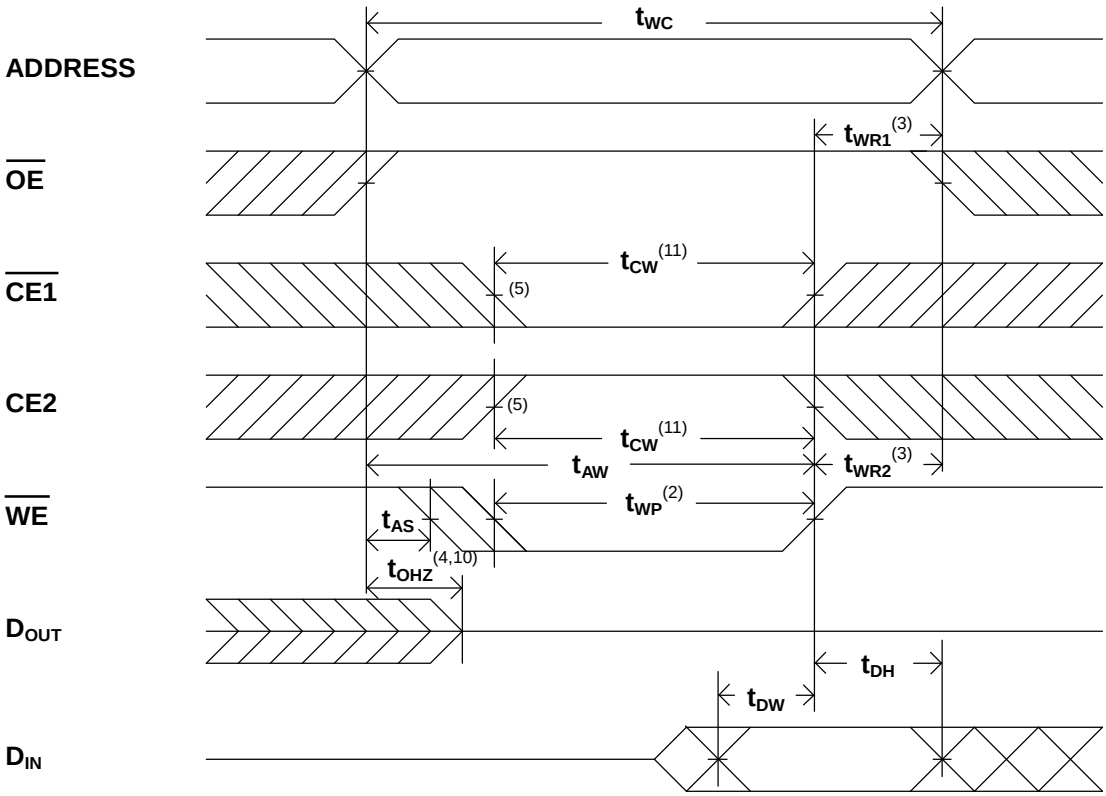
## n AC ELECTRICAL CHARACTERISTICS ($T_A$ = -40°C to +85°C)

### WRITE CYCLE

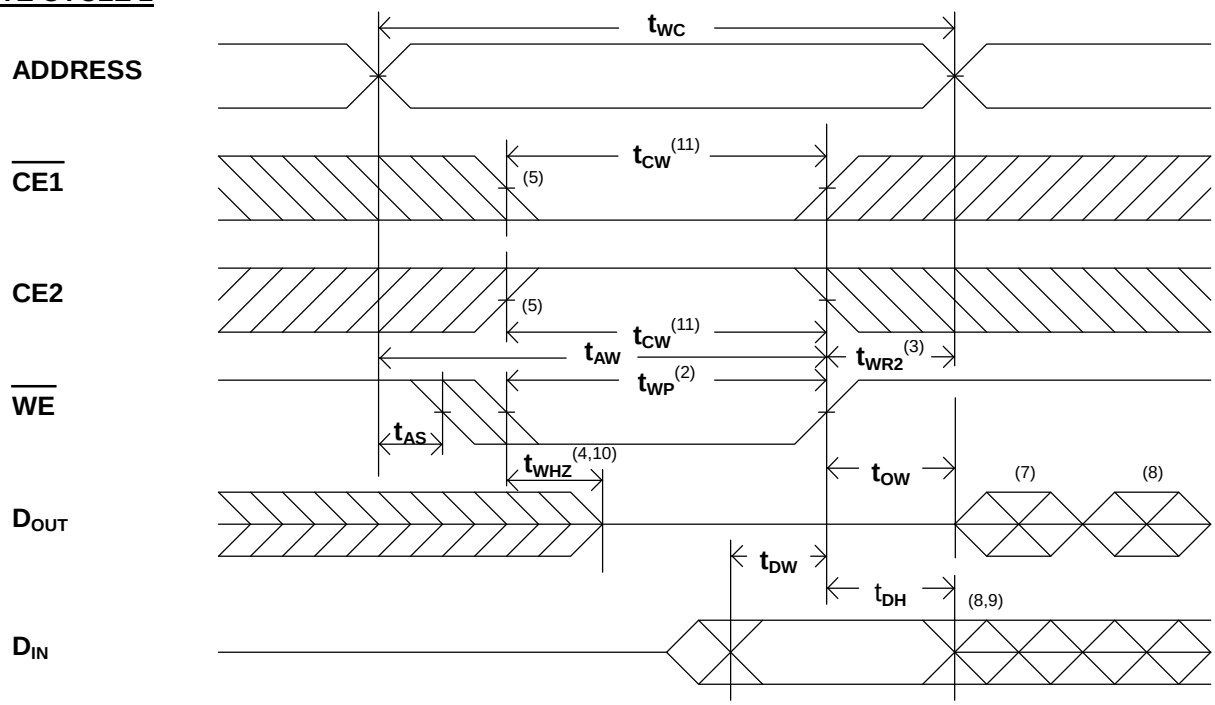
| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | CYCLE TIME : 55ns ($V_{CC}$ = 3.0~5.5V) | | | CYCLE TIME : 70ns ($V_{CC}$ = 2.7~5.5V) | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| $t_{AVAX}$ | $t_{WC}$ | Write Cycle Time | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{E1LWH}$ | $t_{CW}$ | Chip Select to End of Write | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Set up Time | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{AVWH}$ | $t_{AW}$ | Address Valid to End of Write | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | 30 | -- | -- | 35 | -- | -- | ns |
| $t_{WHAX}$ | $t_{WR1}$ | Write Recovery Time ($\overline{CE1}$, $\overline{WE}$) | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{E2LAX}$ | $t_{WR2}$ | Write Recovery Time (CE2) | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{WLQZ}$ | $t_{WHZ}$ | Write to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| $t_{DVWH}$ | $t_{DW}$ | Data to Write Time Overlap | 25 | -- | -- | 30 | -- | -- | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold from Write Time | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{GHQZ}$ | $t_{OHZ}$ | Output Disable to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| $t_{WHQX}$ | $t_{OW}$ | End of Write to Output Active | 5 | -- | -- | 5 | -- | -- | ns |

## n SWITCHING WAVEFORMS (WRITE CYCLE)

### WRITE CYCLE 1 (1)



## WRITE CYCLE 2 (1,6)




NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. $t_{WR}$ is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $D_{OUT}$ is the same phase of write data of this write cycle.
8. $D_{OUT}$ is the read data of next address.
9. If $\overline{CE1}$ is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state with $C_L$ = 5pF.
    The parameter is guaranteed but not 100% tested.
11. $t_{CW}$ is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

## n ORDERING INFORMATION

**BS62LV1027 X X Z Y Y**

**SPEED**
55: 55ns
70: 70ns

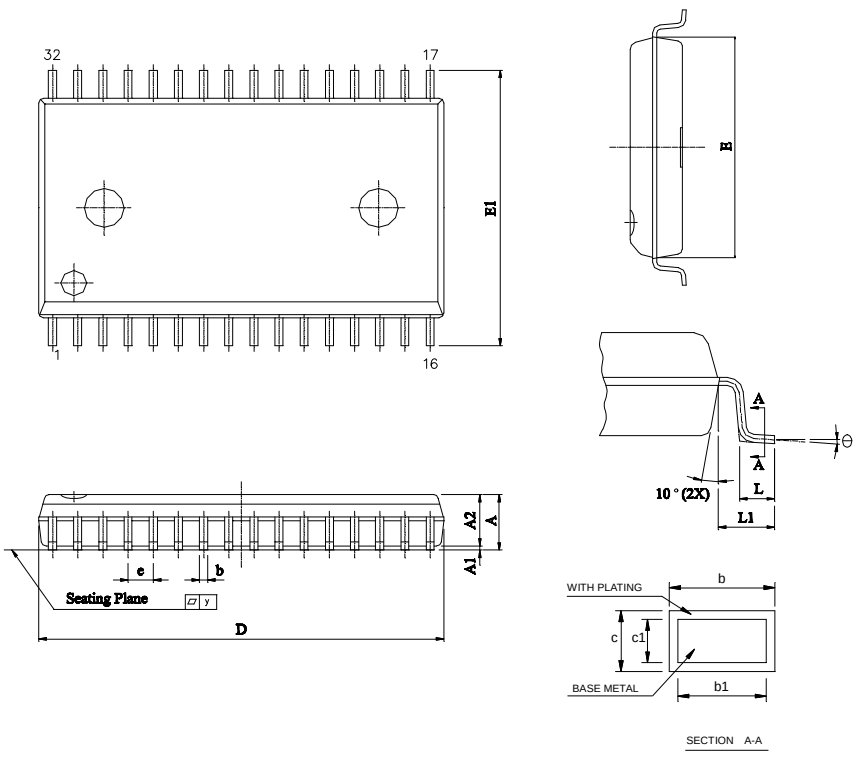
**PKG MATERIAL**
-: Normal
G: Green, RoHS Compliant
P: Pb free, RoHS Compliant

**GRADE**
C: +0°C ~ +70°C
I: -40°C ~ +85°C

**PACKAGE**
D: DICE
H: BGA-36-0608
P: PDIP
S: SOP
T: TSOP (8mm x 20mm)
ST: Small TSOP (8mm x 13.4mm)

Note:
BSI (Brilliance Semiconductor Inc.) assumes no responsibility for the application or use of any product or circuit described herein. BSI does not authorize its products for use as critical components in any application in which the failure of the BSI product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

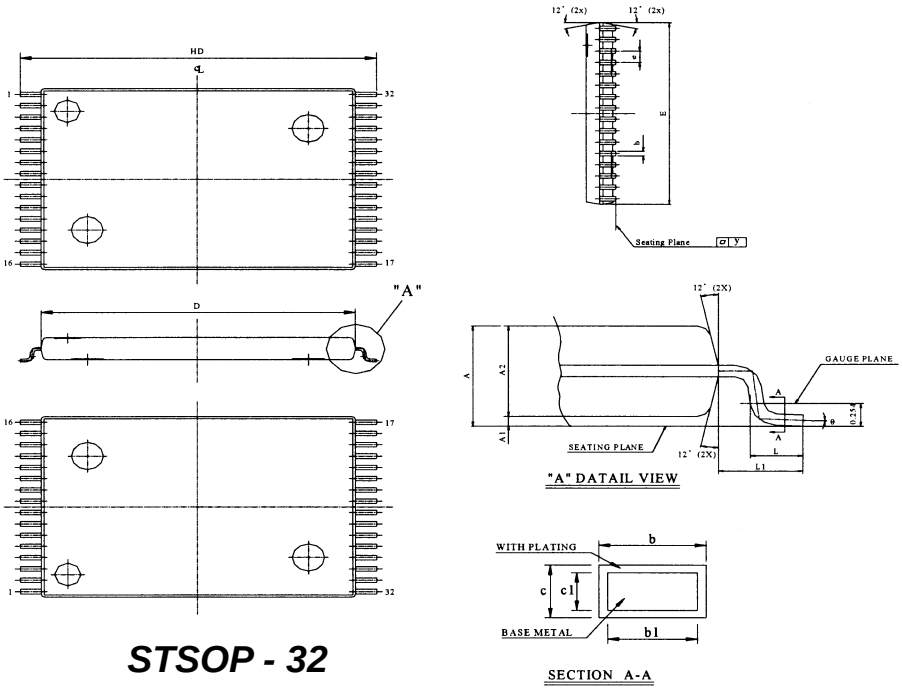
## n PACKAGE DIMENSIONS




| UNIT / SYMBOL | INCH | MM |
|---|---|---|
| A | 0.111±0.007 | 2.821±0.176 |
| A1 | 0.009±0.005 | 0.229±0.127 |
| A2 | 0.1055±0.0055 | 2.680±0.140 |
| b | 0.014 ~ 0.020 | 0.35 ~ 0.50 |
| b1 | 0.014 ~ 0.018 | 0.35 ~ 0.46 |
| c | 0.006 ~ 0.012 | 0.15 ~ 0.32 |
| c1 | 0.006 ~ 0.011 | 0.15 ~ 0.28 |
| D | 0.805±0.005 | 20.447±0.127 |
| E | 0.445±0.005 | 11.303±0.127 |
| E1 | 0.555±0.012 | 14.097±0.305 |
| e | 0.050±0.006 | 1.270±0.152 |
| L | 0.033±0.010 | 0.834±0.25 |
| L1 | 0.055±0.008 | 1.397±0.203 |
| y | 0.004 Max. | 0.1 Max. |
| θ | 0° ~ 10° | 0° ~ 10° |

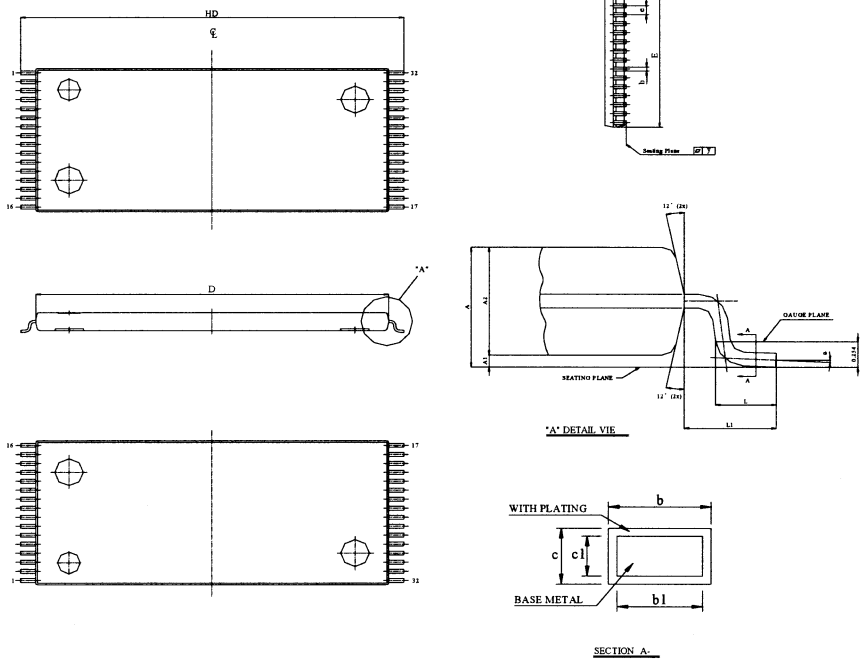
*SOP -32*

## n PACKAGE DIMENSIONS (continued)




| UNIT / SYMBOL | INCH | MM |
|---|---|---|
| A | 0.0433± 0.004 | 1.10± 0.10 |
| A1 | 0.004± 0.002 | 0.10± 0.05 |
| A2 | 0.039± 0.002 | 1.00± 0.05 |
| b | 0.009± 0.002 | 0.22± 0.05 |
| b1 | 0.008± 0.001 | 0.20± 0.03 |
| c | 0.004 ~ 0.008 | 0.10 ~ 0.21 |
| c1 | 0.004 ~ 0.006 | 0.10 ~ 0.16 |
| D | 0.465± 0.004 | 11.80± 0.10 |
| E | 0.315± 0.004 | 8.00± 0.10 |
| e | 0.020± 0.004 | 0.50± 0.10 |
| HD | 0.528± 0.008 | 13.40± 0.20 |
| L | 0.0197 $^{+0.008}_{-0.004}$ | 0.50 $^{+0.2}_{-0.1}$ |
| L1 | 0.0315± 0.004 | 0.80± 0.10 |
| y | 0.004 Max. | 0.1 Max. |
| θ | 0° ~ 8° | 0° ~ 8° |

***STSOP - 32***

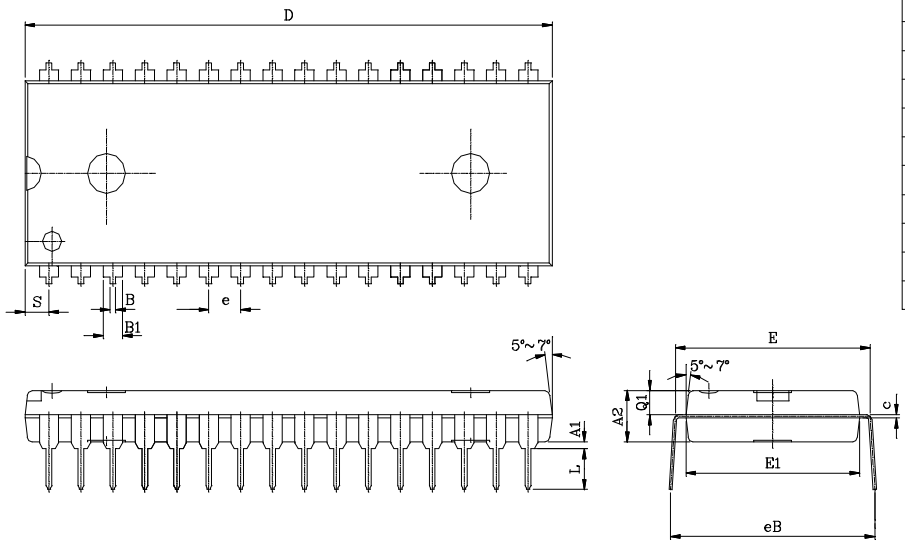



| UNIT / SYMBOL | INCH | MM |
|---|---|---|
| A | 0.0433± 0.004 | 1.10± 0.10 |
| A1 | 0.004± 0.002 | 0.10± 0.05 |
| A2 | 0.039± 0.002 | 1.00± 0.05 |
| b | 0.009± 0.002 | 0.22± 0.05 |
| b1 | 0.008± 0.001 | 0.20± 0.03 |
| c | 0.004 ~ 0.008 | 0.10 ~ 0.21 |
| c1 | 0.004 ~ 0.006 | 0.10 ~ 0.16 |
| D | 0.724± 0.004 | 18.40± 0.10 |
| E | 0.315± 0.004 | 8.00± 0.10 |
| e | 0.020± 0.004 | 0.50± 0.10 |
| HD | 0.787± 0.008 | 20.00± 0.20 |
| L | 0.0197 $^{+0.008}_{-0.004}$ | 0.50 $^{+0.2}_{-0.1}$ |
| L1 | 0.0315± 0.004 | 0.80± 0.10 |
| y | 0.004 Max. | 0.1 Max. |
| θ | 0° ~ 8° | 0° ~ 8° |

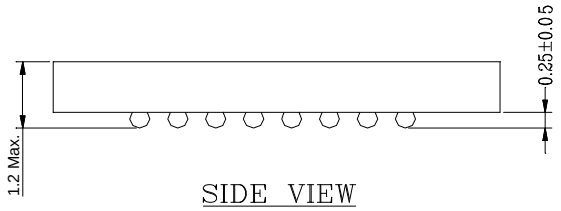
***TSOP - 32***

## PACKAGE DIMENSIONS (continued)

| UNIT / SYMBOL | INCH(BASE) | MM(REF) |
|---|---|---|
| A1 | 0.010(MIN) | 0.254(MIN) |
| A2 | 0.154±0.005 | 3.912±0.127 |
| B | 0.018±0.005 | 0.457±0.127 |
| B1 | 0.050±0.005 | 1.270±0.127 |
| c | 0.010±0.004 | 0.254±0.102 |
| D | 1.650±0.005 | 41.910±0.127 |
| E | 0.600±0.010 | 15.240±0.254 |
| E1 | 0.544±0.004 | 13.818±0.102 |
| e | 0.100(TYP) | 2.540(TYP) |
| eB | 0.650±0.020 | 16.510±0.508 |
| L | 0.130±0.010 | 3.302±0.254 |
| S | 0.075±0.010 | 1.905±0.254 |
| Q1 | 0.070±0.005 | 1.778±0.127 |




*PDIP - 32*

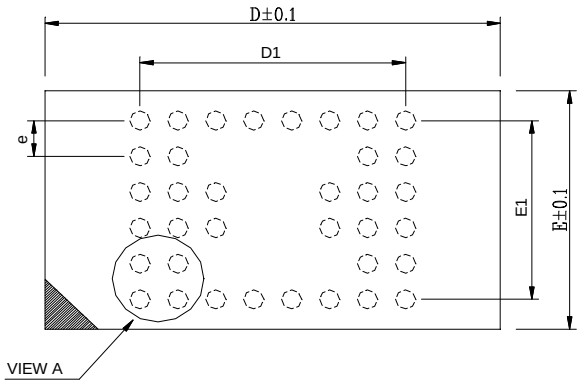



SIDE VIEW

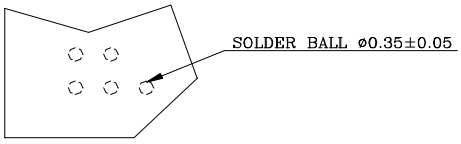
NOTES

1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

| BALL PITCH e = 0.75 | | | | |
|---|---|---|---|---|
| D | E | N | D1 | E1 |
| 8.0 | 6.0 | 48 | 5.25 | 3.75 |




TOP VIEW




VIEW A

*36 mini-BGA (6 x 8mm)*

## n Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 2.2 | Add Icc1 characteristic parameter<br>Improve Iccsb1 spec.<br>I-grade from 20uA to 5.0uA at 5.0V<br>2.5uA to 1.5uA at 3.0V<br>C-grade from 8.0uA to 3.0uA at 5.0V<br>1.3uA to 1.0uA at 3.0V | Jan. 13, 2006 | |
| 2.3 | Change I-grade operation temperature range<br>- from –25°C to –40°C | May. 25, 2006 | |