Rockwell

RC9624AT Data/Fax Modem Design

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INTRODUCTION

This application note describes an RC9624AT Data/Facsimile modem design based on the Rockwell RC224AT and the R96MFX (or R96EFX) modem devices. The RC224AT is a 2400 bps modem with "AT" commands. The R96MFX is a 9600 bps single device MONOFAX™ facsimile (fax) modem.

CONFIGURATIONS CONSIDERED

Four configurations are considered in this application note (Figure 1). The relative merits of each configuration are presented.

Configuration 1 (Figure 1a) requires two communication ports on the host computer. Because the T.4, T.30, and facsimile AT style commands must be implemented in the host, a high degree of compatibility is required of the PC "clones". The advantage of this configuration is that it is the simplest, least power consuming, and least expensive version, and, since both modems can be on at the same time, the host can easily distinguish between incoming facsimile and data calls.

In configuration 2 (Figure 1b), adding a microcontroller to the facsimile portion of the design increases expense and power consumption, but gains the advantage of performing T.4 and T.30 functions off line from the host. Other aspects of the design remain the same as in configuration 1.

Configuration 3 (Figure 1c) is a variation of configuration 2. Only one communication channel is required by this configuration, but more firmware effort is required to ensure compatibility with conventional data communication packages.

Configuration 4 (Figure 1d) has the flexibility of configurations 2 and 3 without adding the cost of a microcontroller. The 2-device version of the RC224AT is used because of its external expansion bus. This bus allows the controller portion of the RC224AT to be the local facsimile modem controller. The bus also allows use of external memory to provide custom AT style commands for facsimile modem functions and to add firmware for T.4 and T.30 algorithms. Since the RC224AT controller is programmed for AT style commands and emulates a 16C450 UART, the data interface is compatible with most communications packages. Configuration 4 is the scheme chosen for this application note, and the resulting design is called the RC9624AT.

REFERENCE INFORMATION

Detailed information on the R96MFX and the RC224AT is provided in the following documents:

R96MFX Data Sheet (Order No. MD47)

R96EFX Data Sheet (Order No. MD49)

9600 bps MONOFAX Modem Programmer's Guide (Order No. 820)

RC224AT Data Sheet (Order No. MD54)

RC224AT Designer's Guide (Order No. 845)

Information provided in this application note concerns the operation of these products in a specific application. For general modem operation and performance information, refer to the specific modem documents.

The controller chip of the two-chip RC224AT is a Rockwell C19 microcomputer. For additional information on the electrical characteristics, timing, and instruction set of this microcomputer refer to the *C19 Microcomputer Technical Reference Manual* (Order No. 400).

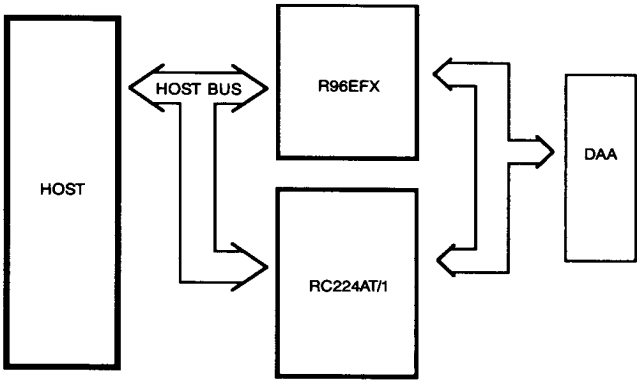
MODEM OPERATION

The RC9624AT incorporates a V.22 bis data modem and a group 2 or group 3 facsimile modem designed to operate on an IBM PC compatible plug-in circuit card. The design contains telephone line Data Access Arrangement (DAA) and loudspeaker circuits that are shared by the two modems.

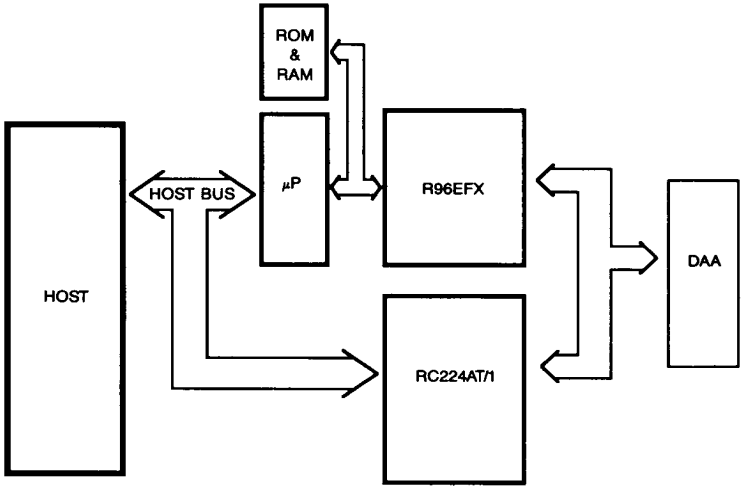
A single host interface is provided by using the C19 data modem controller as a controller for the facsimile modem as well. This controller interprets various AT style commands used with facsimile operation. A transparent mode is also available in which the controller passes data between the host and the facsimile modem. The transparent mode is used by host computers that provide T.4 and T.30 algorithms in the host software. An alternative method of operation is to code the T.4 and T.30 algorithms in the external memory of the C19.

Power consumption is minimized for lap top applications by switching off clock signals and operating voltages when not needed.

A test connector makes various modem signals available to an external circuit for generating diagnostic eye patterns. This connector ensures that the eye pattern circuit draws power only when needed for trouble shooting.

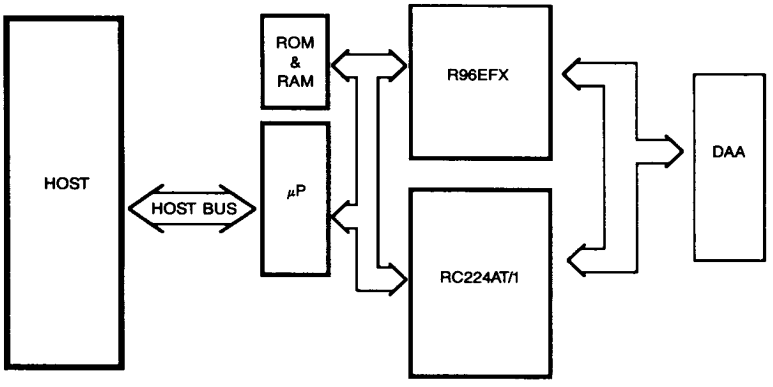


a. RC224AT/1 and Host - R96EFX

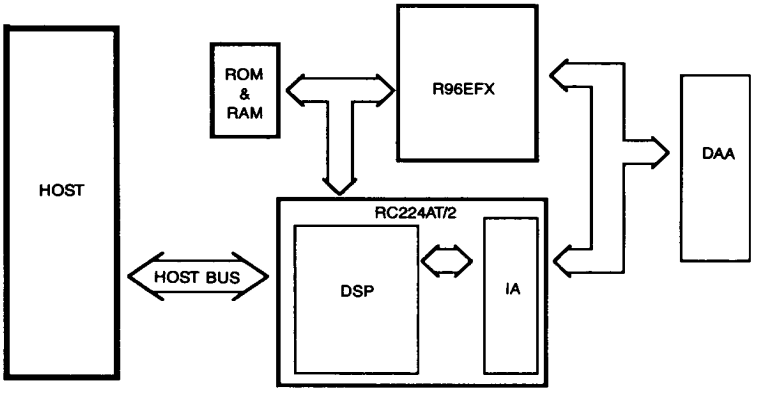


b. RC224AT/1 and Microprocessor - R96EFX

Figure 1. RC9624AT Configurations



c. RC224AT/1 and Microprocessor - R96EFX



d. RC224AT/2 and R96EFX

Figure 1. RC9624AT Design Configurations (Cont'd)

HARDWARE DESIGN

The following description refers to the RC9624AT schematic diagram shown in Figure 2. Sheet 1 of the schematic illustrates the two modem device sets and the necessary support hardware for their interconnection. Sheet 2 shows the interface to the host computer bus and the connector for the external eye pattern generator. Sheet 3 is a schematic of the DAA, which appears on sheet 1 as a single box labeled DAA. Sheet 4 contains schematics for the serial and parallel eye pattern generators that interface to the test connector shown on sheet 2.

Capacitors and inductors shown on sheet 2 of the schematic provide decoupling circuits for the PC power source. This power is also connected to the test connector for driving the external eye pattern circuits.

The remaining circuitry on sheet 2 decodes the host computer address bus to map the RC9624AT into the host I/O space. The addresses normally used by serial ports COM1 or COM2 are used in this design for the modem interface. Jumpers select either COM1 (addresses 3F8H to 3FFH and interrupt IRQ4) or COM2 (addresses 2F8H to 2FFH and interrupt IRQ3).

RC224AT DATA MODEM WITH C19 CONTROLLER

The two large blocks on the bottom of sheet 1 represent the two devices of the RC224AT. The block labeled DSP is the Rockwell C19 controller. The block labeled IA is the integrated analog device. Refer to the RC224AT designer's guide for a detailed description of the device interconnect signals.

Host Bus

The C19 host bus connections are labeled with a B, indicating that the source of these signals is also identified with a letter B. This source is located on sheet 2 at the output of the PC bus decode logic.

A non-volatile memory (HY93C46) is interfaced to the controller by a 4-pin serial port. This memory stores initial modem conditions and frequently called phone numbers. Four signals labeled $\overline{\text{RING}}$, SPKREN, SPKRH, and SPKRL provide ring signal detection and speaker control for the DAA circuit.

Expansion Bus

The remaining C19 signals form an expansion bus that accesses the external memory (27C64) via the address latch (74HC373). The external memory contains specialized code for detecting and executing the AT style facsimile commands and for operating the C19 in transparent mode. The C19 also exchanges data with the facsimile modem via the external bus.

R96MFX FACSIMILE MODEM

The block labeled R96MFX represents the facsimile modem. This single package modem is an R96MFX or an R96EFX, since the pin functions are identical. The two jumpers on pins 32 and 33 select the cable equalizer option as described in the R96MFX data sheet.

SUPPORTING CIRCUITS

Analog Interface

Three operational amplifiers provide buffering and filtering for the analog transmit and receive signals. Because the filter requirements are different for the two transmitter circuits, the signals are filtered separately and then resistively summed at the DAA hybrid input.

Clock Oscillator

A single oscillator supplies clock signals for the two modems. This 24 MHz oscillator is very accurate and stable in order to meet the requirements of group 2 facsimile. A less expensive oscillator may be used if group 2 is not required, however, the oscillator selected must meet the two modem requirements of less than 0.01% error over temperature, voltage, and aging for a period of six years.

The ideal clock frequency for the facsimile modem is 24.00014 MHz. The ideal clock frequency for the data modem is 12.000393 MHz. By choosing the ideal facsimile frequency for the oscillator, all the initial error is placed on the data modem. Dividing the oscillator frequency by two (using a D flip-flop) yields 12.00007 MHz. This frequency contains an error of 27 ppm relative to the ideal data modem clock. The oscillator illustrated in the schematic of the RC9624AT may have an initial error of 2 ppm, plus 5 ppm change over the modem temperature range, 1 ppm change over the modem operating voltage, and 6 ppm drift over six years, for a total of 41 ppm, which is well within the 100 ppm requirement.

FAX Modem Enable

FAXEN1. When the facsimile modem is not in operation, the facsimile clock is turned off by fax enable signal, FAXEN1. Turning off the clock on a CMOS device reduces its power consumption. Clock control is accomplished by a 2-to-1 multiplexer (74HCT257). The switched clock, F24CLK, is maintained at +5V when in data modem operation. The F24CLK follows 24CLK when in facsimile modem operation.

In order for the C19 to reduce IA power consumption in sleep mode the signal IAEN drives a digital switch to turn off the IA bias voltage. In a similar fashion, signal $\overline{\text{FAXEN1}}$ drives a FET to turn off -5VA to the R96MFX when it is not in use.

FAXEN. The fax enable signal, FAXEN, is generated by the C19 controller in response to a special AT style command that selects facsimile modem operation. The second D flip-flop on sheet 1 of the schematic synchronizes

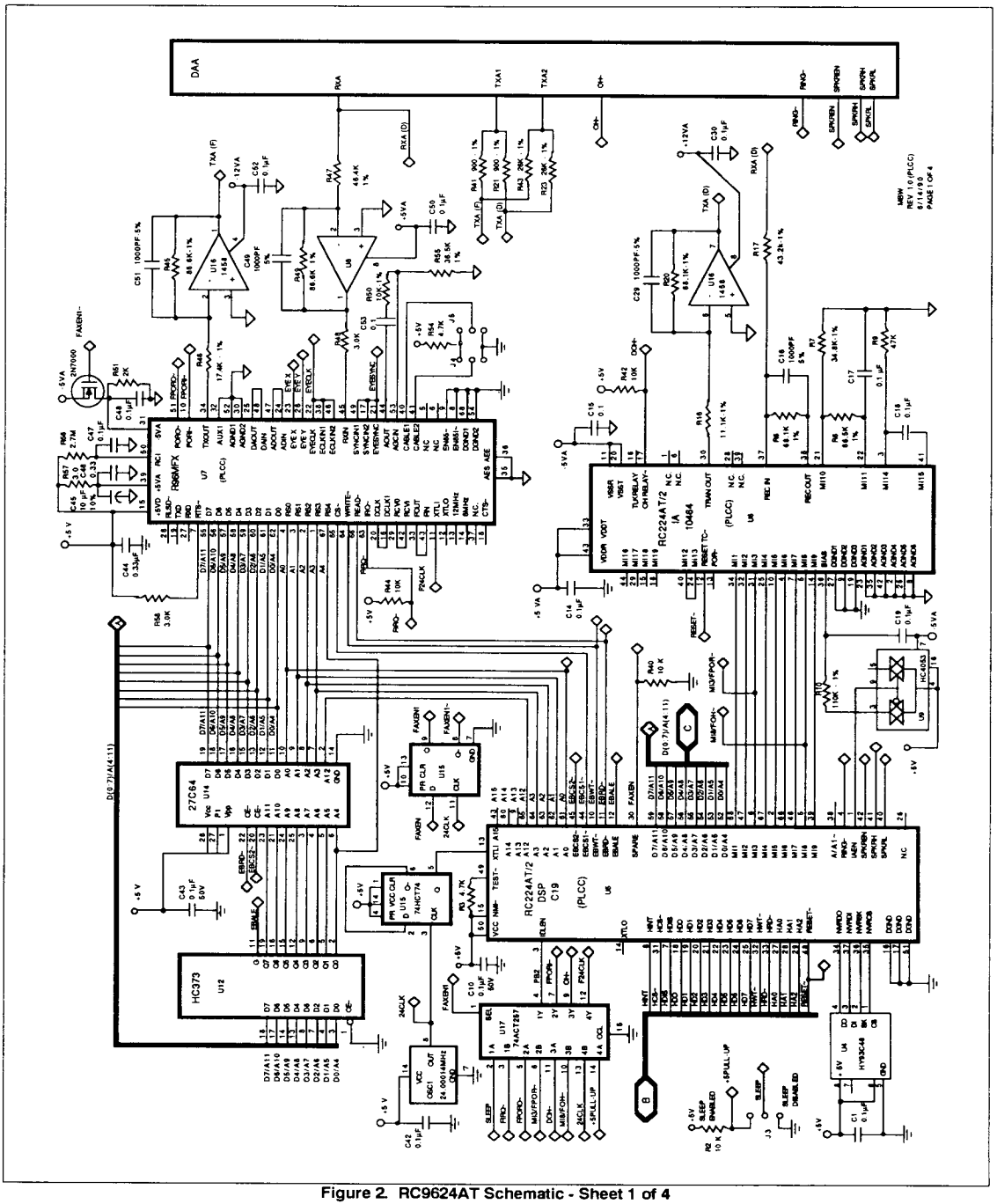


Figure 2. RC9624AT Schematic - Sheet 1 of 4

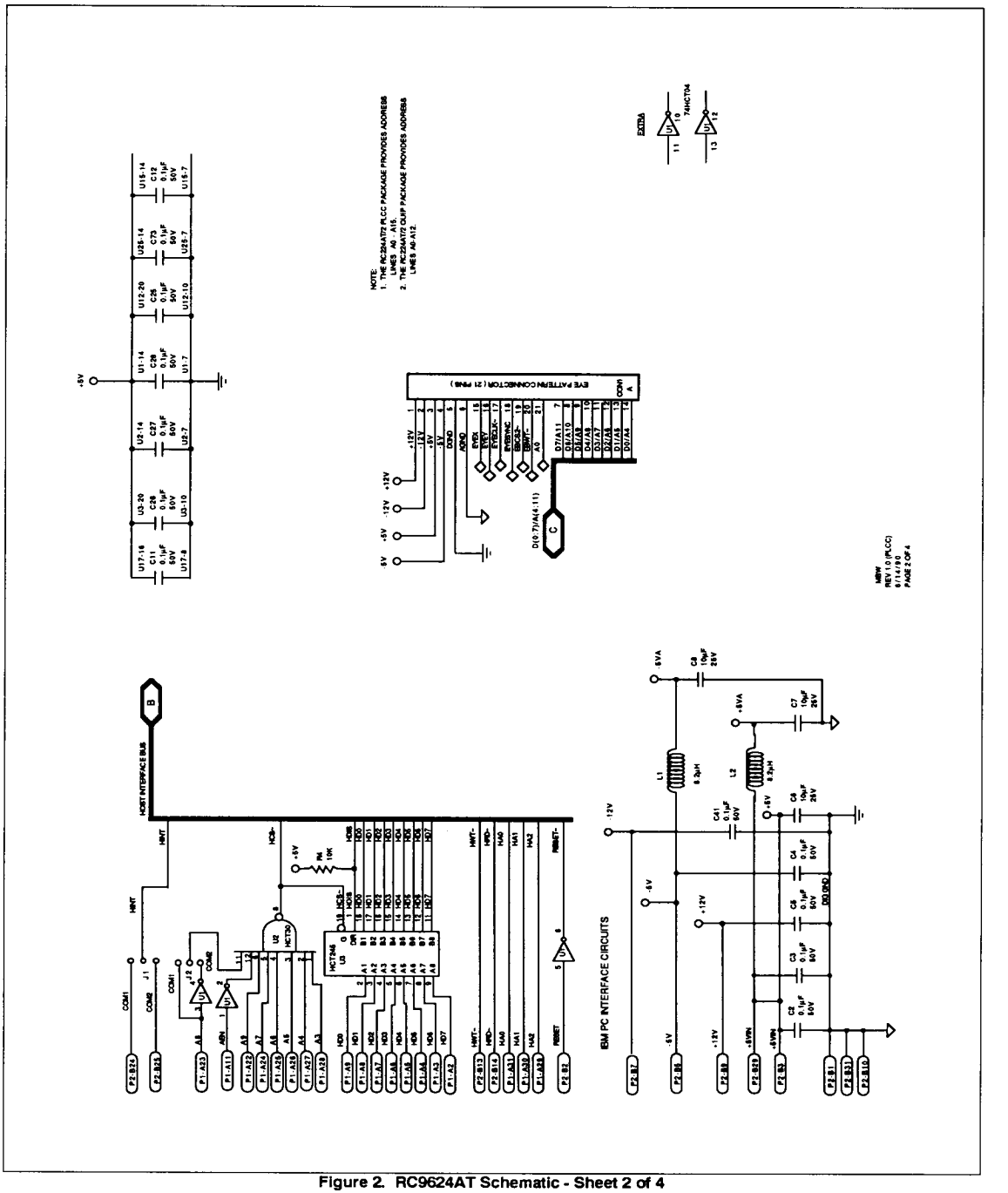


Figure 2. RC9624AT Schematic - Sheet 2 of 4

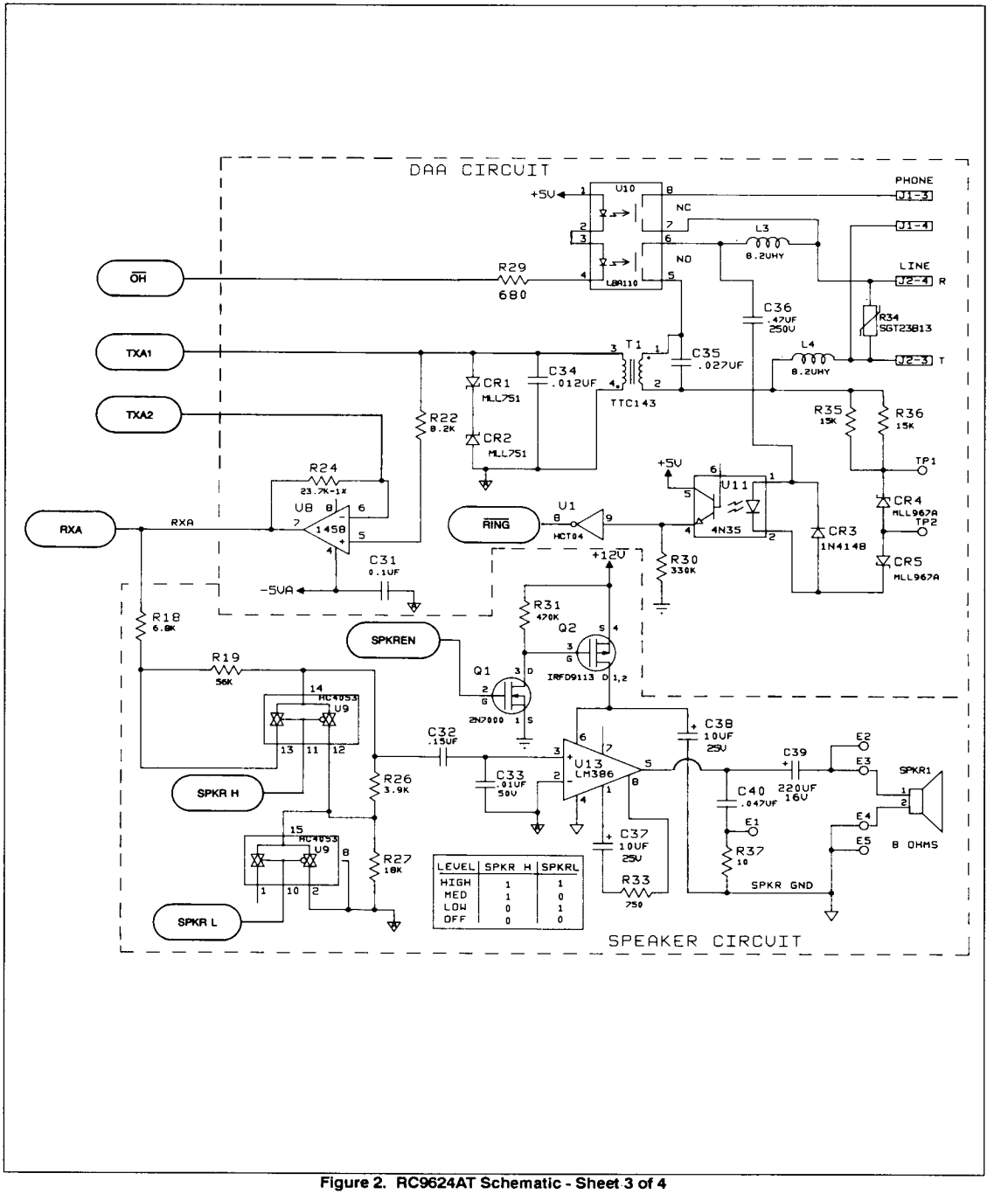


Figure 2. RC9624AT Schematic - Sheet 3 of 4

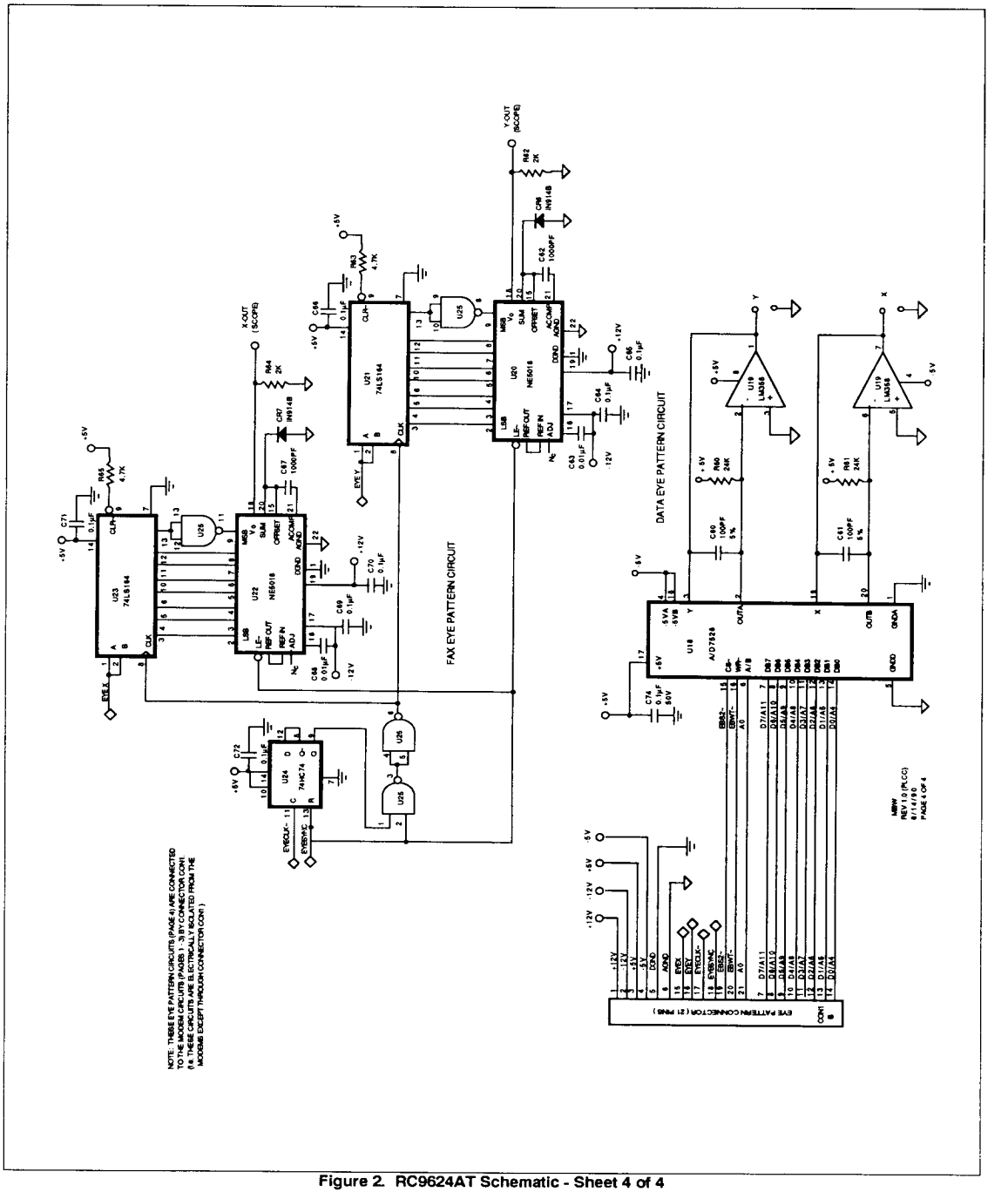


Figure 2. RC9624AT Schematic - Sheet 4 of 4

FAXEN with the rising edge of the 24 MHz clock. By ensuring that the FAXEN1 signal changes state on the rising edge of 24CLK the facsimile modem is prevented from experiencing narrow clock "slivers" when switching from data operation to facsimile operation.

Three additional functions are switched by the fax enable signal controlling the 2-to-1 multiplexer.

DAA Off-Hook Control. The first function is control of the DAA off-hook state. When in data modem operation the RC224AT IA controls the telephone line off-hook condition. When in facsimile modem operation a general purpose I/O signal, MI8, controls off-hook.

Fax Modem Power-On-Reset. The second function is generation of power-on-reset to the facsimile modem. During power turn on, the signal $\overline{\text{FPORO}}$ drives the R96MFX input signal $\overline{\text{FPORI}}$. These pins are normally hard-wired together, so connecting them via the multiplexer provides a conventional method of resetting the facsimile modem at power turn-on time. When the facsimile modem has been selected for communication, the general purpose output MI3 controls the facsimile modem reset. By using MI3 the C19 resets the facsimile modem as necessary when changing between data and facsimile operation.

Data Modem Sleep Mode. The third function is selecting a source for the C19 PB2 input. When in data modem operation, input PB2 allows the C19 to test the enabled or not enabled state for data modem sleep mode. This option determines whether or not the data modem enters a low power usage state when it senses inactivity for a preset period of time. In facsimile operation, input PB2 becomes an interrupt input from the R96MFX IRQ line.

DAA Circuit

Sheet 3 of the RC9624AT schematic illustrates the DAA and loudspeaker circuit. Two connectors, J1 and J2, are modular telephone jacks, type RJ11. A telephone handset may be connected to the modem via connector J1 pins 3 and 4. The DAA connects to the local telephone line via connector J2 pins 3 and 4. The T and R designations refer to the TIP and RING wires of the telephone line.

The telephone handset may be used for manual call establishment and voice communication. An optically coupled form A and form B switch combination connects either the telephone handset or the modem to the telephone line. When signal $\overline{\text{OH}}$ is low, the switch connects the modem to the telephone line. When $\overline{\text{OH}}$ is high, the handset is connected to the telephone line.

An optically coupled npn transistor is ac coupled across tip and ring. The transistor turns on when a ring signal is present on the telephone line. The signal $\overline{\text{RING}}$ is monitored by the C19 to detect incoming calls.

When the C19 places the DAA off-hook, an audio transformer type TTC143 ac couples the modem to the telephone line. An operational amplifier type 1458 forms a solid state hybrid circuit in combination with the four resistors illustrated on sheet 1 of the schematic. When a received signal from the audio transformer is present at point TXA1 and not present at point TXA2, the signal is passed to the modem receiver at point RXA. If, however, the signal present at TXA1 is from the modem transmitter, then an attenuated version of the same signal is present at point TXA2. This second signal tends to cancel the signal from TXA1 reducing the component of the transmitter signal coupled to the receiver.

Loudspeaker Circuit

The amplifier used in the speaker circuit is a type LM386. This amplifier has variable gain controlled by the C19. Signals SPKRH and SPKRL operate digital switches that select various resistor values in a resistive divider. Audio attenuation changes in 6 dB steps for the low, medium, and high settings. The fourth setting is off. A pair of FET switches removes power from the amplifier when the speaker circuit is not required. This feature reduces power consumption in sleep mode.

Eye Pattern Generation Circuit

Circuitry on sheet 4 of the schematic is not actually part of the modem. These circuits generate eye patterns on an oscilloscope when trouble shooting modem problems. For a description of eye pattern analysis refer to the application note, *Quality Of Received Data For Signal Processor-based Modems* (Order No. 671).

The R96MFX provides a serial port for generating eye patterns. This port is connected to a pair of shift registers (74LS164) and a D-type flip-flop (74HC74) for converting data from serial to parallel form. The parallel data bytes are then transferred to a pair of digital-to-analog converters (NE5018) for output to the analog X and Y inputs of an oscilloscope.

No serial eye pattern is available on the RC224AT so the data must be read by the C19 controller and then sent to an addressable digital-to-analog converter (A/D7528). This digital-to-analog converter requires two external amplifiers (LM358) to convert the signals for display.

FIRMWARE

Standard firmware is used in the two modems comprising the RC9624AT. Custom firmware, created to facilitate the integration of these two modems into a single product, resides in the external EPROM (27C64). This custom firmware decodes the special AT style commands necessary for facsimile operation, and provides the C19 with a transparent mode for exchanging data between the R96MFX and the host controller.

AT STYLE COMMANDS

The AT style commands implemented for changing between data modem and facsimile modem operation and the AT style commands implemented for facsimile opera-

tion are described in the following paragraphs. Some of these commands are suggested by a document entitled, *Working Draft Standard For PN-2188: Asynchronous Facsimile DCE Control Standard*. This document is being generated by the Telecommunications Industry Association Subcommittee TR30.4, DTE-DCE Protocols.

Modem Class/Configuration Selection

Two commands function when either the data modem or the facsimile modem is selected. These commands are: AT+FCLASS=n and AT+FCLASS?.

AT+FCLASS=n. The AT+FCLASS=n command sets the RC9624AT to one of several classes that are defined in the above referenced document and described briefly here.

Class 0 is the only data modem class defined. Class 1 operation implies that the T.4 and T.30 facsimile protocols are performed in the host computer software. Class 2 operation means that only the T.4 protocol is performed by the host, since the modem performs the T.30 protocol. For class 3 operation the host does not perform either protocol, since the modem performs data compression and decompression plus handshaking for modem connection. The RC9624AT external EPROM firmware is written for class 0 and class 1 operation only. Attempts to select other values of n result in an error message.

AT+FCLASS=?. The AT+FCLASS=? command returns a number identifying the supported class types. Though class 1 is not fully supported, the RC9624AT will return "0, 1" when AT+FCLASS=? command is executed. The "0" refers to class 0 and the "1" refers to class 1.

AT+FCLASS?. The AT+FCLASS? command returns the previously selected value of n. When n = 0, the RC9624AT is configured as a data modem. When n = 1, the RC9624AT is configured as a facsimile modem.

Fax Modem Commands

Five commands function only in facsimile modem operation. These commands are: AT+C, AT+S, AT+T, AT+Z, and ATZ.

AT+C. The AT+C command configures the facsimile modem for 9600 bps and parallel data mode.

AT+S. The AT+S command places the facsimile modem in sleep mode.

AT+T. The AT+T command places the facsimile modem in transparent mode.

AT+Z and ATZ. The AT+Z and ATZ commands cause a power-on-reset to the facsimile modem.

Extended Data Modem Commands

Finally, six commands that exist already for data modem operation are extended to facsimile modem operation. These commands are: ATEn, ATH, ATO, ATSn=x, ATSn?, and ATVn.

ATEn. The ATEn command enables or disables echo back to the host. For n = 0, echo back is disabled. For n = 1, echo back is enabled.

ATH and ATO. The ATH and ATO commands cause the facsimile modem to go on-hook or off-hook, respectively.

ATSn=x. The ATSn=x command sets register "n" to the value "x".

ATSn?. The ATSn? command causes the stored contents in register "n" to be sent to the DTE.

ATVn. The ATVn command selects numeric or text responses. For n = 0, responses are numeric. For n = 1, responses are text.

TRANSPARENT MODE

The transparent mode allows the C19 controller to pass data between the host processor and the facsimile modem without interpreting the data. Transparent mode causes the UART registers of the C19 to be redefined. See the RC224AT data sheet for a description of the standard C19 UART interface as used for AT style commands and data modem operation. The following description applies to the C19 interface when transparent mode is selected in facsimile modem operation.

UART Functions In Transparent Mode

Register names and numbers shown in Figure 3 are taken from RC224AT usage and may have no relationship to their use in transparent mode. When referring to bits in the interface registers the following convention is used. The register is specified first followed by a colon and then the bit number. For example register seven bit six is designated as 7:6.

As mentioned previously, transparent mode is entered by the facsimile modem decoding an AT+T command in the data stream. Once the C19 is in transparent mode it no longer decodes data being transferred to the facsimile modem. The transparent mode is terminated by the host setting the EXIT bit in register 3 (EXIT bit, 3:5). This bit serves a dual function as described later.

The eight interface registers (registers 0 through 7) are organized into two data ports. One port handles reading or writing data for the communication channel (telephone line), and the other port handles reading or writing R96MFX interface memory data.

Communication Channel

The communication channel is serviced by operating the facsimile modem in parallel data mode with the Interrupt Enable Two bit (IE2) set, as described in the R96MFX data sheet.

When sending data the host first sets the R96MFX Request to Send bit (RTSP). The first byte of data is then written to the C19 Channel Data register (Register 0), causing an interrupt to the C19. The C19 transfers the data to the R96MFX data buffer. The C19 sets the Transmit

Channel Data bit (TCD bit, 5:5) when interrupted by the R96MFX request for more data (IA2). The host polls TCD to determine when the next byte is required, or, by setting the Enable TCD Interrupt bit (ETCDI bit, 1:1), the host is interrupted when TCD sets. The TCD bit resets when the host writes the next byte of data to register 0. This handshaking procedure continues until the host sends all required data, turns off RTSP, and disables interrupts by resetting IE2.

Receiving channel data follows a similar sequence. The host enables the R96MFX to interrupt the C19 by setting IE2. When the R96MFX has a byte of data for the host, it interrupts the C19, and the C19 transfers the data to register 0 and sets the Receive Channel Data bit (RCD bit, 5:0). This bit is polled by the host or causes a host interrupt when the Enable RCD Interrupt bit (ERCDI bit, 5:0) is set. When RCD is set, the channel data is available in register 0. When the host reads register 0, the RCD bit resets. This handshaking procedure continues until the host receives all the data and resets the R96MFX IE2 bit.

Modem Interface Memory

As described in the R96MFX data sheet, the modem interface memory consists of 32 8-bit registers that contain modem status and control information. The interface memory is accessed by the host using a read address or write address, stored in register 4 or register 3 of the C19 interface, and a read/write data byte, stored in register 7. Flowcharts for reading and writing the fax modem interface registers are shown in Figure 4.

Reading Interface Memory. A typical read of the R96MFX interface memory begins with the host writing the interface memory register number to the MCR register (register 4). The register number occupies the five least significant bits of the MCR register. The host writing to register 4 causes an interrupt to the C19 controller and results in the contents of the designated interface memory register being transferred to the C19 SCRATCH register (Register 7). When the C19 writes data to register 7 it also sets the Acknowledge bit (ACK bit, 5:2). The host polls this bit or enables an interrupt by setting the Enable Transparent Status Interrupt bit (ETSI bit, 1:2). When the host reads register 5, the ACK bit resets. The host responds to ACK setting by reading the data from register 7.

Writing Interface Memory. A typical write to the interface memory begins with the host writing data to register 7, the SCRATCH register. Next, the host writes the interface memory register number to the LCR register (register 3). The interface memory register number occupies the five least significant bits of register 3. The three most significant bits of register 3 must remain zeros during a standard interface memory write cycle. Writing to register 3 causes an interrupt to the C19 controller and results in the contents of register 7 being transferred to the designated interface memory register. Once data is written to the R96MFX interface memory, the C19 sets the Acknowledge bit (ACK bit, 5:2). The host polls this bit or enables an interrupt as described previously.

Read Modify Write. Because many operations require setting or resetting a single bit or group of bits in a modem interface memory register, a unique write operation is provided for this purpose. The next to most significant bit in register 3 is designated the Read Modify Write bit (RMW bit, 3:6). When the write address is written with the RMW bit equal to one, the C19 reads the contents of the designated address, sets or resets bits specified by a mask, and writes the resulting data back to the designated address.

First, the mask is stored in register 7 in place of normal write date. Then the write address is written to register 3 with the RMW bit (3:6) set. Setting or resetting bits is determined by the state of the SET bit (3:5). When SET is a one, all bits marked by a one in the data mask are set by the read modify write cycle, while all other bits remain unchanged. When SET is a zero, all bits marked by a one in the data mask are reset by the read modify write cycle, while all other bits remain unchanged. The cycle ends the same as a standard write cycle with the C19 setting the ACK bit.

Register Name	Register No.	Bit No. 7	6	5	4	3	2	1	0
SCRATCH	7	READ/WRITE DATA							
MSR	6	ERROR CODE							
LSR	5	—	—	TCD	EFI	PI	ACK	DDI	RCD
MCR	4	0	0	0	READ ADDRESS				
LCR	3	0	0	Set/Exit	WRITE ADDRESS				
IIR	2	—	—	—	—	—	IID1	IID0	IP
IER	1	—	—	—	—	0	ETSI	ETCDI	ERCDI
TBUF	0	CHANNEL DATA (TRANSMIT)							
RBUF	0	CHANNEL DATA (RECEIVE)							
NOTE: (—) indicates reserved for modem use only.									

Figure 3. UART Register Definitions in Transparent Mode

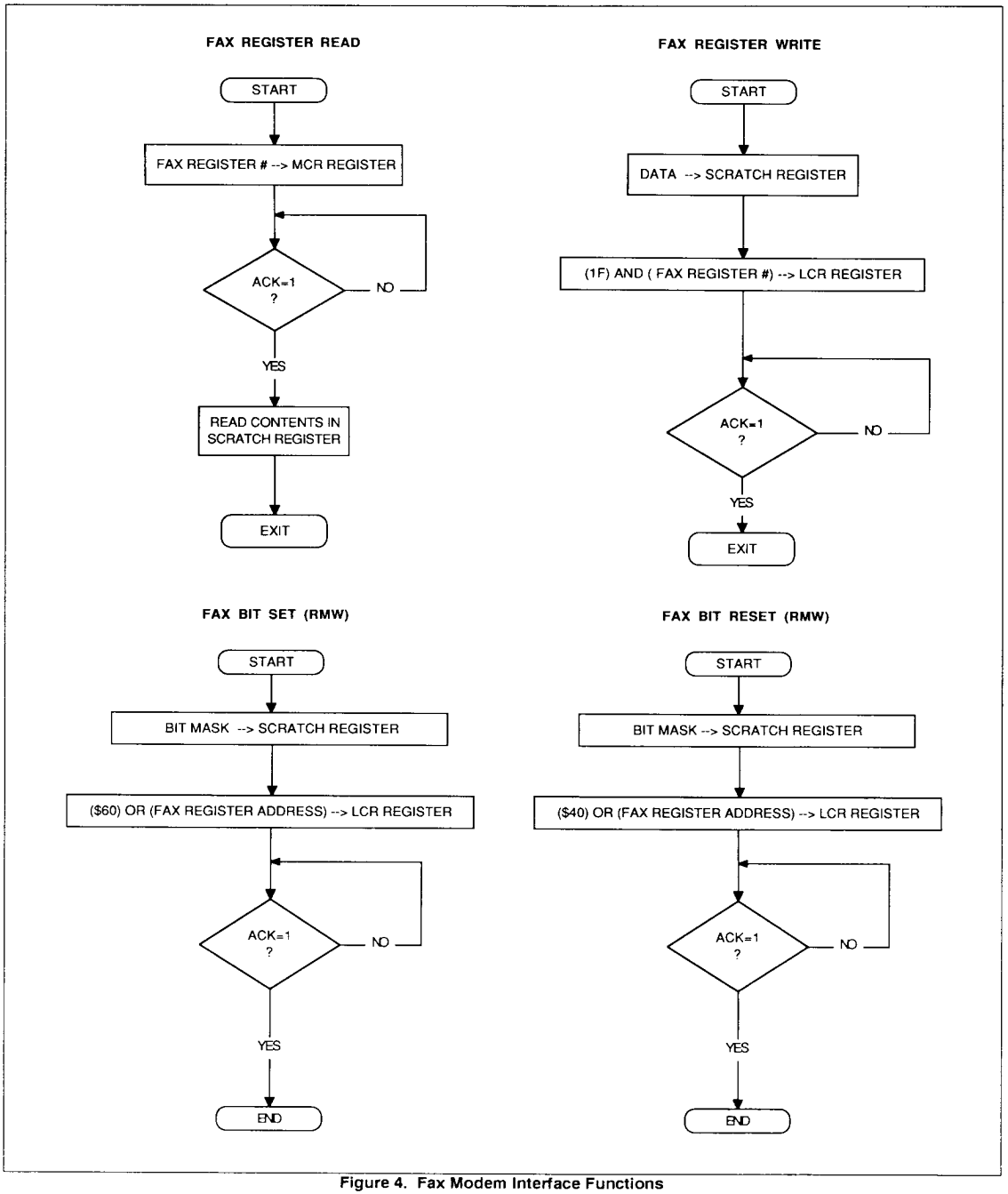


Figure 4. Fax Modem Interface Functions

The 3:5 bit serves two functions. When RMW is a one, 3:5 functions as described for SET. When RMW is a zero, 3:5 functions as the EXIT bit, causing the C19 to leave transparent mode. Note that bit 3:7 is a hardware bit that performs a register remapping function required for data modem operation, but is not used in the facsimile modem configuration. This bit must remain a zero for proper facsimile modem operation.

R96MFX RAM

The R96MFX RAM consists of 256 32-bit words containing operational information useful in performing diagnostics. When reading or writing diagnostic data, the host accesses the RAM indirectly by using the R96MFX interface memory as an intermediary. The desired RAM address is written to a specific interface memory register using the standard interface memory write scheme described previously. A modem diagnostic read or write cycle then transfers two 32-bit data words between modem RAM and four 8-bit modem interface memory registers reserved for this purpose. The host reads or writes the 8-bit interface memory registers one at a time using the standard interface memory read or write scheme.

In order to prevent errors from occurring while reading or writing the two 32-bit diagnostic data words as four 8-bit bytes, the host synchronizes its read/write operation to the modem's diagnostic cycle. The host first reads the least significant byte of the four modem diagnostic registers to clear any pending diagnostic interrupt from the R96MFX to the C19 (see the R96MFX data sheet for an explanation of the diagnostic read/write cycle). The host then starts the modem diagnostic cycle by setting modem bits IE1 and ACC1. The end of the diagnostic cycle is indicated by the setting of C19 Diagnostic Data Indicator bit (DDI bit, 5:1). The DDI bit sets when the R96MFX completes the four-byte transfer to or from modem RAM, and sets the modem BA1 bit. The host now turns off modem bit IE1 to prevent further diagnostic interrupts. The host polls the DDI bit or enables DDI to cause a host interrupt by setting the Enable Transparent Status Interrupt bit (ETSI bit, 1:2).

Error Codes

Various facsimile modem operations generate error codes for specified conditions; for example, a read or write cycle that fails to run to completion before a watchdog timer times out. When these errors occur, error codes are written to the MSR register (register 6) by the C19 controller. Writing to register 6 causes the Error Flag Indicator (EFI bit, 5:4) to set. An interrupt to the host occurs if the host has enabled transparent mode status interrupts by setting the ETSI bit (1:2).

Programmable Interrupts

One source of interrupts, available only on the R96EFX, is programmable. This feature is described in detail in the R96EFX data sheet. By setting certain pointers and masks in the R96EFX interface memory the modem generates an interrupt to the C19 when a programmed condition occurs. When the programmable interrupt occurs, the C19 sets the Programmable Indicator bit (PI bit, 5:3). A host interrupt is generated when PI sets if the host has set bit ETSI, as previously described.

Interrupt Pending Bit

Register 1, the IIR register, contains three interrupt indicator bits in the three least significant positions. Bit 1:0 is the Interrupt Pending bit (IP bit, 1:0). This bit sets when the C19 generates a host interrupt. In a system that shares the IRQ line between multiple devices, IP is polled by the host to determine the interrupting device.

Interrupt Identification Bits

The two Interrupt Identification bits, IID1 and IID0, are binary coded to indicate the highest priority interrupt pending from the C19. Code 0 indicates an interrupt caused by writing to the MSR register. This interrupt is not used in the RC9624AT and is disabled by writing a zero to bit 1:3. Code 1 indicates that the TCD bit is set. Code 2 indicates that the RCD bit is set. Code 3 indicates that one or more of the Transparent Status bits, 5:1 to 5:4, is set. The highest magnitude code is the highest priority.

DESIGN AIDS

The RC9624AT modem design provides an OEM customer with a starting point for developing a product based on the R96MFX and RC224AT combination. The hardware and software described here are examples drawn from a basic product combining these devices. In general, OEM engineers modify both hardware and software to fit their application. Examples of these modifications are: eliminating the built in speaker circuit and substituting the speaker of the host controller, or adding custom AT style facsimile commands. The OEM product also requires a software driver for installation in the host system.

To facilitate these design changes several aids are provided. Descriptions of the C19 expansion bus hardware and software explain capabilities and restrictions important to understanding this interface. The parts list in Table 1 provides examples of components suitable for use. The power requirements for the existing design is listed in Table 2 as a guide to hardware characteristics. Mnemonic definitions for the transparent mode host interface are summarized in Table 3 to assist in both firmware and software development.

A flowchart of the Data Modem AT Command Interpreter is shown in Figure 5. A program listing is included in Appendix A as an example of external EPROM coding for the C19 controller.

For additional assistance, contact a Rockwell Field Applications Engineer at any of the sales offices listed on the back of this document.

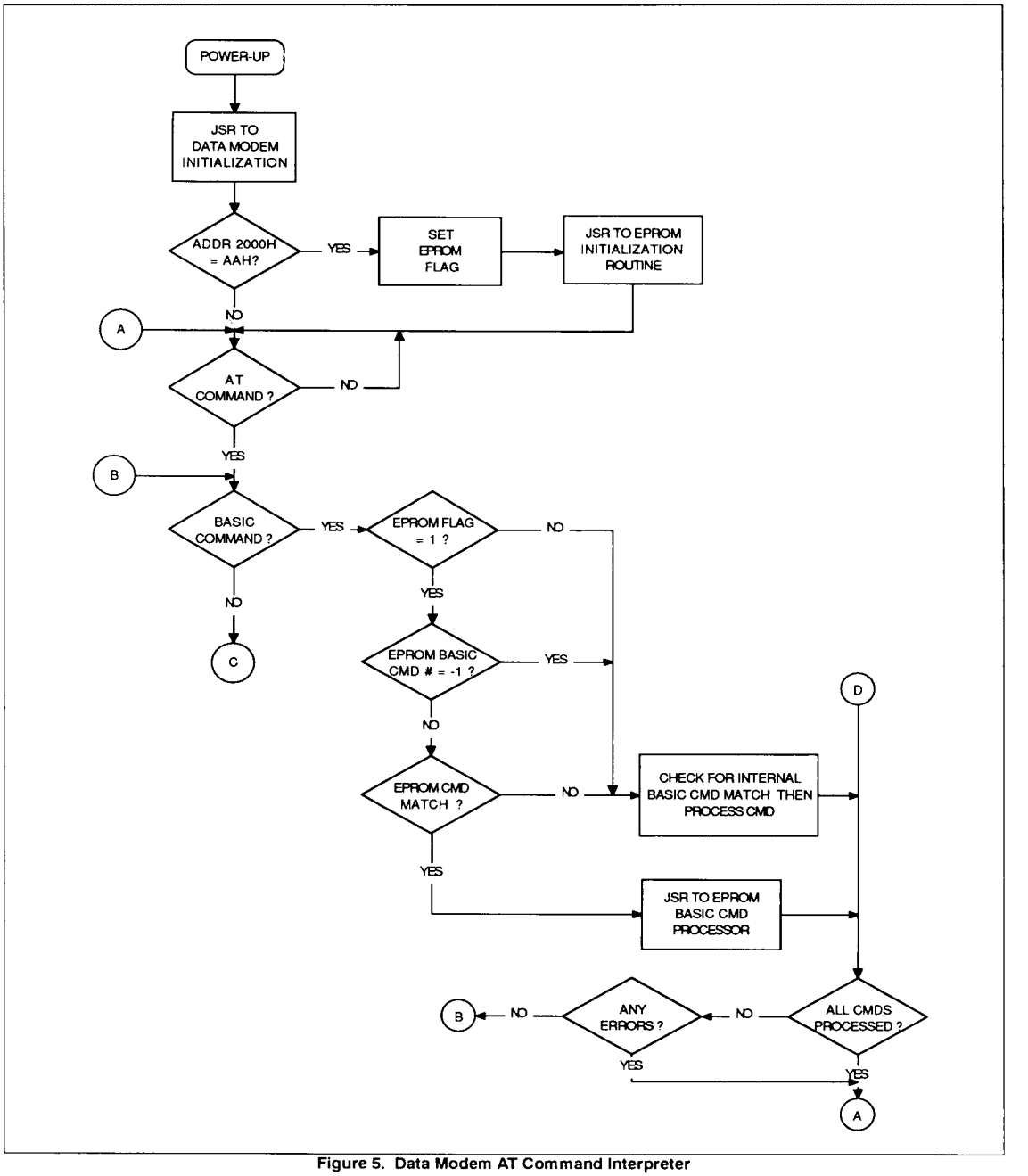


Figure 5. Data Modem AT Command Interpreter

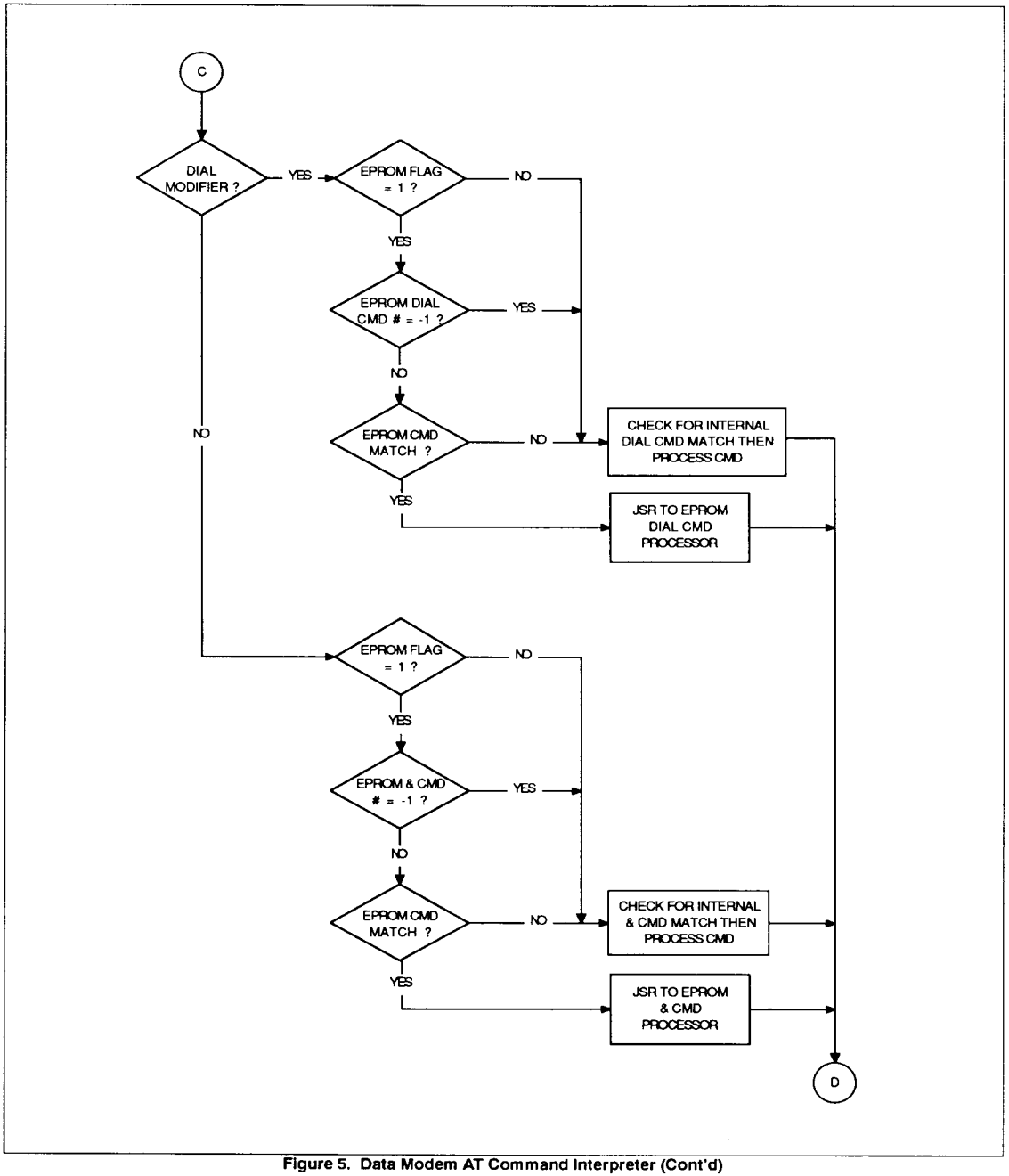


Figure 5. Data Modem AT Command Interpreter (Cont'd)

Table 1. RC9624AT Parts List

Qty. Reqd.	Nomenclature or Description	Part or Identifying Number	Circuit		
			General	DAA/Speaker	Eye Pattern
1	Printed Circuit Board (PCB)	-	-	-	-
1	IC, Inverter	74HCT04	1/2 U1	1/6 U1	-
1	IC, 8-Input NAND Gate	74HCT30	U2	-	-
1	IC, Octal Bus Transceiver	74HCT245	U3	-	-
1	IC, Non-Volatile RAM (NVRAM)	HY93C46	U4	-	-
1	IC, Data Modem DSP	RC224AT/2 DSP	U5	-	-
1	IC, Data Modem IA	RC224AT/2 IA	U6	-	-
1	IC, MONOFAX Modem	R96MFX	U7	-	-
1	IC, Operational Amplifier	1458	1/2 U8	1/2 U8	-
1	IC, Analog Multiplexer	HC4053	1/3 U9	2/3 U9	-
1	IC, Opto Relay	LBA110	-	U10	
1	IC, Opto Relay	4N35	-	U11	-
1	IC, Octal Latch	74HC373	U12	-	-
1	IC, Power Amplifier	LM386	1/2 U13	1/2 U13	-
1	IC, 8Kx8 EPROM	27C64	U14	-	-
1	IC, Dual D Flip-flops	74HCT74	U15	-	-
1	IC, Operational Amplifier	1458	U16	-	-
1	IC, Two-to-One Multiplexer	74ACT257	U17	-	-
1	IC, Analog-to-Digital Converter	A/D7528	-	-	U18
1	IC, Power Amplifier	LM358	-	-	U19
1	IC, Digital-to-Analog Converter	NE5018	-	-	U20, U22
1	IC, Parallel Output Shift Register	74LS164	-	-	U21, U23
1	IC, Dual D Flip-Flops	74HC74	-	-	U24
1	IC, 2 Input NAND Buffer	74HCT37	-	-	U25
1	Transformer	TTC143	-	T1	-
2	NFET Transistor	2N7000	Q1	Q3	-
1	PFET Transistor	1RFD9113	-	Q2	-
1	24.00014 MHz Oscillator	-	OSC1	-	-
2	Capacitor, 100pF, 5%, 50V	-	-	-	C60, C61
6	Capacitor, 1000pF, 5%, 50V	-	C16, C29 C49, C51	-	C62 , C67
1	Capacitor, 0.012µF, 20%, 50V	-	-	C34	-
1	Capacitor, 0.02µF, 20%, 50V	-	-	C35	-
1	Capacitor, 0.047µF, 20%, 50V	-	-	C40	-
3	Capacitor, 0.01µF, 20%, 50V	-	-	C33	C63, C68
36	Capacitor, 0.1µF, 20%, 50V	-	Note 1	-	-
1	Capacitor, 0.15µF, 20%, 50V	-	-	C32	-
2	Capacitor, 0.33µF, 20%, 50V	-	C44, C46	-	-
1	Capacitor, 10µF, 10%, 25V	-	C45	-	-
5	Capacitor, 10µF, 20%, 25V	-	C6, C7, C8	C37, C38	-
1	Capacitor, 220µF, 20%, 16V	-	-	C39	-
1	Capacitor, 0.47µF, 20%, 250V	-	-	C36	-
1	Resistor, 10KΩ, 1%, 1/8W	-	R50	-	-

Table 1. RC9624AT Parts List (Cont'd)

Qty. Reqd.	Nomenclature or Description	Part or Identifying Number	Circuit		
			General	DAA/Speaker	Eye Pattern
1	Resistor, 11.1KΩ, 1%, 1/8W	-	R16	-	-
1	Resistor, 17.4KΩ, 1%, 1/8W	-	R46	-	-
1	Resistor, 23.7KΩ, 1%, 1/8W	-	-	R24	-
1	Resistor, 34.8KΩ, 1%, 1/8W	-	R7	-	-
1	Resistor, 43.2KΩ, 1%, 1/8W	-	R17	-	-
1	Resistor, 46.4KΩ, 1%, 1/8W	-	R47	-	-
1	Resistor, 66.5KΩ, 1%, 1/8W	-	R8	-	-
2	Resistor, 68.1KΩ, 1%, 1/8W	-	R6, R20	-	-
2	Resistor, 86.6KΩ, 1%, 1/8W	-	R45, R49	-	-
1	Resistor, 110KΩ, 1%, 1/8W	-	R10	-	-
2	Resistor, 900Ω, 1%, 1/8W	-	R21, R41	-	-
2	Resistor, 26KΩ, 1%, 1/8W	-	R23, R43	-	-
1	Resistor, 36.5KΩ, 1%, 1/8W	-	R55	-	-
1	Resistor, 3.0Ω, 5%, 1/8W	-	R57	-	-
1	Resistor, 10.0Ω, 5%, 1/8W	-	-	R37	-
1	Resistor, 680Ω, 5%, 1/8W	-	-	R29	-
1	Resistor, 750Ω, 5%, 1/8W	-	R33	-	-
2	Resistor, 3.0KΩ, 5%, 1/8W	-	R48, R58	-	-
1	Resistor, 3.9KΩ, 5%, 1/8W	-	-	R26	-
4	Resistor, 4.7KΩ, 5%, 1/8W	-	R3, R5	-	R63, R65
1	Resistor, 6.8KΩ, 5%, 1/8W	-	R18	-	-
1	Resistor, 8.2KΩ, 5%, 1/8W	-	-	R22	-
5	Resistor, 10KΩ, 5%, 1/8W	-	R2, R4, R40, R42, R44	-	-
2	Resistor, 15KΩ, 5%, 1/8W	-	-	R35, R36	-
1	Resistor, 18KΩ, 5%, 1/8W	-	-	R27	-
1	Resistor, 47KΩ, 5%, 1/8W	-	R9	-	-
1	Resistor, 56KΩ, 5%, 1/8W	-	-	R19	-
1	Resistor, 330KΩ, 5%, 1/8W	-	-	R30	-
1	Resistor, 470KΩ, 5%, 1/8W	-	-	R31	-
1	Resistor, 2.7MΩ, 5%, 1/8W	-	R56	-	-
3	Resistor, 2KΩ, 5%, 1/8W	-	R51	-	R62, R64
2	Resistor, 24KΩ, 5%, 1/8W	-	-	-	R60, R61
2	Inductor, 8.2μH	-	L1, L2	-	-
2	Inductor, 0.2μH	-	-	L3, L4	-
1	Varistor	SGT23813	-	R34	-
2	Zener Diode	1LL751	-	CR1, CR2	-
1	Diode	1N4148	-	CR3	-
2	Diode	1LL967	-	CR4, CR5	-
2	Diode	1N914B	-	-	CR6, CR7
1	Piezo-electric Speaker	-	-	SPKR1	-
2	RJ11 Phone Jacks	-	-	J1, J2	-

Note 1: C1, C2, C3, C4, C5, C10, C11, C12, C14, C15, C17, C18, C19, C25, C26, C27, C28, C30, C31, C41, C42, C43, C47, C48, C50, C52, C53, C64, C65, C66, C69, C70, C71, C72, C73, C75.

Table 2. RC9624AT Power Requirements

Mode	+5V	–5V	+12V	–12V	Total Power
Modem Devices Only					
Sleep	-	-	-	-	73 mW
Data Operation	-	-	-	-	305 mW
Fax Operation	275 mW	75 mW	-	-	350 mW
Full Board					
Sleep	155 mW	90 mW	40 mW	40 mW	325 mW
Data Operation	435 mW	180 mW	40 mW	40 mW	695 mW
Fax Operation	430 mW	92 mW	128 mW	40 mW	690 mW

Note: Power listed is typical @ 25°C.

Table 3. C19 Transparent Mode Interface Memory Definitions

Mnemonic	Location	Name/Description
ACK	5:2	**Acknowledge.** Sets when the C19 completes a modem interface memory read or write cycle.
CHANNEL DATA	0:0-7	**Channel Data Register.** Handles send/receive data for communication channel.
DDI	5:1	**Diagnostic Data Indicator.** Sets when diagnostic data transfer is completed (32-bits).
EFI	5:4	**Error Flag Indicator.** Sets when an error code is written to register 6 by the C19.
ERCDI	1:0	**Enable RCD Interrupt.** When set, RCD causes host interrupt.
ERROR CODE	6:0-7	**Error Code Register.** C19 writes error codes here.
ETCDI	1:1	**Enable TCD Interrupt.** When set, TCD causes host interrupt.
ETSI	1:2	**Enable Transparent Status Interrupt.** When set, bits 5:1 to 5:4 cause host interrupt.
EXIT	3:5	**Exit.** When set, the C19 exits from transparent mode (if RMW=0).
IIDn	2:1,2	**Interrupt Identification Code.** 0 = N/A, 1 = TCD, 2 = RCD, 3 = Transparent Status.
IP	2:0	**Interrupt Pending.** Set when C19 is generating a host interrupt.
READ ADDRESS	4:0-4	**Read Address.** Number of interface memory register to be read.
READ/WRITE DATA	7:0-7	**Read/Write Data.** Handles read or write data for modem interface memory.
RCD	5:0	**Receive Channel Data.** Sets when the channel data register has been filled by C19.
RMW	3:6	**Read Modify Write.** Causes setting or resetting of interface memory bits per mask in register 7.
SET	3:5	**Set.** Selects set or reset for RMW = 1 (Read Modify Write Cycle). 1 = Set, 0 = Reset.
TCD	5:5	**Transmit Channel Data.** Sets when the fax modem requires data.
WRITE ADDRESS	3:0-4	**Write Address.** Number of interface memory register to be written.

C19 EXPANSION BUS (HARDWARE)

Modem Device Package Considerations. The C19 available address space for external memory depends on the package type. The PLCC package provides external addressing for 280H through BFFFH. The QUIP package provides external addressing for 2000H through 3FFFH. Both packages support address lines A0 through A12, but the PLCC package also supports A13 through A15. These additional address lines allow the PLCC package to provide more addressing space than the QUIP package. It is suggested that all data/facsimile modem designs use the PLCC package because of the extra addressing capabilities.

Addressing. The C19 can address up to 64K of memory. The external memory may be either RAM or ROM. The C19 memory map is shown below (all values in hex).

0 - 027F	Internal RAM
0280 - BFFF	External memory
C000 - FFFF	Internal ROM

Note that the internal software writes the data modem eye pattern data to locations 3FFEH through 3FFFH.

External PROM. Any external PROM must be partially located between address 2000H through 201FH. An AAH at location 2000H indicates to the C19 that an external PROM is present. If any other value is read at 2000H then the C19 assumes that a PROM is not present.

External Memory Access Time. The C19 operates at an internal clock rate of 6 MHz. The C19 expansion bus operates at one of two selectable speeds. The normal expansion bus mode operates at the same speed as the internal bus. The extended expansion bus mode operates slower at one-half the internal bus speed. The C19 defaults to the extended bus access time. An internal C19 register must be modified in order to use the faster (normal bus) access time. (Refer to the C18 Technical Reference Manual for detail bus timing information.)

C19 EXPANSION BUS (SOFTWARE)

While in Data modem operation, all AT commands are processed using the internal command interpreter which divides the AT commands into three types:

1. Basic Commands
2. Dial Commands
3. Ampersand (&) Commands

The required external memory vector table format for locations 2000H through 201FH is shown in Table 4.

Power-on Initialization. During the power-on initialization routine the C19 reads address 2000H. If an AAH character is read, the C19 sets an internal flag that indicates an external memory is present. At the end of the internal initialization routine the C19 implements a jump to subroutine (JSR) to address 2001H. The external code then jumps to an external initialization routine or uses a return from subroutine (RTS) instruction. Upon completing the external initialization routine the external code performs an RTS instruction. This instruction causes the C19 to return to internal code and places the device in idle mode. The C19 stays in idle mode until an AT command string is received.

AT Command String Processing. The following discussion assumes that external memory is present. After an AT command string is received, the C19 starts the command process by determining the command type. It then reads the "Table # of bytes" in the expansion memory table (2000H - 201FH) for the appropriate command type. If the value is positive, the C19 reads the AT command comparison string, the location of which is given in the "command table address bytes" in the vector table (Table 4). If the entered command matches one of the commands in the command table then the C19 jumps to the external code processor specified in the vector table. If the command does not match any character in the command table, or the "table # of bytes" equals -1, then the C19 uses its internal command table for processing the command (Figure 5).

Before the expansion command processor is entered, the command character is stored in the accumulator. The command table index for the AT command is stored in register X. Variable CMDIPT points to the next command in the command buffer (CMDBUF).

Upon process completion the external code implements an RTS instruction. If an error occurs while processing the command, the external code may first output an error message to the host. Next, the code resets several internal flags and then performs an RTS instruction. Resetting the internal flags, causes the internal code to stop processing the rest of the command string and to enter the idle mode.

Addresses of commonly used data modem I/O functions are shown in Table 5. The input and output routines cannot be used when configured for facsimile modem operation.

TEST EQUIPMENT AND ASSEMBLER REQUIREMENTS

A cross assembler for the C19, designed to run on an IBM PC, is available from Rockwell. This product is called the C18/C19 Cross Assembler/Linker for PC (product order number C19-PCAS). A user's manual for this product is also available (order number 409).

Test of assembled code may be performed on a PROM emulator. The emulator access time must conform to the C19 expansion bus timing requirements.

Table 4. C19 External Memory Vectors

C19 Byte Address	Byte Contents
2000H	External AT command enable flag AAH
2001H	Power_on init instruction byte 0
2002H	Power_on init instruction byte 1
2003H	Power_on init instruction byte 2
2004H	Basic command processor address LSB
2005H	Basic command processor address MSB
2006H	Basic command table address LSB
2007H	Basic command table address MSB
2008H	Basic command table # bytes - 1
2009H	Dial command processor address LSB
200AH	Dial command processor address MSB
200BH	Dial command table address LSB
200CH	Dial command table address MSB
200DH	Dial command table # bytes - 1
200EH	"&" command processor address LSB
200FH	"&" command processor address MSB
2010H	"&" command table address LSB
2011H	"&" command table address MSB
2012H	"&" command table # bytes - 1
2013H-201FH	Reserved for future use

Table 5. Commonly Used Data Modem I/O Functions*

Item	Address (Hex)	Function
CMDCVT	C000	Terminal Input Routine
CMDBUF	0140-0168	Terminal Input Command Buffer
CMDIPT	0169	Terminal Input Command Buffer Pointer
CMDPUT	C00B	Terminal Output Routine
CMDOBF	016A-0178	Terminal Output Buffer
CMDOIP	017A	Terminal Output Buffer Insert Pointer
CMDOBC	0179	Terminal Output Buffer Counter
RESET	C035	Data Modem Reset (Note 1)
S0-S27	004C-0067	S-Register RAM Locations

* RC224AT E-Code.