54160/74160 Synchronous Decade Counter with Direct Clear

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF
T.I.											SN54LS160	J①			W①	SN54160	J①			W①					
											SN74LS160	J①	N①			SN74160	J①	N①							
FAIRCHILD											FM54LS160/FM93LS160	D①			F①	FM93160	D①								
											FC74LS160/FC93LS160	D①	P①		F①	FC74160/FC93160	D①	P①		F①					
MOTOROLA											SN74LS160		P①			SN74160		P①							
N.S.C.											DM54LS160		①			DM54160A									
											DM74LS160		①			DM74160A									
PHILIPS																N74160		①							
SIGNETICS																S54160	F①	B①		W①					
											N74LS160		A①			N74160	F①	B①							
SIEMENS																FLJ401		①							
FUJITSU											74LS160		M①												
HITACHI											HD74LS160		P①			HD74160		①P①							
MITSUBISHI											M74LS160		P①			M53360		P①							
AMD	Am54S160		①								Am74LS160		①												
	Am74S160		①								Am54LS160		①												
TOSHIBA																									

Electrical Characteristics SN54LS160/SN74LS160

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54LS	−55°C to 125°C
Input voltage	7V		SN74LS	0°C to 70°C
		Storage temperature range		−65°C to 150°C

recommended operating conditions

		SN54LS160 MIN	NOM	MAX	SN74LS160 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup}	Data inputs A, B, C, D	20			20			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

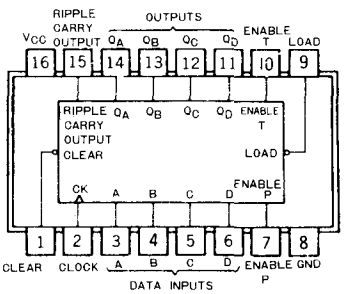
electrical characteristics over recommended operating free-air temperature range

PARAMETER *		TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC}=MIN, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=8mA			0.35	0.5	V
I_I	Input current at maximum input voltage: Load, clock or enable T	V_{CC}=MAX, V_I=7V				0.2	mA
	Input current at maximum input voltage: Other inputs					0.1	
I_{IH}	High-level input current: Load, clock or enable T	V_{CC}=MAX, V_I=2.7V				40	μA
	High-level input current: Other inputs					20	
I_{IL}	Low-level input current: Load, clock or enable T	V_{CC}=MAX, V_I=0.4V				−0.8	mA
	Low-level input current: Other inputs					−0.4	
I_{OS}	Short-circuit output current ◆	V_{CC}=MAX		−20		100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=MAX, See Note 2	SN54LS		18	31	mA
			SN74LS		18	31	
I_{CCL}	Supply current, all outputs low	V_{CC}=MAX, See Note 3	SN54LS		19	32	mA
			SN74LS		19	32	
f_{max}	Maximum clock frequency	V_{CC}=−5V, T_A=25°C, C_L=15pF, R_L=2kΩ, See Note 4		25	32		ns
t_{PLH}	from Clock to output Ripple carry				20	35	ns
t_{PHL}					18	35	
t_{PLH}	from Clock (load input high) to output Any Q				13	24	ns
t_{PHL}					18	27	
t_{PLH}	from Clock (load input low) to output Any Q				13	24	ns
t_{PHL}					18	27	
t_{PLH}	from Enable T to output Ripple carry				9	14	ns
t_{PHL}					9	14	
t_{PHL}	from Clear to output Any Q				20	28	ns

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC}=5V, T_A=25°C.
◆ Not more than one output should be shorted at a time
* t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low level output

Pin Assignment (Top View)

①



positive logic:

NOTES: 1. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
2. I_{CCH} is measured with the load input high, then again with the load input low, *with all other inputs high and all outputs open.*
3. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.
4. Propagation delay for clearing is measured from the clear input for the '160.

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