M74LS290P

DECADE COUNTER

DESCRIPTION

The M74LS290P is a semiconductor integrated cirucit containing an asynchronous decade counter function with direct reset and direct 9-set inputs.

FEATURES

- Direct reset inputs provided
- Direct 9-set inputs provided
- Usable independently as binary and divide-by-5 counter
- High-speed counting (f_{max}= 75MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

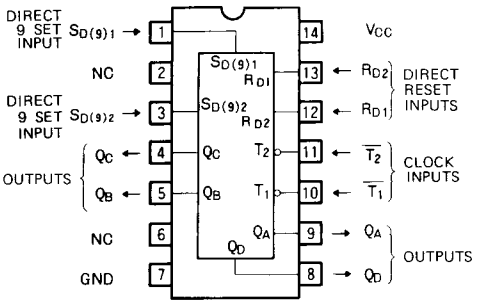
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A, Q_B, Q_C and Q_D. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-5 counters can be reset or set to 9 simultaneously by setting direct reset inputs R_{D1} and R_{D2} and direct 9 set inputs $S_{D(9)1}$ and $S_{D(9)2}$ high. For use as a counter, either R_{D1} or R_{D2}, or both, and $S_{D(9)1}$ or $S_{D(9)2}$, or both, are set low.

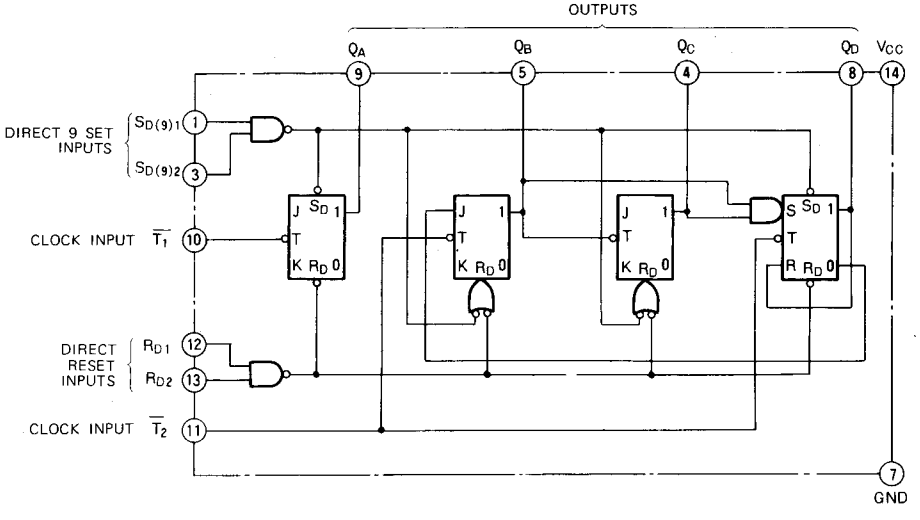
Also provided is the M74LS90P with the same functions and electrical characteristics. This device differs only in its pin configuration.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

BLOCK DIAGRAM



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FUNCTION TABLE (Note 1)

$\overline{T}$	R_{D1}	R_{D2}	$S_{D(9)1}$	$S_{D(9)2}$	Q_A	Q_B	Q_C	Q_D
X	H	H	L	X	L	L	L	L
X	H	H	X	L	L	L	L	L
X	X	X	H	H	H	L	L	H
↓	L	X	L	X	Count			
↓	X	L	X	L	Count			
↓	L	X	X	L	Count			
↓	X	L	L	X	Count			

Note 1: ↓ : Transition from high to low
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(1) Valid when Q_A and $\overline{T}_2$ are connected and $\overline{T}_1$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75℃$, unless other wise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltae	Inputs $\overline{T}_1$, $\overline{T}_2$	−0.5 ~ +5.5	V
		Inputs R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	HIgh-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I= 2 V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltate		V_{CC}=4.75V	I_{OL}=4 mA (Note 2)		0.25	0.4	V
			V_I=0.8V, V_I= 2 V	I_{OL}=8 mA (Note 2)		0.35	0.5	V
I_{IH}	High-level input current	R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{T}_1$					40	
		$\overline{T}_2$					80	
		$\overline{T}_1$	V_{CC}=5.25V, V_I=5.5V				0.2	mA
		$\overline{T}_2$					0.4	
		R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		$\overline{T}_1$					−2.4	
		$\overline{T}_2$					−3.2	
I_{OS}	Short-circuit output current (Note 3)		V_{CC}=5.25V, V_O= 0 V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC}= 5 V, T_a=25℃.

Note 2: Output Q_A should be tested with input $\overline{T}_2$ connected to output Q_A.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T}_1$, $\overline{T}_2$, $S_{D(9)1}$ and $S_{D(9)2}$ at 0V after R_{D1} and R_{D2} have been set to 0V after 4.5V.

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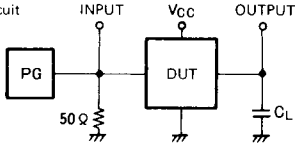
SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L = 15pF (Note 5)	32	75		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			7	16	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			15	48	ns
t_{PHL}				16	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			7	16	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			15	32	ns
t_{PHL}				15	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_D			7	32	ns
t_{PHL}				8	35	ns
t_{PHL}	Low-to-high-level output propagation time, from inputs $S_{D(9)1}$, $S_{D(9)2}$ to outputs Q_A, Q_D			17	40	ns
t_{PLH}	High-to-low-level output propagation time, from inputs $S_{D(9)1}$, $S_{D(9)2}$ to outputs Q_B, Q_C			10	30	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1}, R_{D2} to outputs Q_A, Q_B, Q_C, Q_D			14	40	ns

Note 5: Measurement circuit

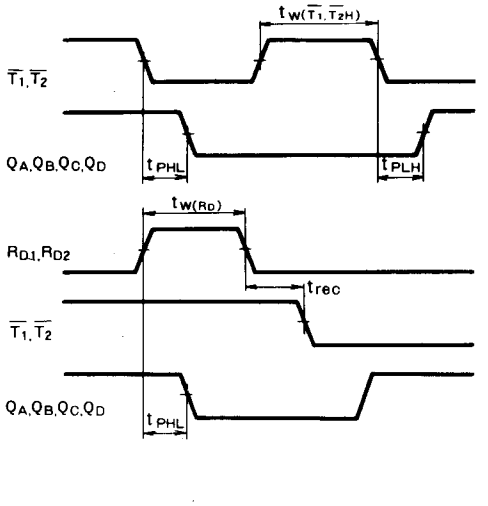


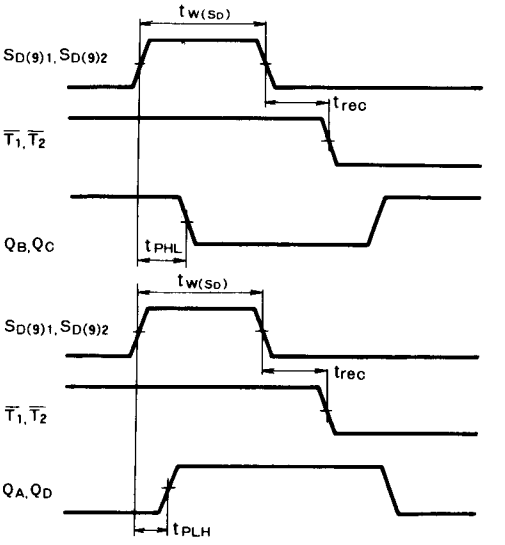
(1) The pusle generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3$V_{P\text{-}P}$, Zo = 50Ω.
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		15	6		ns
$t_{w(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	17		ns
$t_{w(RD)}$	Direct reset R_{D1}, R_{D2} pulse width		15	5		ns
$t_{w(SD)}$	Direct 9 set $S_{D(9)1}$, $S_{D(9)2}$ pulse width		15	5		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(RD)}$	Recovery time R_{D1}, R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns
$t_{rec(SD)}$	Recovery time $S_{D(9)1}$, $S_{D(9)2}$ to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





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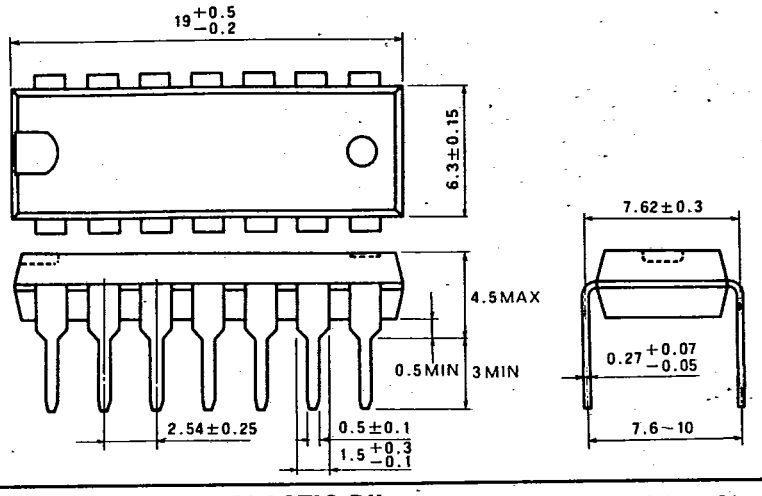
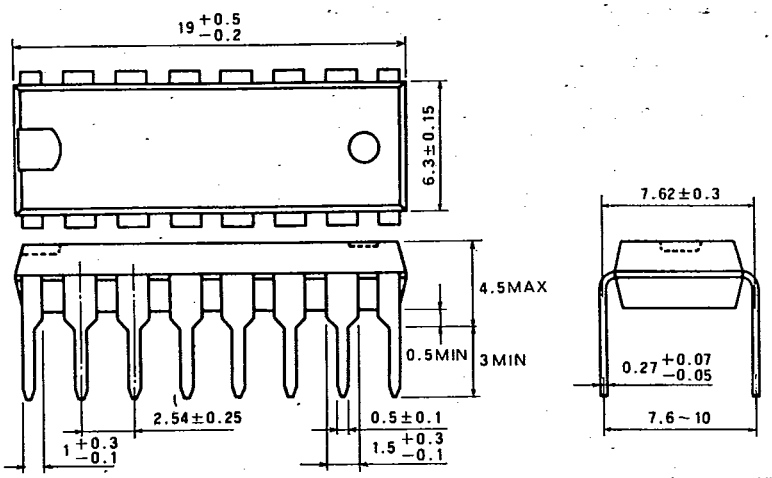
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm