

RSL10

Bluetooth® 5 Radio System-on-Chip (SoC)

Introduction

RSL10 is an ultra-low-power, highly flexible multi-protocol 2.4 GHz radio specifically designed for use in high-performance wearable and medical applications. With its Arm® Cortex®-M3 Processor and LPDSP32 DSP core, RSL10 supports Bluetooth low energy technology and 2.4 GHz proprietary protocol stacks, without sacrificing power consumption.

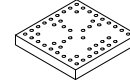
Key Features

- Rx Sensitivity (Bluetooth Low Energy Mode, 1 Mbps): -94 dBm
- Data Rate: 62.5 to 2000 kbps
- Transmitting Power: -17 to +6 dBm
- Peak Rx Current = 5.6 mA (1.25 V VBAT)
- Peak Rx Current = 3.0 mA (3 V VBAT)
- Peak Tx Current (0 dBm) = 8.9 mA (1.25 V VBAT)
- Peak Tx Current (0 dBm) = 4.6 mA (3 V VBAT)
- Bluetooth 5 Certified with LE 2M PHY Support
- Arm Cortex-M3 Processor Clocked at up to 48 MHz
- LPDSP32 for Audio Codec
- Supply Voltage Range: 1.1 – 3.3 V
- Current Consumption (1.25 V VBAT):
 - ◆ Deep Sleep, IO Wake-up: 50 nA
 - ◆ Deep Sleep, 8 kB RAM Retention: 300 nA
 - ◆ Audio Streaming at 7 kHz Audio BW: 1.8 mA RX, 1.8 mA TX
- Current Consumption (3 V VBAT):
 - ◆ Deep Sleep, IO Wake-up: 25 nA
 - ◆ Deep Sleep, 8 kB RAM Retention: 100 nA
 - ◆ Audio Streaming at 7 kHz Audio BW: 0.9 mA RX, 0.9 mA TX
- 384 kB of Flash Memory
- Highly-integrated System-on-Chip (SoC)
- Supports FOTA (Firmware Over-The-Air) Updates

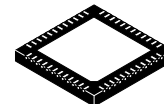


ON Semiconductor®

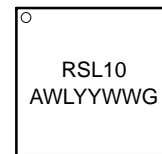
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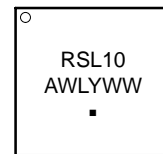
WLCSP51
CASE 567MT



1 48
QFN48
CASE 485BA



(QFN48)



(WLCSP51)

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y or YY = Year
WW = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------------|-------------------|--------------------|
| NCH-RSL10-101WC51-ABG | WLCSP51 (Pb-Free) | 5000 / Tape & Reel |
| NCH-RSL10-101Q48-ABG | QFN48 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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FEATURES

- **Arm Cortex–M3 Processor:** A 32–bit core for real–time applications, specifically developed to enable high–performance low–cost platforms for a broad range of low–power applications.
- **LPDSP32:** A 32–bit Dual Harvard DSP core that efficiently supports audio codecs required for wireless audio communication. Various codecs are available to customers through libraries that are included in RSL10’s development tools.
- **Radio Frequency Front–End:** Based on a 2.4 GHz RF transceiver, the RFFE implements the physical layer of the Bluetooth low energy technology standard and other proprietary or custom protocols.
- **Protocol Baseband Hardware:** Bluetooth 5 certified and includes support for a 2 Mbps RF link and custom protocol options. The RSL10 baseband stack is supplemented by support structures that enable implementation of ON Semiconductor and customer designed custom protocols.
- **Highly–Integrated SoC:** The dual–core architecture is complemented by high–efficiency power management units, oscillators, flash and RAM memories, a DMA controller, along with a full complement of peripherals and interfaces.
- **Deep Sleep Mode:** RSL10 can be put into a Deep Sleep Mode when no operations are required. Various Deep Sleep Mode configurations are available, including:
 - ◆ “IO wake–up” configuration. The power consumption in deep sleep mode is 50 nA (1.25 V VBAT).
 - ◆ Embedded 32 kHz oscillator running with interrupts from timer or external pin. The total current drain is 90 nA (1.25 V VBAT).
 - ◆ As above with 8 kB RAM data retention. The total current drain is 300 nA (1.25 V VBAT).
 - ◆ With the exception of IO wake up only configuration, the on–chip buck converter can also be enabled to reduce current consumption in Deep Sleep Mode (at higher VBAT voltages).
- **Standby Mode:** Can be used to reduce the average power consumption for off–duty cycle operation, ranging typically from a few ms to a few hundreds of ms. The typical chip power consumption is 30 μ A in Standby Mode.
- **Multi–Protocol Support:** Using the flexibility provided by LPDSP32, the Arm Cortex–M3 processor, and the RF front–end; proprietary protocols and other custom protocols are supported.
- **Flexible Supply Voltage:** RSL10 integrates high–efficiency power regulators and has a VBAT range of 1.1 to 3.3 V. See Table 2. RECOMMENDED OPERATING CONDITIONS.
- **Highly Configurable Interfaces:** I²C, UART, two SPI interfaces, PCM interface, multiple GPIOs. It also supports a digital microphone interface (DMIC) and an output driver (OD).
- **The Asynchronous Sample Rate Converter (ASRC) Block and Audio Sink Clock Blocks** Provides a means of synchronizing the audio sample rate between an audio source and an audio sink. The audio sink clock also provides a high accuracy mechanism to measure an input clock used for the RTC or protocol timing.
- **Flexible Clocking Scheme:** RSL10 must be clocked from the XTAL/PLL of the radio front–end at 48 MHz when transmitting or receiving RF traffic. When RSL10 is not transmitting/receiving RF traffic, it can run off the 48 MHz XTAL, the internal RC oscillators, the 32 kHz oscillator, or an external clock. A low frequency RTC clock at 32 kHz can also be used in Deep Sleep Mode. It can be sourced from either the internal XTAL, the RC oscillator, or a digital input pad.
- **Diverse Memory Architecture:** 76 kB of SRAM program memory and 88 kB of SRAM data memory are available. A total of 384 kB of flash is available to store the Bluetooth stack and other applications. The Arm Cortex–M3 processor can execute from SRAM and/or flash.
- **IP Protection Feature:** Ensures that the customer’s flash contents cannot be copied by a third party. It prevents any core or memory from being accessed externally after the chip has booted.
- **Ultra–Low Power Consumption Application Examples:**
 - ◆ **Audio Signal Streaming:** IDD = 1.8 mA @ VBAT 1.25 V in Rx Mode for receiving, decoding and sending an 7 kHz bandwidth audio signal to the SPI interface using a proprietary custom audio protocol from ON Semiconductor.
 - ◆ **Low Duty Cycle Advertising:** IDD 1.1 μ A for advertising at all three channels at 5 second intervals @ VBAT 3 V, DCDC converter enabled.
- **RoHS Compliant Device**

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RSL10 INTERNAL BLOCK DIAGRAM

The block diagram of the RSL10 chip is shown in Figure 1.

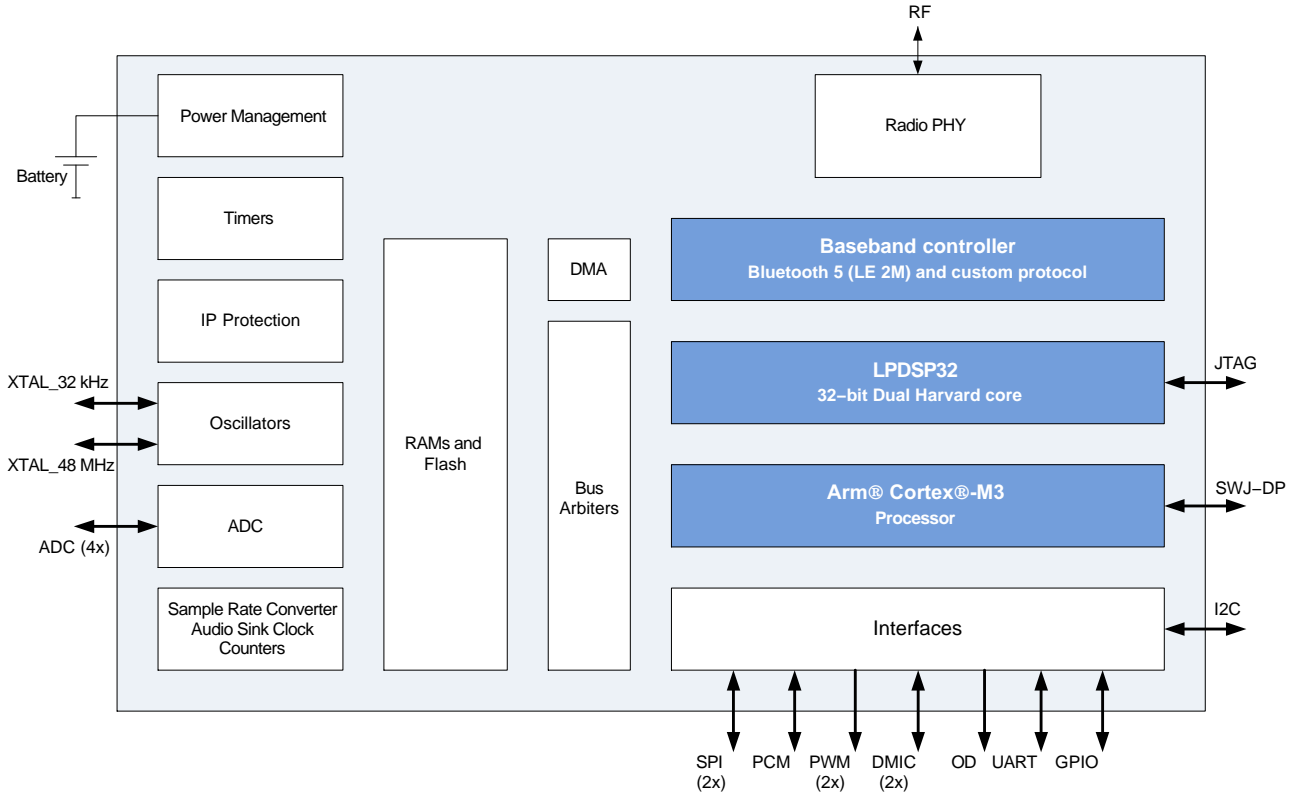


Figure 1. RSL10 Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|-------------------------|------------------------------|-----------------------|------------------------|------|
| V _{BAT} | Power supply voltage | – | 3.63 | V |
| V _{DDO} | I/O supply voltage | – | 3.63 | V |
| V _{SSRF} | RF front-end ground | –0.3 | – | V |
| V _{SSA} | Analog ground | –0.3 | – | V |
| V _{SSD} | Digital core and I/O ground | –0.3 | – | V |
| V _{in} | Voltage at any input pin | V _{SSD} –0.3 | V _{DDO} + 0.3 | V |
| T _{functional} | Functional temperature range | –40 | 85 | °C |
| T _{storage} | Storage temperature range | –40 | 85 | °C |

Caution: Class 2 ESD Sensitivity, JEDEC22–A114–B (2000 V)
The QFN package meets 450 V CDM level

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 2. RECOMMENDED OPERATING CONDITIONS

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|--------------------------------|--------|---|------|------|-----|-------|
| Supply voltage operating range | VBAT | Input supply voltage on VBAT pin (Note 1) | 1.18 | 1.25 | 3.3 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:

- Maximum Tx power 0 dBm.
- SYSCLK ≤ 24 MHz.
- Functional temperature range limited to 0–50 deg C

The following trimming parameters should be used:

- VCC = 1.10 V
- VDDC = 0.92 V
- VDDM = 1.05 V, will be limited by VCC at end of battery life
- VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled

RSL10 should enter in end-of-battery-life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT ≥ 1.10 V under the restricted operating conditions described above.

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|-------------|--------|------------|-----|-----|-----|-------|
|-------------|--------|------------|-----|-----|-----|-------|

OVERALL

| | | | | | | |
|--|-------|---|---|------|---|----|
| Current consumption RX, VBAT = 1.25 V, low latency | IVBAT | RX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. | – | 1.8 | – | mA |
| Current consumption TX, VBAT = 1.25 V, low latency | IVBAT | TX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm | – | 1.8 | – | mA |
| Current consumption RX, VBAT = 1.25 V | IVBAT | RX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 37 ms delay. | – | 1.15 | – | mA |
| Deep sleep current, example 1, VBAT = 1.25 V | Ids1 | Wake up from wake up pin. | – | 50 | – | nA |
| Deep sleep current, example 2, VBAT = 1.25 V | Ids2 | Embedded 32 kHz oscillator running with interrupts from timer or external pin. | – | 90 | – | nA |
| Deep sleep current, example 3, VBAT = 1.25 V | Ids3 | As Ids2 but with 8 kB RAM data retention. | – | 300 | – | nA |
| Standby Mode current, VBAT = 1.25 V | Istb | Digital blocks and memories are not clocked and are powered at a reduced voltage. | – | 30 | – | µA |
| Current consumption RX, VBAT = 3 V | IVBAT | RX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. | – | 0.9 | – | mA |
| Current consumption TX, VBAT = 3 V | IVBAT | TX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm | – | 0.9 | – | mA |
| Deep sleep current, example 1, VBAT = 3 V | Ids1 | Wake up form wake up pin. | – | 25 | – | nA |
| Deep sleep current, example 2, VBAT = 3 V | Ids2 | Embedded 32 kHz oscillator running with interrupts from timer or external pin. | – | 40 | – | nA |
| Deep sleep current, example 3, VBAT = 3 V | Ids3 | As Ids2 but with 8 kB RAM data retention. | – | 100 | – | nA |
| Standby Mode current, VBAT = 3 V | Istb | Digital blocks and memories are not clocked and are powered at a reduced voltage. | – | 17 | – | µA |

EEMBC ULPMark BENCHMARK, CORE PROFILE

| | | | | | | |
|------------------|--|--|---|------|---|----------|
| ULPMark CP 3.0 V | | Arm Cortex-M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183 | – | 1090 | – | ULP Mark |
|------------------|--|--|---|------|---|----------|

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|---|---------------------------|--|------|------|----------------------|---------------|
| EEMBC ULPMark BENCHMARK, CORE PROFILE | | | | | | |
| ULPMark CP 2.1 V | | Arm Cortex-M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183 | – | 1260 | – | ULP Mark |
| EEMBC CoreMark BENCHMARK for the Arm Cortex-M3 Processor and the LPDSP32 DSP | | | | | | |
| Arm Cortex-M3 processor running from RAM | | At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified | – | 159 | – | Core Mark |
| LPDSP32 running from RAM | | At 48 MHz SYSCLK Using the 2017.03-SP3-2 release of the Synopsys LPDSP32 C compiler | – | 133 | – | Core Mark |
| Arm Cortex-M3 processor and LPDSP32 running from RAM, VBAT = 1.25 V | | At 48 MHz SYSCLK | – | 108 | – | Core Mark/ mA |
| Arm Cortex-M3 processor and LPDSP32 running from RAM, VBAT = 3 V | | At 48 MHz SYSCLK | – | 257 | – | Core Mark/ mA |
| INTERNALLY GENERATED VDDC: Digital Block Supply Voltage | | | | | | |
| Supply voltage: operating range | VDDC | | 0.92 | 1.15 | 1.32 (Note 2) | V |
| Supply voltage: trimming range | VDDC _{RANGE} | | 0.75 | – | 1.38 | V |
| Supply voltage: trimming step | VDDC _{STEP} | | – | 10 | – | mV |
| INTERNALLY GENERATED VDDM: Memories Supply Voltage | | | | | | |
| Supply voltage: operating range | VDDM | | 1.05 | 1.15 | 1.32 (Note 3) | V |
| Supply voltage: trimming range | VDDM _{RANGE} | | 0.75 | – | 1.38 | V |
| Supply voltage: trimming step | VDDM _{STEP} | | – | 10 | – | mV |
| INTERNALLY GENERATED VDDRF: Radio Front end supply voltage | | | | | | |
| Supply voltage: operating range | VDDRF | | 1.00 | 1.10 | 1.32 (Notes 4 and 5) | V |
| Supply voltage: trimming range | VDDRF _{RANGE} | | 0.75 | – | 1.38 | V |
| Supply voltage: trimming step | VDDRF _{STEP} | | – | 10 | – | mV |
| INTERNALLY GENERATED VDDPA: Optional Radio Power Amplifier Supply Voltage | | | | | | |
| Supply voltage: operating range | VDDPA | | 1.05 | 1.3 | 1.68 | V |
| Supply voltage: trimming range | VDDPA _{RANGE} | | 1.05 | – | 1.68 | V |
| Supply voltage: trimming step | VDDPA _{STEP} | | – | 10 | – | mV |
| Supply voltage: trimming step | DCDC _{STEP} | | – | 10 | – | mV |
| VDDO PAD SUPPLY VOLTAGE: Digital Level High Voltage | | | | | | |
| Digital I/O supply | VDDO | | 1.1 | 1.25 | 3.3 | V |
| INDUCTIVE BUCK DC-DC CONVERTER | | | | | | |
| VBAT range when the DC-DC converter is active (Note 6) | DCDC _{IN_RANGE} | | 1.4 | – | 3.3 | V |
| VBAT range when the LDO is active | LDO _{IN_RANGE} | | 1.1 | – | 3.3 | V |
| Output voltage: trimming range | DCDC _{OUT_RANGE} | | 1.1 | 1.2 | 1.32 | V |
| Supply voltage: trimming step | DCDC _{STEP} | | – | 10 | – | mV |
| POWER-ON RESET | | | | | | |
| POR voltage | VBAT _{POR} | | 0.4 | 0.8 | 1.0 | V |

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|--|---------------|---|------|------|------|----------|
| RADIO FRONT-END: General Specifications | | | | | | |
| RF input impedance | Z_{in} | Single ended | – | 50 | – | Ω |
| Input reflection coefficient | S_{11} | All channels | – | – | –8 | dB |
| Data rate FSK / MSK / GFSK | R_{FSK} | OQPSK as MSK | 62.5 | 1000 | 3000 | kbps |
| Data rate 4-FSK | | | – | – | 4000 | kbps |
| On-air data rate | bps | GFSK | 250 | – | 2000 | kbps |
| RADIO FRONT-END: Crystal and Clock Specifications | | | | | | |
| Xtal frequency | F_{XTAL} | Fundamental | 48 | | | MHz |
| Equiv. series Res. | ESR_{XTAL} | RSL10 has internal load capacitors, additional external capacitors are not required | 20 | – | 80 | Ω |
| Differential equivalent load capacitance | CL_{XTAL} | Internal load capacitors (NO EXTERNAL LOAD CAPACITORS REQUIRED) | 6 | 8 | 10 | pF |
| Settling time | | | – | 0.5 | 1.5 | ms |
| RADIO FRONT-END: Synthesizer Specifications | | | | | | |
| Frequency range | F_{RF} | Supported carrier frequencies | 2360 | – | 2500 | MHz |
| RX frequency step | | RX Mode frequency synthesizer resolution | – | – | 100 | Hz |
| TX frequency step | | TX Mode frequency synthesizer resolution | – | – | 600 | Hz |
| PLL Settling time, RX | t_{PLL_RX} | RX Mode | – | 15 | 25 | μ s |
| PLL Settling time, TX | t_{PLL_TX} | TX mode, BLE modulation | – | 5 | 10 | μ s |
| RADIO FRONT-END: Receive Mode Specifications | | | | | | |
| Current consumption at 1 Mbps, VBAT = 1.25 V | $IBAT_{RFRX}$ | VDDRF = 1.1 V, 100% duty cycle | – | 5.6 | – | mA |
| Current consumption at 2 Mbps, VBAT = 1.25 V | $IBAT_{RFRX}$ | VDDRF = 1.1 V, 100% duty cycle | – | 6.2 | – | mA |
| Current consumption at 1 Mbps, VBAT = 3 V, DC-DC | $IBAT_{RFRX}$ | VDDRF = 1.1 V, 100% duty cycle | – | 3.0 | – | mA |
| Current consumption at 2 Mbps, VBAT = 3 V, DC-DC | $IBAT_{RFRX}$ | VDDRF = 1.1 V, 100% duty cycle | – | 3.4 | – | mA |
| RX Sensitivity, 0.25 Mbps | | 0.1% BER (Notes 7, 8) | – | –97 | – | dBm |
| RX Sensitivity, 0.5 Mbps | | 0.1% BER (Notes 7, 8) | – | –96 | – | dBm |
| RX Sensitivity, 1 Mbps, BLE | | 0.1% BER (Notes 7, 8) Single-ended on chip antenna match to 50 Ω | – | –94 | – | dBm |
| RX Sensitivity, 2 Mbps, BLE | | 0.1% BER (Notes 7, 8) | – | –92 | – | dBm |
| RSSI effective range | | Without AGC | – | 60 | – | dB |
| RSSI step size | | | – | 2.4 | – | dB |
| RX AGC range | | | – | 48 | – | dB |
| RX AGC step size | | Programmable | – | 6 | – | dB |
| Max usable signal level | | 0.1% BER | 0 | 5 | – | dBm |
| RADIO FRONT-END: Transmit Mode Specifications | | | | | | |
| Tx peak power consumption at VBAT = 1.25 V (Note 9) | $IBAT_{RFTX}$ | Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, LDO mode | – | 8.9 | – | mA |
| | | Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, LDO mode | – | 17.4 | – | mA |
| | | Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, LDO mode | – | 25 | – | mA |

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|--|----------------------|---|------|------|-----|-------|
| RADIO FRONT-END: Transmit Mode Specifications | | | | | | |
| Tx peak power consumption at VBAT = 3 V (Note 9) | IBAT _{RFTX} | Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, DC-DC mode | – | 4.6 | – | mA |
| | | Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, DC-DC mode | – | 8.6 | – | mA |
| | | Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, DC-DC mode | – | 12 | – | mA |
| Transmit power range | | BLE or 802.15.4 OQPSK | –17 | +0.5 | +6 | dBm |
| Transmit power step size | | Full band. | – | 2 | – | dB |
| Transmit power accuracy | | Tx power 3 dBm. Full band. Relative to the typical value. | –1.5 | – | +1 | dB |
| | | Tx power 0 dBm. Full band. Relative to the typical value. | –1.5 | – | 1.5 | dB |
| Power in 2 nd harmonic | | 0 dBm mode. 50 Ω for “Typ” value. (Note 10) | – | –31 | –18 | dBm |
| Power in 3 rd harmonic | | 0 dBm mode. 50 Ω for “Typ” value. (Note 10) | – | –40 | –31 | dBm |
| Power in 4 th harmonic | | 0 dBm mode. 50 Ω for “Typ” value. (Note 10) | – | –49 | –42 | dBm |

ADC

| | | | | | | |
|----------------------------|----------------------|--|--------|----|------|------|
| Resolution | ADC _{RES} | | 8 | 12 | 14 | bits |
| Input voltage range | ADC _{RANGE} | | 0 | – | 2 | V |
| INL | ADC _{INL} | | –2 | – | +2 | mV |
| DNL | ADC _{DNL} | | –1 | – | +1 | mV |
| Channel sampling frequency | ADC _{CH_SF} | For the 8 channels sequentially, SLOWCLK = 1 MHz | 0.0195 | – | 6.25 | kHz |

32 kHz ON-CHIP RC OSCILLATOR

| | | | | | | |
|---------------------|----------------------|--|----|-----|----|-----|
| Untrimmed Frequency | Freq _{UNTR} | | 20 | 32 | 50 | kHz |
| Trimming steps | Steps | | – | 1.5 | – | % |

3 MHz ON-CHIP RC OSCILLATOR

| | | | | | | |
|---------------------|----------------------|--|---|-----|---|-----|
| Untrimmed Frequency | Freq _{UNTR} | | 2 | 3 | 5 | MHz |
| Trimming steps | Steps | | – | 1.5 | – | % |
| Hi Speed mode | Fhi | | – | 10 | – | MHz |

32 kHz ON-CHIP CRYSTAL OSCILLATOR (Note 11)

| | | | | | | |
|------------------------------|---------------------|--|----|-------|------|----|
| Output Frequency | Freq _{32k} | Depends on xtal parameters | – | 32768 | – | Hz |
| Startup time | | | – | 1 | 3 | s |
| Internal load trimming range | | Steps of 0.4 pF | 0 | | 25.2 | pF |
| Load Capacitance | | No external load capacitors required. Maximum external parasitic capacity allowed (package, routing, etc.) | – | – | 3.5 | pF |
| ESR | | | – | – | 100 | kΩ |
| Duty Cycle | | | 40 | 50 | 60 | % |

DC CHARACTERISTICS OF THE DIGITAL PADS – With VDDO = 2.97 V – 3.3 V, nominal: 3.0 V Logic

| | | | | | | |
|------------------------------|-----------------|--|----------|---|----------|---|
| Voltage level for high input | V _{IH} | | 2 | – | VDDO+0.3 | V |
| Voltage level for low input | V _{IL} | | VSSD–0.3 | – | 0.8 | V |

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|--|-----------------|------------|------------|-----|------------|--------------------|
| DC CHARACTERISTICS OF THE DIGITAL PADS – With VDDO = 1.1 V – 1.32 V, nominal: 1.2 V Logic | | | | | | |
| Voltage level for high Input | V _{IH} | | 0.65* VDDO | – | VDDO+0.3 | V |
| Voltage level for low input | V _{IL} | | VSSD–0.3 | – | 0.35* VDDO | V |
| DIO DRIVE STRENGTH | | | | | | |
| DIO drive strength | IDIO | | 2 | 12 | 12 | mA |
| FLASH SPECIFICATIONS | | | | | | |
| Endurance of the 384 kB of flash | | | 100,000 | – | – | write/erase cycles |
| Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total) | | | 1000 | – | – | write/erase cycles |
| Retention | | | 25 | – | – | years |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- The maximum VDDC voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
- The maximum VDDM voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
- The maximum VDDRF voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
- The VDDRF calibrated targets are:
 - 1.10 V (TX power > 0 dBm, with optimal RX sensitivity)
 - 1.07 V (TX power = 0 dBm)
 - 1.20 V (TX power = 2 dBm)
 The VDDPA calibrated targets are:
 - 1.30 V
 - 1.26 V (TX power = 3 dBm, assumes VDDRF = 1.10 V)
 - 1.60 V (TX power = 6 dBm, assumes VDDRF = 1.10 V)
- The LDO can be used to regulate down from VBAT and generate VCC. For VBAT values higher than 1.5 V, the LDO is less efficient and it is possible to save power by activating the DC–DC converter to generate VCC.
- Signal generated by RF tester.
- 0.5 to 1.0 dB degradation in the RX sensitivity is present on the QFN package vs WLCSP. This is attributed to the presence of the metal slug of the QFN package which is in close proximity to on–chip inductors.
- All values are based on evaluation board performance at the antenna connector, including the harmonic filter loss
- The values shown here are without RF filter. Harmonics need to be filtered with an external filter (See “RF Filter” on Table 6).
- These specifications have been validated with the Epson Toyocom MC – 306 crystal

Table 4. VDDM Target Trimming Voltage in Function of VDDO Voltage

| VDDM Voltage (V) | DIO_PAD_CFG DRIVE | Maximum VDDO Voltage (V) |
|------------------|-------------------|--------------------------|
| 1.05 | 1 | 2.7 |
| 1.05 | 0 | 3.2 |
| 1.10 | 0 | 3.3 |

NOTE: These are trimming targets at room/ATE temperature 25~30°C.

Table 5. VDDC Target Trimming Voltage in Function of SYSCLK Frequency

| VDDC Voltage (V) | Maximum SYSCLK Frequency (MHz) | Restriction |
|------------------|--------------------------------|---|
| 0.92 | ≤ 24 | The ADC will be functional in low frequency mode and between 0 and 85°C only. |
| 1.00 | ≤ 24 | Fully functional |
| 1.05 | 48 | Fully functional |

NOTE: These are trimming targets at room/ATE temperature 25~30°C.

RSL10

Table 6. RECOMMENDED EXTERNAL COMPONENTS:

| Components | Function | Recommended typical value | Tolerance |
|---------------------|------------------------------------|--|-----------|
| Cap (VBAT–VSSA) | VBAT decoupling | 4.7 μ F // 100 pF (Note 12) | \pm 20% |
| Cap (VDDO–VSSD) | VDDO decoupling | 1 μ F | \pm 20% |
| Cap (VDDRF–VSSRF) | VDDRF decoupling | 2.2 μ F | \pm 20% |
| Cap (VCC–VSSA) | VCC decoupling | Low ESR 2.2 μ F (Note 13) or 4.7 μ F | \pm 20% |
| Cap (VDDA–VSSA) | VDDA decoupling | 1 μ F | \pm 20% |
| Cap (CAP0–CAP1) | Pump capacitor for the charge pump | 1 μ F | \pm 20% |
| Inductor (DC–DC) | DC–DC converter inductance | Low ESR 2.2 μ H (See Table 7 below) | \pm 20% |
| Xtal_32 kHz | Xtal for 32 kHz oscillator | – MC – 306, Epson – CM8V–T1A, Micro Crystal Switzerland | |
| Xtal_48 MHz | Xtal for 48 MHz oscillator | 8Q–48.000MEEV–T, TXC Corporation, Taiwan | |
| RF filter (Note 14) | External harmonic filter | 1.5 pF / 3 nH / 1.5 pF / 1.8 nH | \pm 20% |

NOTE: All capacitors used must have good RF performance.

12. The recommended decoupling capacitance uses 2 capacitors with the values specified.

13. Example: AMK105BJ225_P, Taiyo Yuden.

14. For improved harmonic performance in environments where RSL10 is operating in close proximity to smartphones or base stations, FBAR filters such as the Broadcom ACPF–7924 can be applied instead of the suggested discrete harmonic filter.

Table 7. RECOMMENDED DC–DC CONVERTER INDUCTANCE TABLE

| Manufacturer | Part Number | Case Size | Comments |
|--------------|---------------|-------------------------------------|---|
| Taiyo Yuden | CKP2012N_2R2 | 0805 SMD with $T_{max} = 1.0$ mm | A degradation of 1 dB in the RX sensitivity is expected in DC–DC mode (Vbat = 3.3 V) versus LDO mode operation. |
| Taiyo Yuden | CBMF1608T2R2M | 0603 SMD with $T_{max} = 1.0$ mm | A degradation of <1 dB in RX sensitivity is expected in DC–DC mode (Vbat = 3.3 V) versus LDO mode operation. Also, the current drawn from the battery will be 4–10% higher than when the CKP2012N_2R2 is used depending on operation mode and settings. |

NOTE: Values have been measured on the QFN version of the RSL10 development board.

PCB Design Guidelines

1. Decoupling capacitors should be placed as close to the related balls as possible.
2. Differential output signals should be routed as symmetrically as possible.
3. Analog input signals should be shielded as well as possible.
4. Pay close attention to the parasitic coupling capacitors.
5. Special care should be made for PCB design in order to obtain good RF performance.
6. Multi–layer PCB should be used with a keep–out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance.
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip’s pin to the supply source.
8. Digital signals shouldn’t be routed close to the crystal or the power supply lines.
9. Proper DC–DC component placement and layout is critical to RX sensitivity performance in DC–DC mode.

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Table 8. BUMP AND COATING SPECIFICATIONS

| Subject | Specification |
|--------------------------------|----------------------|
| Bump metallization | Sn 97.7%/Ag 2.3% |
| Backside coating specification | Lintec Adwill LC2850 |
| Backside coating thickness | 25 μm |

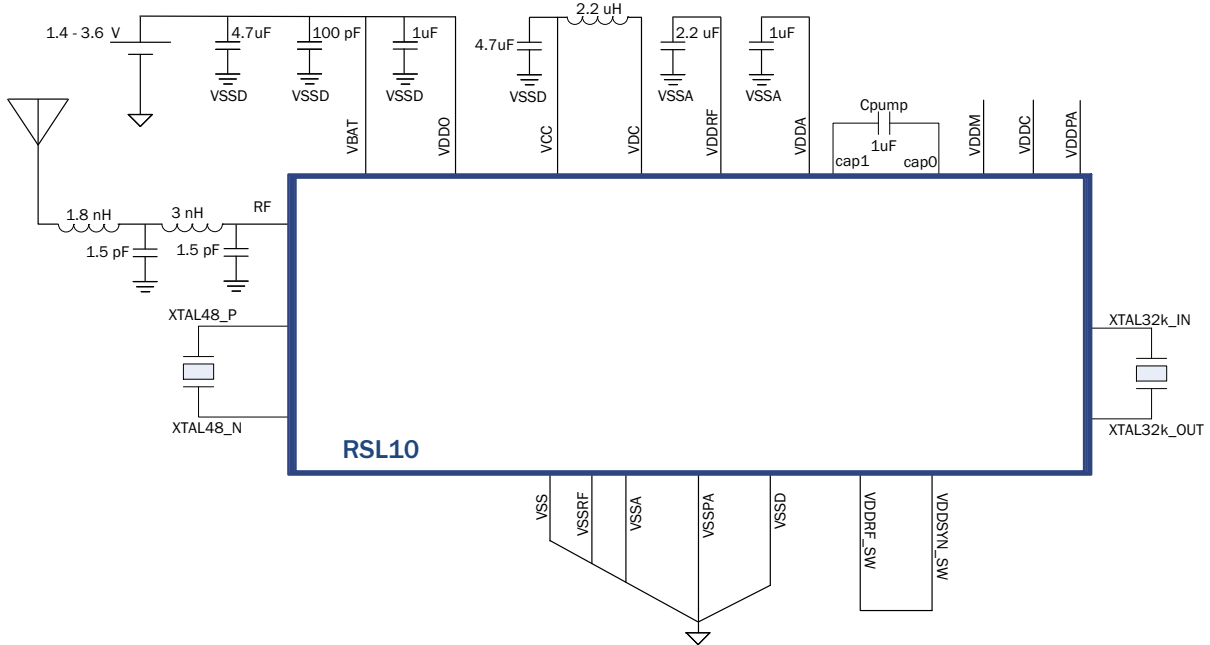
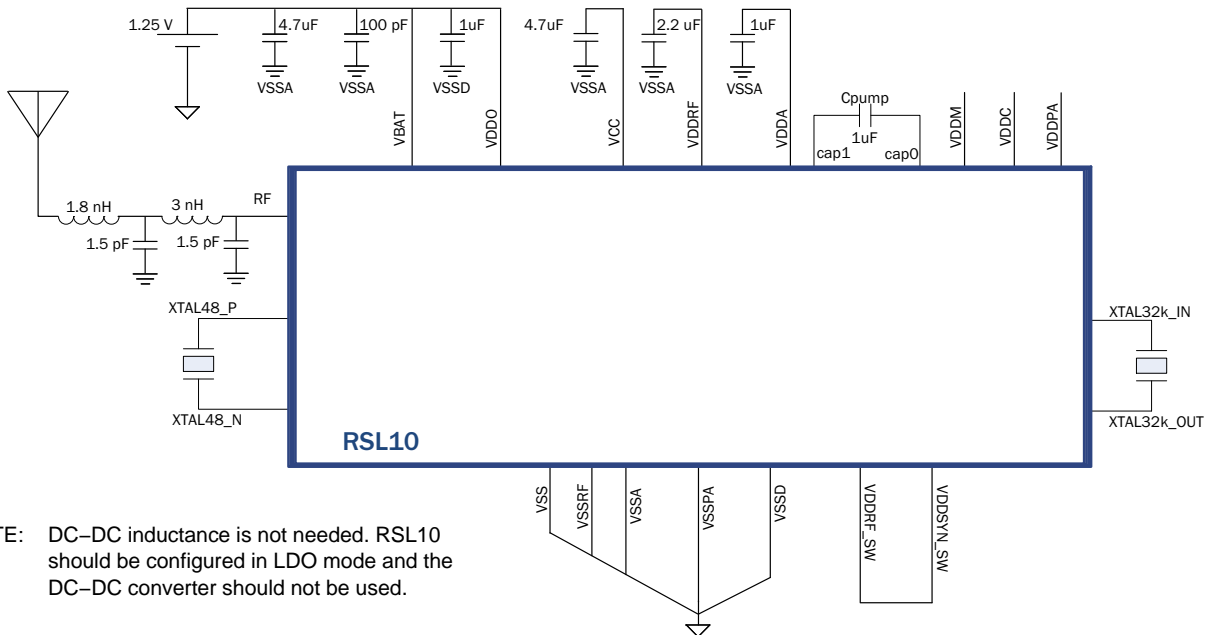


Figure 2. RSL10 Application Diagram in Buck Mode



NOTE: DC-DC inductance is not needed. RSL10 should be configured in LDO mode and the DC-DC converter should not be used.

Figure 3. RSL10 Application Diagram in LDO Mode

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Table 9. CHIP INTERFACE SPECIFICATIONS

| Pad Name | Description | Power Domain | I/O | A/D | Pull | Pad #, WLCSP | Pad #, QFN48 |
|------------|--|--------------|-----|-----|------|--------------|--------------|
| VBAT | Battery input voltage | VBAT | I | P | | K5,K7,K10 | 9 |
| VDC | DC-DC output voltage to external LC filter | | O | A | | J11 | 10 |
| VCC | DC-DC filtered output | | I | P/A | | K11 | 12 |
| XTAL32_IN | Xtal input pin for 32 kHz xtal | | I/O | A | | L10 | 14 |
| XTAL32_OUT | Xtal output pin for 32 kHz xtal | | I/O | A | | L11 | 13 |
| VSSA | Analog ground | | I/O | P | | E10 | 8 |
| RES | RESERVED | | I | D | D | F8 | 11 |
| VDDA | Charge pump output for analog and flash supplies | VDDA | I/O | P/A | | F11 | 5 |
| VDDRF | LDO's output for radio voltage supply | | I/O | P/A | | A11 | 48 |
| CAP0 | Pump capacitor connection | | O | A | | H11 | 7 |
| CAP1 | Pump capacitor connection | | O | A | | G10 | 6 |
| AOUT | Analog test pin | | O | A | | L6 | 4 |
| VDDRF_SW | Supply pin for the RF | VDDRF_SW | | P/A | | A9 | 47 |
| VDDSYN_SW | Supply pin for the radio synthesizer | | | P/A | | B8 | 45 |
| VSSRF | RF analog ground | | I/O | P | | B9 | 46 |
| XTAL48_N | Negative input for the 48 MHz xtal block | | I/O | A | | A6 | 43 |
| XTAL48_P | Positive input for the 48 MHz xtal block | | I/O | A | | A8 | 44 |
| VDDPA | Radio power amplifier voltage supply | VDDPA | I/O | P/A | | C11 | 2 |
| VSSPA | Radio power amplifier ground | | I/O | P | | D11 | 3 |
| RF | RF signal input/output (Antenna) | RF | I/O | A | | B11 | 1 |
| VPP | Flash high voltage access | VPP | I/O | A | | J6 | 17 |

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Table 9. CHIP INTERFACE SPECIFICATIONS (continued)

| Pad Name | Description | Power Domain | I/O | A/D | Pull | Pad #, WLCSP | Pad #, QFN48 |
|----------|---|--------------|-----|-----|------|--------------|--------------|
| NRESET | Reset pin | VDDO | I | D | U1 | L9 | 16 |
| WAKEUP | Wake-up pin for power modes | | I | A | | L8 | 15 |
| VDDC | LDO output for Core logic voltage supply | | I/O | P | | H6 | 19 |
| VDDM | LDO output for memories voltage supply | | I/O | P | | F4 | 21 |
| VDDO | Digital I/O voltage supply | | I | P | | B4 | 36 |
| VSSD | Digital ground pad for I/O | | I/O | P | | F3, D6, F9 | 28, 35 |
| VSS (*) | Substrate connection for the RF part | | I/O | P | | B6 | 42 |
| EXTCLK | External clock input | | I | D | U | F1 | 31 |
| DIO[0] | Digital input output / ADC 0 | | I/O | A/D | U/D | L4 | 18 |
| DIO[1] | Digital input output / ADC 1 | | I/O | A/D | U/D | L3 | 20 |
| DIO[2] | Digital input output / ADC 2 | | I/O | A/D | U/D | L2 | 23 |
| DIO[3] | Digital input output / ADC 3 | | I/O | A/D | U/D | L1 | 25 |
| DIO[4] | Digital input output 4 | | I/O | D | U/D | K2 | 24 |
| DIO[5] | Digital input output 5 | | I/O | D | U/D | K1 | 27 |
| DIO[6] | Digital input output 6 | | I/O | D | U/D | J1 | 29 |
| DIO[7] | Digital input output 7 | | I/O | D | U/D | H1 | 30 |
| DIO[8] | Digital input output 8 | | I/O | D | U/D | G2 | 26 |
| DIO[9] | Digital input output 9 | | I/O | D | U/D | E2 | 22 |
| DIO[10] | Digital input output 10 | | I/O | D | U/D | D1 | 32 |
| DIO[11] | Digital input output 11 | | I/O | D | U/D | B2 | 38 |
| DIO[12] | Digital input output 12 | | I/O | D | U/D | A1 | 37 |
| DIO[13] | Digital input output / CM3-JTAG Test Reset | | I/O | D | U/D | A2 | 39 |
| DIO[14] | Digital input output / CM3-JTAG Test Data In | | I/O | D | U/D | A3 | 41 |
| DIO[15] | Digital input output / CM3-JTAG Test Data Out | | I/O | D | U/D | A4 | 40 |
| JTCK | CM3-JTAG Test Clock | | I/O | D | U | C1 | 33 |
| JTMS | CM3-JTAG Test Mode State | | I/O | D | U | B1 | 34 |

*VSS should be connected to VSSRF at the PCB level.

NOTE: It is recommended that the QFN package metal slug be left open/floating for optimal Rx sensitivity performance

Legend:

Type: A = analog; D = digital; I = input; O = output; P = power

Pull: U = pull up; D = pull down

Pull up: selectable between 10 kΩ and 250 kΩ. U1 = pull up, 200 kΩ.

Pull down: 250 kΩ

All digital pads have a Schmitt trigger input.

All DIO pads have a programmable I²C low pass filter. All DIOs can be configured to no pull.

RSL10

ARCHITECTURE OVERVIEW

The architecture of the RSL10 chip is shown in Figure 4.

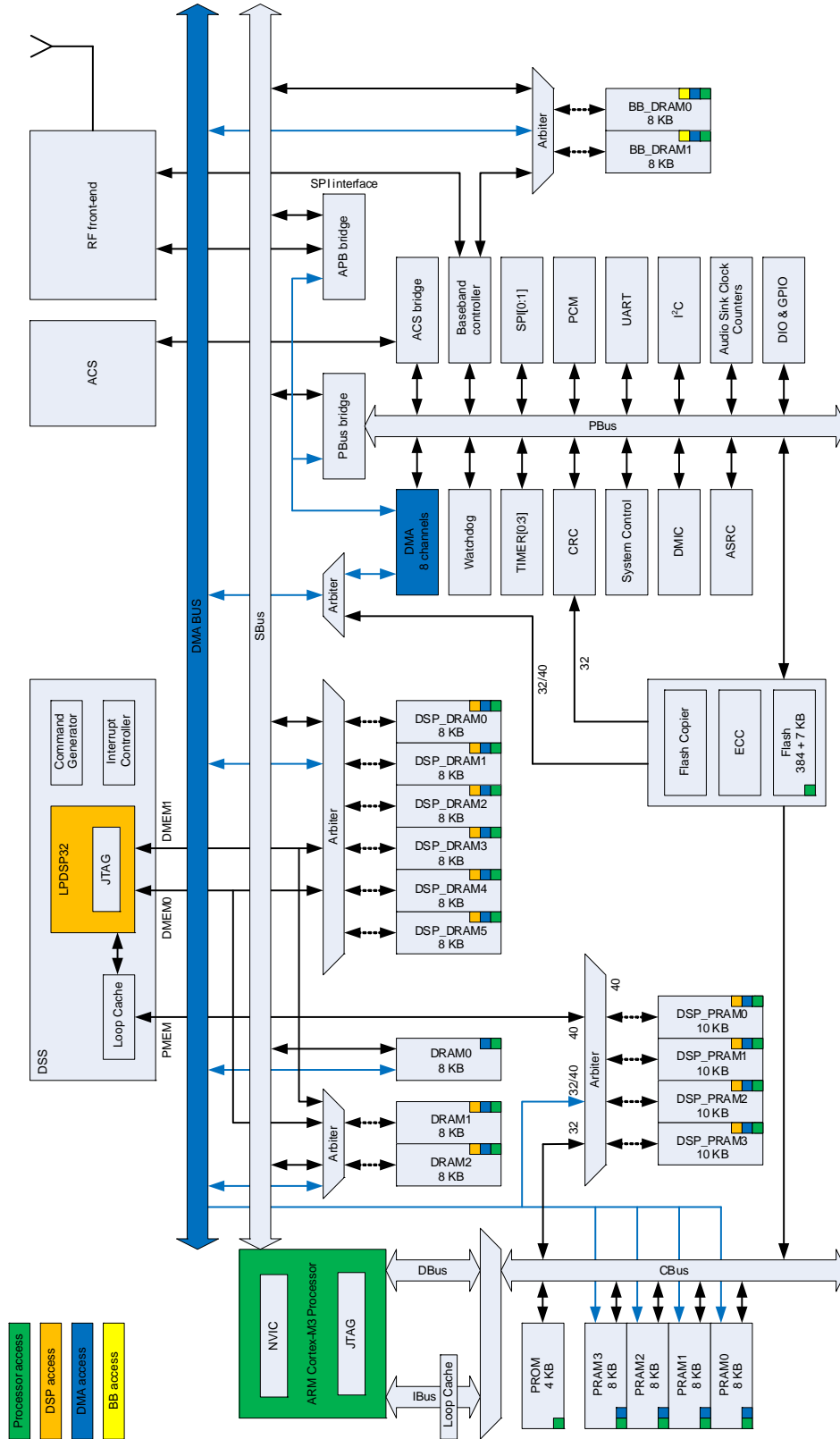


Figure 4. RSL10 Architecture

Power Management Unit

The RSL10 power management unit prevents system brown-outs in case the battery voltage dips below the specified minimum voltage required for reliable operation. It does this by:

1. Monitoring the power supply and safely shutting down the system if needed.
2. Preventing possible damage to RSL10 when the battery is inserted or removed.
3. Allowing operation across wide temperature and voltage ranges at low power consumption.

RSL10 allows the use of either the DC-DC converter for a better efficiency when the battery voltage is higher than 1.4 V or the internal LDO when VBAT is lower than 1.4 V. The output of the DC-DC converter or the LDO regulator is used to supply other voltage regulator blocks of RSL10. These blocks are:

- A programmable voltage regulator to supply the digital cores (VDDC)
- A programmable voltage regulator to supply the memories (VDDM)
- A charge pump supplying the analog blocks and the flash memory (VDDA)
- A programmable voltage regulator to supply the radio front-end (VDDRF)
- A programmable voltage regulator to supply the power amplifier of the radio (VDDPA): This regulator is used only for the +6 dBm output power case or if we want to transmit at +3 dBm output power with a battery level less than 1.4 V. The VDDPA regulator can be disabled if RSL10 doesn't have to transmit at high power, and VDDRF only should be used.

Clock and Clocking Options

RSL10's system clock (SYSCLK) can come from various sources:

- A 48 MHz crystal oscillator, used in normal operation mode
- An internal trimmable RC oscillator that supplies a 3 MHz – 12 MHz clock used at system startup
- A Real Time Clock, used in stand-by mode, generated from one of:
 - ◆ A 32 kHz RC oscillator
 - ◆ A 32 kHz crystal oscillator
 - ◆ An external input on one of DIO0 to DIO3
- A JTAG clock, used in debug mode, coming from the JTCK pad
- An external clock source, coming from the EXTCLK pad

Every clock generated in the system can be disabled when they are not needed. Also, every clock has an associated configurable prescaler to minimize the power dissipated on the clock tree.

A clock detector unit can be used to monitor the system clock and/or the RTC clock in sleep and standby modes. In the event the clock frequency goes below a certain threshold, the RSL10 IC will be reset. The clock detector threshold is nominally 2 kHz. This block and the reset it triggers is enabled by default, but both can be disabled.

Radio Front-End

RSL10 2.4 GHz radio front-end implements the physical layer for the Bluetooth low energy technology standard and other standard, proprietary, and custom protocols. It operates in the worldwide deployable 2.4 GHz ISM band (2.4000 to 2.4835 GHz) and supports:

- Bluetooth 5 certified with LE 2M PHY support
- ON Semiconductor's custom audio protocol and other custom protocols

The RSL10 Radio Front End includes the necessary hardware to support the following protocols:

- The IEEE 802.15.4 standard, used as the physical layer for many standard and proprietary protocols including ZigBee and Thread
- Proprietary protocols or proprietary audio protocols

The 2.4 GHz radio front-end is based on a low-IF architecture and comprises the following building blocks:

- High performance single-ended RF port
- On-chip matching network with 50 ohm RF input
- High gain, low power LNA (low noise amplifier), and mixer
- PA (Power Amplifier) with +3 dBm output power for Bluetooth and 802.15.4 OQPSK applications, and up to +6 dBm with dedicated PA voltage supply
- ADC converter
- RSSI (Received Signal Strength Indication) with 60 dB nominal range with 2.4 dB steps (not considering AGC)
- Fully integrated ultra-low power frequency synthesis with fast settling time, with direct digital modulation in transmission (pulse shape programmable)
- 48 MHz XTAL reference (finely trimmable)
- Fully-integrated FSK-based modem with programmable pulse shape, data rate, and modulation index
- Digital baseband (DBB) with Link layer functionalities, including automatic packet handling with preamble & sync, CRC, and separate Rx and Tx 128-bytes FIFOs
- Serial and parallel digital interfaces

The 2.4 GHz radio front-end contains a full transceiver with the following features:

- IEEE 802.15.4 chip encoding & decoding
- Manchester encoding
- Data whitening

The 2.4 GHz radio front-end contains also a highly-flexible digital baseband—in terms of modulations, configurability and programmability – in order to support Bluetooth low energy technology, 802.15.4 OQPSK and DSSS, and proprietary protocols. It allows for programmable data rates from 62.5 kbps up to 2 Mbps, FSK with programmable pulse shape and modulation index.

The 2.4 GHz radio front-end also include IEEE 802.15.4 chip encoding & decoding, Manchester encoding and Data whitening. Its packet handling includes:

- Automatic preamble and sync word insertion
- Automatic packet length handler
- Basic address check
- Automatic CRC calculation and verification with a programmable CRC polynomial
- Multi-frame support
- 2x128 byte FIFOs

Baseband Controller and Software Stack

The RSL10 Bluetooth baseband controller is connected to the radio front-end. It configures the physical layer of the RSL10 for use as a Bluetooth low energy technology device. It provides access and support for the Direct-Test Mode (DTM) layer for RF testing, and it implements portions of the link layer and other controller level components from the Bluetooth stack. It is dedicated to low level bitwise operations and data packet processing.

RSL10 is Bluetooth 5 certified and includes LE 2 Mbps support and all optional features from earlier versions of Bluetooth low energy technology.

The RSL10 device also supports custom software stacks for:

- Custom audio protocol to support low-latency audio streaming
- Custom audio protocol to support low-power audio streaming from a remote dongle

Also, the coexistence between Bluetooth and a custom protocol is supported. For example, when streaming audio from a remote dongle, it is possible to also use the phone to control the audio device using the standard Bluetooth low energy technology protocol.

The software stack, including the profiles and the application, handles the protocol functions and is executed on the Arm Cortex-M3 processor. The Bluetooth IP implementation is split among software and hardware as shown in Figure 5.

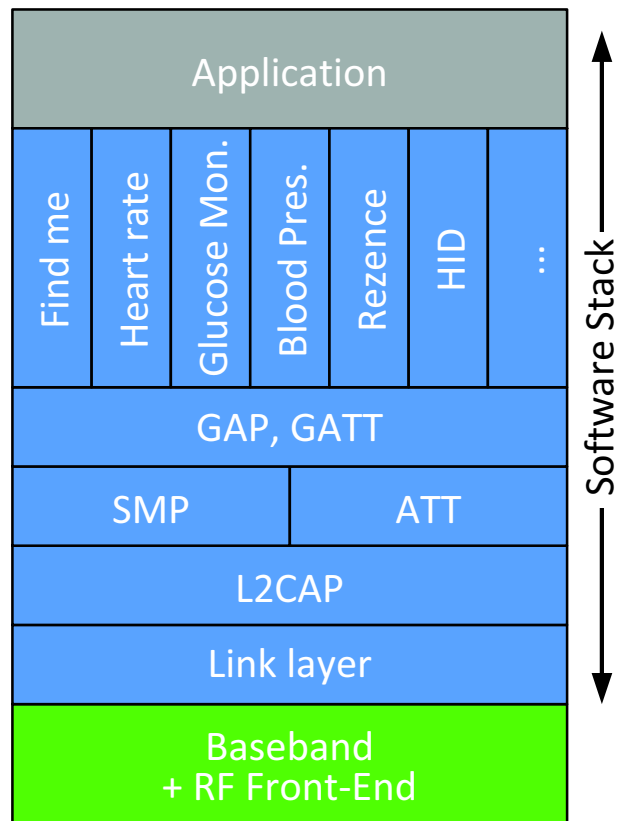


Figure 5. Bluetooth Protocol Implementation

The following is a sample of the Bluetooth low energy profiles supported by RSL10. For more information and a complete list of the profiles offered, please download the RSL10 development tools kit.

- Find Me
- Proximity
- Health Thermometer
- Heart Rate
- Time
- Blood Pressure
- Glucose Monitor
- HID over GATT (HOG)
- Alert Notification
- Phone Alert Status
- Running Speed
- Cycling Speed
- Cycling Power
- Location and Navigation
- Rezenze (custom protocol defined by AirFuel™ Alliance to support wireless battery charging)

Arm Cortex–M3 Processor Subsystem

The Arm Cortex–M3 processor subsystem includes the Arm Cortex–M3 processor, which is the master processor of the RSL10 chip. It also contains the Bluetooth baseband controller, and all interfaces and other peripherals.

Arm Cortex–M3 Processor

The Arm Cortex–M3 processor is a state-of-the-art 32-bit core with embedded multiplier and ALU for handling typical control functions. Software development is done in C.

It features a low gate count, low interrupt latency, and low-cost debug functionality. It is primarily intended for deeply embedded applications that require low power consumption with fast interrupt response. The processor implements the Arm architecture v7–M. For power management, the processor can be placed under firmware control, into a Standby mode, in which the processor clock is disabled. The Nested Vectored Interrupt Controller (NVIC) will continue to run to enable exiting Standby mode on an interrupt.

LPDSP32

LPDSP32 is a C-programmable, 32-bit DSP developed by ON Semiconductor. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32-bit) and double precision (64-bit) arithmetic.

LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks. The advanced architecture also provides:

- Two 72-bit ALUs capable of doing single and double precision arithmetic and logical operations
- Two 32-bit integer/fractional multipliers
- Four 64-bit accumulators with 8-bit overflow (extension bits)

LPDSP32 can typically support the audio codecs needed to deploy audio device communication use cases. This includes (but is not limited to) codecs to support:

- A 16 kHz sample rate, producing a signal with a 7 kHz bandwidth (E.g.; G.722 and mSBC codec)
- A 24 kHz sample rate, producing a signal with an 11 kHz bandwidth (E.g.: G.722, CELT codec from the OPUS standard)

Communications to the Arm Cortex–M3 processor are completed via interrupts and shared memories. Software development is done in C, and the development tools are provided upon request from Synopsys.

Interfaces

RSL10 includes:

- Two independent SPI interfaces that can be configured in master and slave mode
- A fully configurable PCM interface
- A standard general purpose I²C interface

- A standard general purpose UART interface
- Two PWM (Pulse Width Modulation) drivers that can generate a single bit output signal at a given frequency
- A two-channel digital microphone (DMIC) input
- An output driver (OD) to allow direct connection to high impedance speakers
- SWJ–DP interface for the Arm Cortex–M3 processor
- JTAG interface for LPDSP32

RSL10 includes 16 DIO pads (Digital Input/Output) that all can be assigned to any of the interfaces above, or used as general purpose DIOs.

Peripherals

RSL10 includes:

- Four general purpose timers
- A DMA (Direct Memory Access) controller to transfer data between peripherals and memories without any core intervention
- A flash copier to initialize SRAM memories and that can be used with the CRC blocks to validate flash memory contents
- An Analog to Digital converter (ADC), accessed by the Arm Cortex–M3 processor. The ADC can read 4 external values (DIO[0]–DIO[3]), AOUT, VDDC, VBAT/2 and the ADC offset value.
- Two standard Cyclic Redundancy Code (CRC) blocks to ensure data integrity of the user application code and data
- An Asynchronous Sample Rate Converter (ASRC) and Audio Sink Clock Counters blocks to provide a means of synchronizing the audio sample rate between the radio link and the host device
- A Watchdog timer to detect and recover from RSL10 malfunctions.
- Four autonomous 32-bit Activity Counters. These counters help analyze how long the system has been running and how much the Arm Cortex–M3 processor, LPDSP32, and the flash memory have been used by the application. This is useful information to estimate and optimize the power consumption of the application.
- An IP protection system to ensure that the flash content cannot be copied by a third party. It can be used to prevent any core or memory of the RSL10 from being accessed externally after the RSL10 has booted.
- Program memory loop caches for each processor to reduce the RSL10 power consumption. This reduces the number of flash and RAM memory accesses by caching the program words that are read in these loops.

RSL10 Memory Structure

Table 10 lists the memory structures attached to RSL10, and the size and width of each memory structure.

RSL10

Table 10. RSL10 MEMORY STRUCTURES

| Memory type | Data Width | Memory Size | Accessed by |
|----------------------|------------|----------------------|--|
| Program memory (ROM) | 32 | 4 kB | Arm Cortex–M3 processor |
| Program memory (RAM) | 32 | 4 instances of 8 kB | Arm Cortex–M3 processor |
| Program memory (RAM) | 40 | 4 instances of 10 kB | LPDSP32 / Arm Cortex–M3 processor |
| Data memory (RAM) | 32 | 1 instances of 8 kB | Arm Cortex–M3 processor |
| Data memory (RAM) | 32 | 2 instances of 8 kB | Arm Cortex–M3 processor / LPDSP32 |
| Data memory (RAM) | 32 | 6 instances of 8 kB | LPDSP32 / Arm Cortex–M3 processor |
| Data memory (RAM) | 32 | 2 instances of 8 kB | Baseband / Arm Cortex–M3 processor |
| Flash | 32 | 384 kB | Arm Cortex–M3 processor / Flash copier |

Chip Identification

System identification is used to identify different system components. For the RSL10 chip, the key identifier components and values are as follows:

- Chip Family: 0x09
- Chip Version: 0x01
- Chip Revision: 0x01

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high–energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Solder Information

The RSL10 QFN package is constructed with all RoHS compliant material and should be reflowed accordingly.

This device is Moisture Sensitive Class MSL3 and must be stored and handled accordingly. Re–flow according to IPC/JEDEC standard J–STD–020C, Joint Industry

Standard: Re–flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For more information, see SOLDERRM/D available from <http://onsemi.com>.

Development Tools

RSL10 is supported by a full suite of comprehensive tools including:

- An easy–to–use development board
- Software Development Kit (SDK) including an Oxygen Eclipse–based development environment, Bluetooth protocol stacks, sample code, libraries, and documentation

Company or Product Inquiries

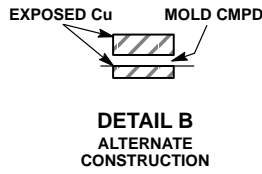
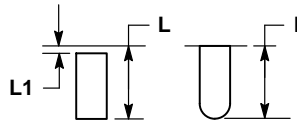
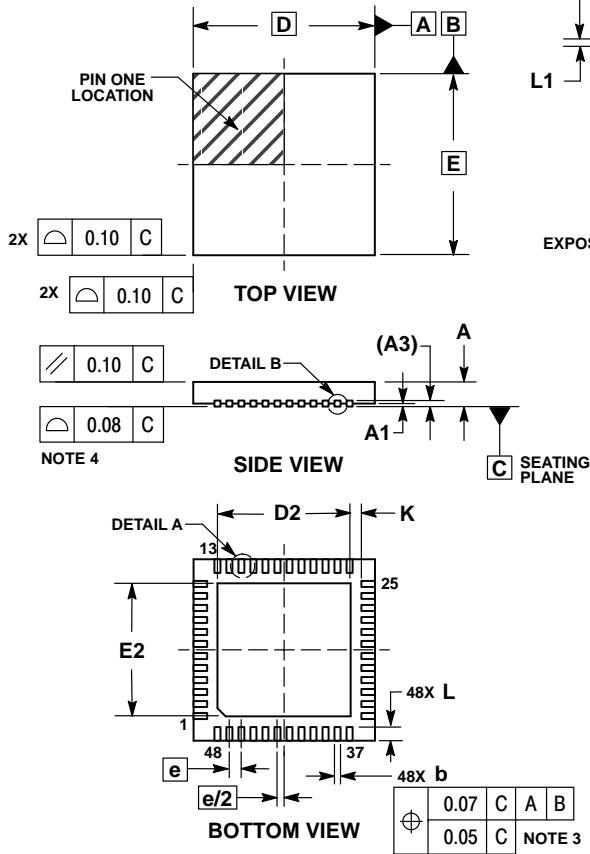
For more information about ON Semiconductor products or services visit our Web site at <http://onsemi.com>.

For sales or technical support, contact your local representative or authorized distributor.

RSL10

PACKAGE DIMENSIONS

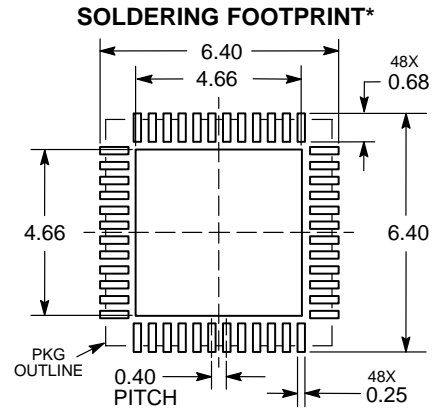
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CASE 485BA
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 6.00 BSC | |
| D2 | 4.40 | 4.60 |
| E | 6.00 BSC | |
| E2 | 4.40 | 4.60 |
| e | 0.40 BSC | |
| K | 0.20 MIN | |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

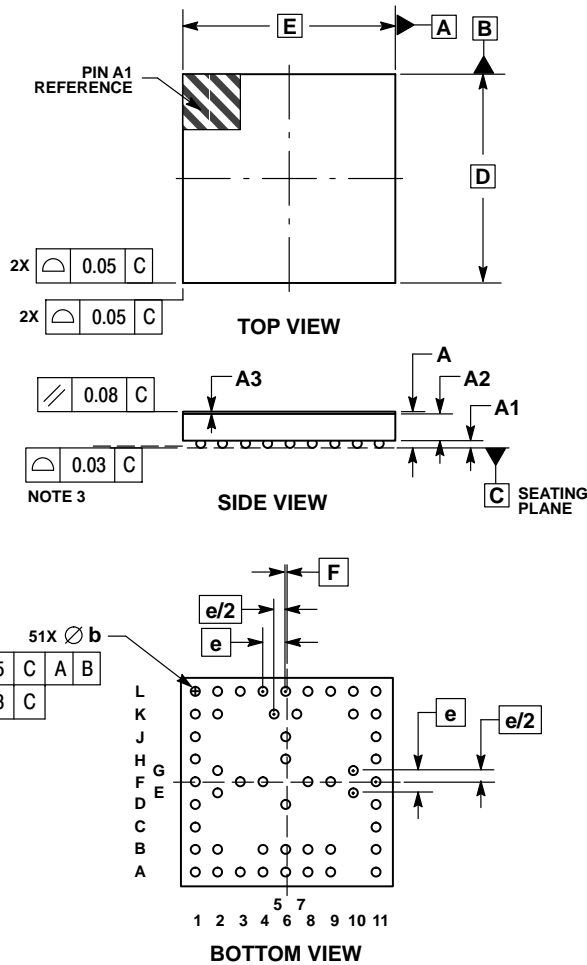


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

RSL10

PACKAGE DIMENSIONS

WLCSP51, 2.364x2.325
CASE 567MT
ISSUE A

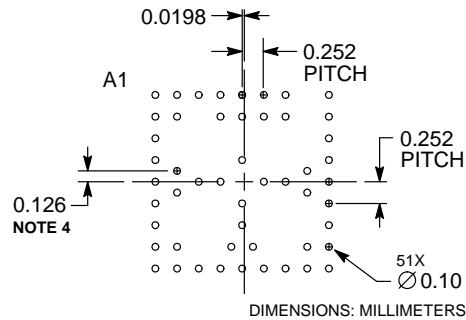


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. PACKAGE CENTER AND FOOTPRINT CENTER ARE NOT COINCIDENT. REFER TO DIMENSION F FOR OFFSETS.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN | NOM | MAX |
| A | 0.319 | 0.350 | 0.381 |
| A1 | 0.060 | 0.075 | 0.090 |
| A2 | 0.237 | 0.250 | 0.263 |
| A3 | 0.022 | 0.025 | 0.028 |
| b | 0.09 | 0.10 | 0.12 |
| D | 2.325 BSC | | |
| E | 2.364 BSC | | |
| e | 0.252 BSC | | |
| F | 0.0198 BSC | | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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