TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

TC511002P/J/Z-85, TC511002P/J/Z-10
TC511002P/J/Z-12

DESCRIPTION

The TC511002P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

FEATURES

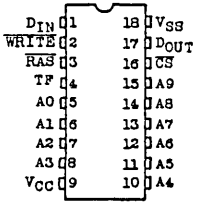
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511002P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

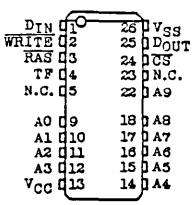
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  385mW MAX. Operating (TC511002P/J/Z-85)
  330mW MAX. Operating (TC511002P/J/Z-10)
  275mW MAX. Operating (TC511002P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability.
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511002P
  Plastic SOJ: TC511002J
  Plastic ZIP: TC511002Z

PIN CONNECTION (TOP VIEW)

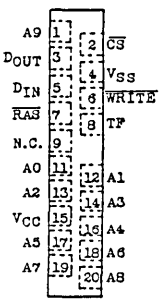
Plastic DIP



Plastic SOJ



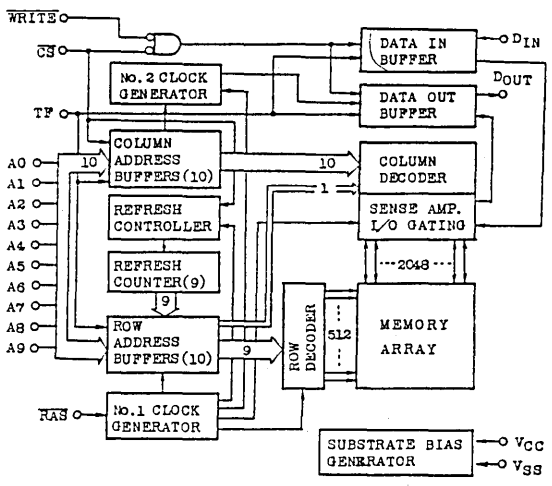
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511002P/J/Z-85	-	70	mA	3,4
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC}, MIN.)	TC511002P/J/Z-85	-	70	mA	3
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC511002P/J/Z-85	-	50	mA	3,4
		TC511002P/J/Z-10	-	40	mA	
		TC511002P/J/Z-12	-	30	mA	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511002P/J/Z-85	-	70	mA	3
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V≦V_{IH}≦6.5V, All Other Pins Not Under Test = 0V)		-10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V≦$V_{IN(TF)}$≦0.8V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦+5.5V)		-10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RWC}	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{SRWC}	Static Column Mode Read Write Cycle Time	90	-	100	-	120	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{ALW}	Access Time from Last Write	-	85	-	95	-	115	ns	8,15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{LWAD}	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	15
t_{AHLW}	Last Write to Column Address Hold Time	85	-	95	-	115	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	25	-	25	-	30	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	85	-	100	-	120	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEH}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

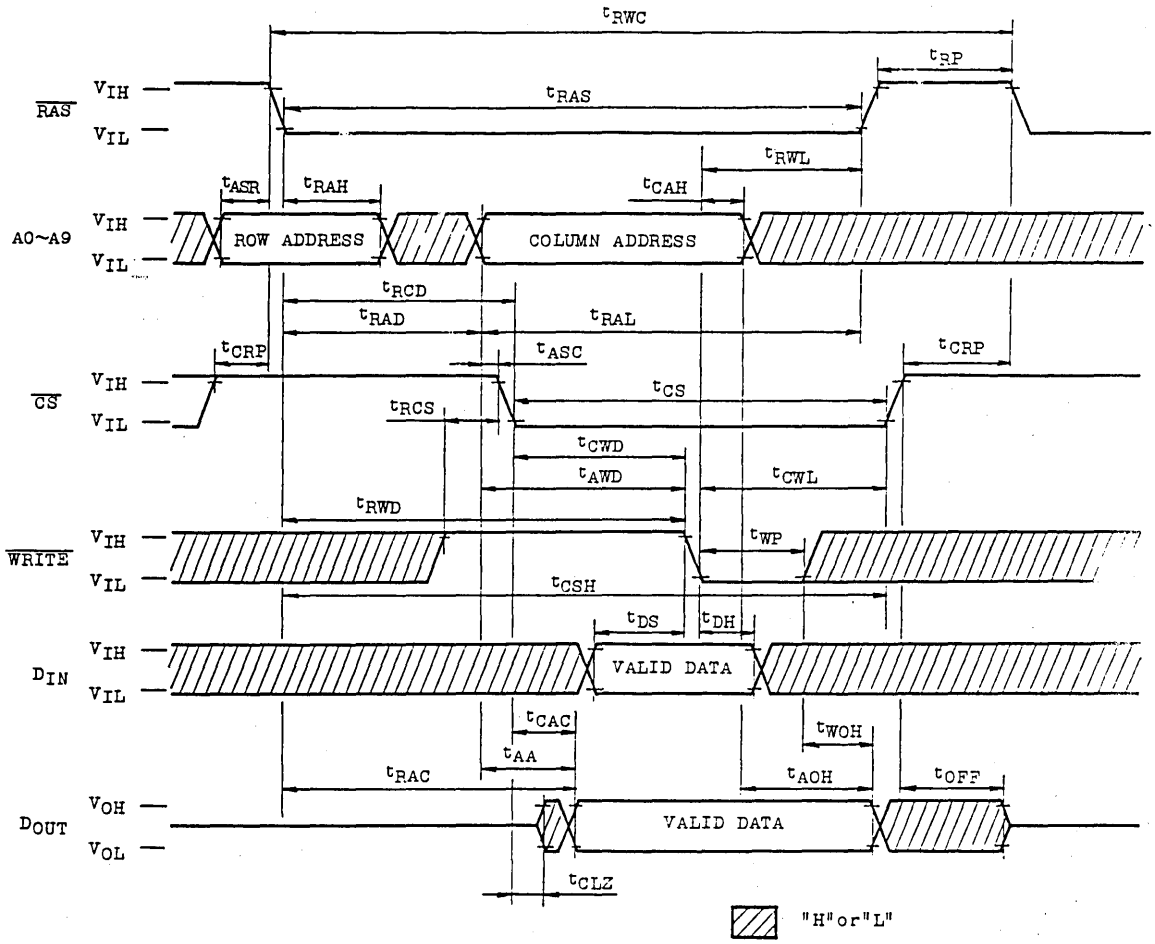
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
   In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ intialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electeical characteristics only. If $t_{WS} \geq t_{WS}$(min.) and $t_{WH} \geq t_{WH}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specilied t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD} (max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

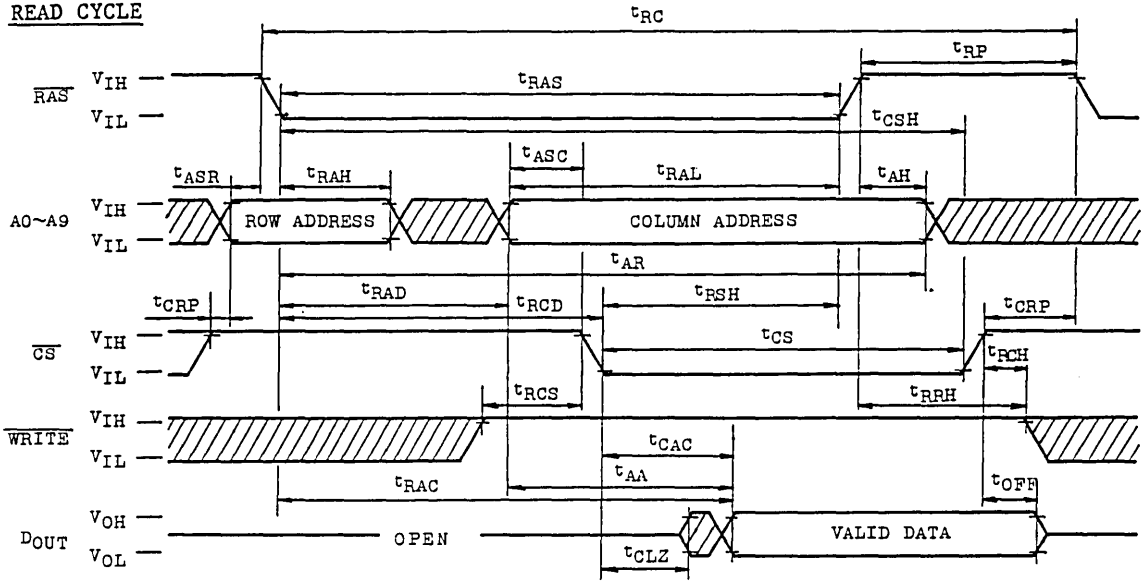
READ-WRITE CYCLE



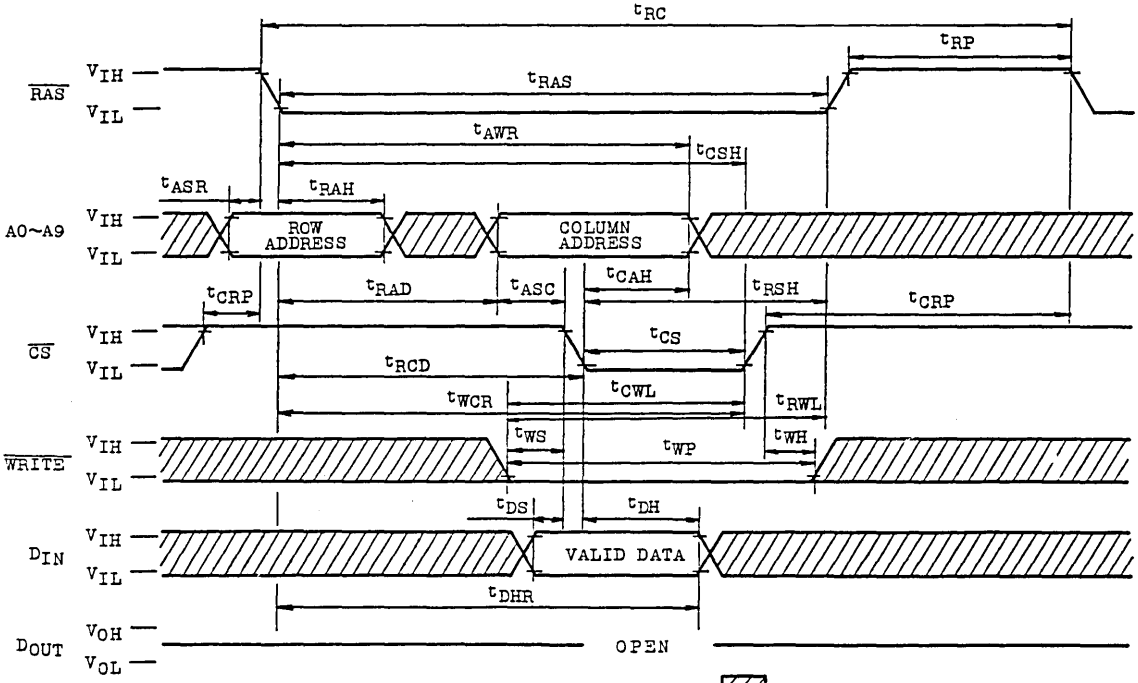
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

TIMING WAVEFORMS

READ CYCLE

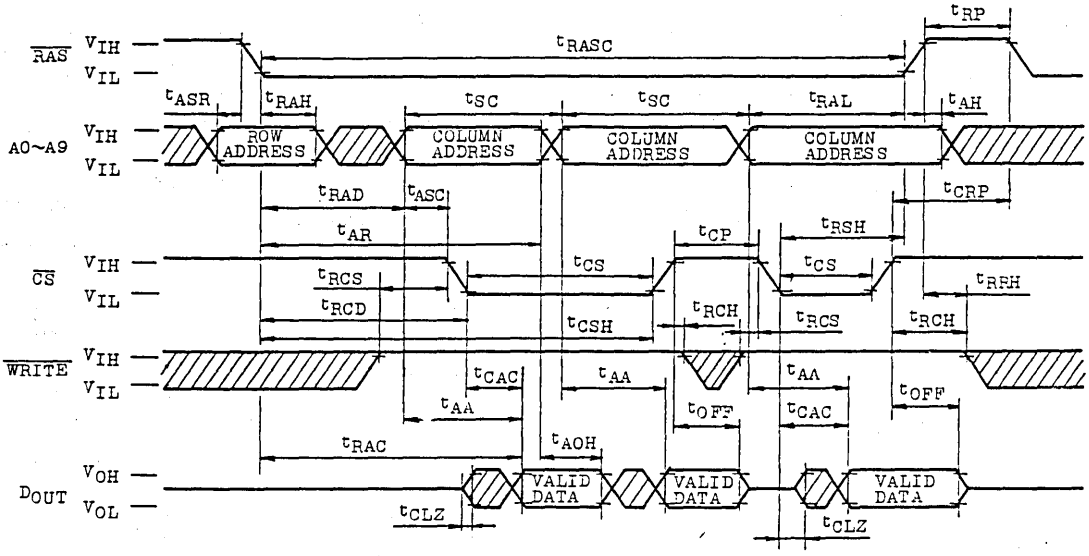


WRITE CYCLE (EARLY WRITE)

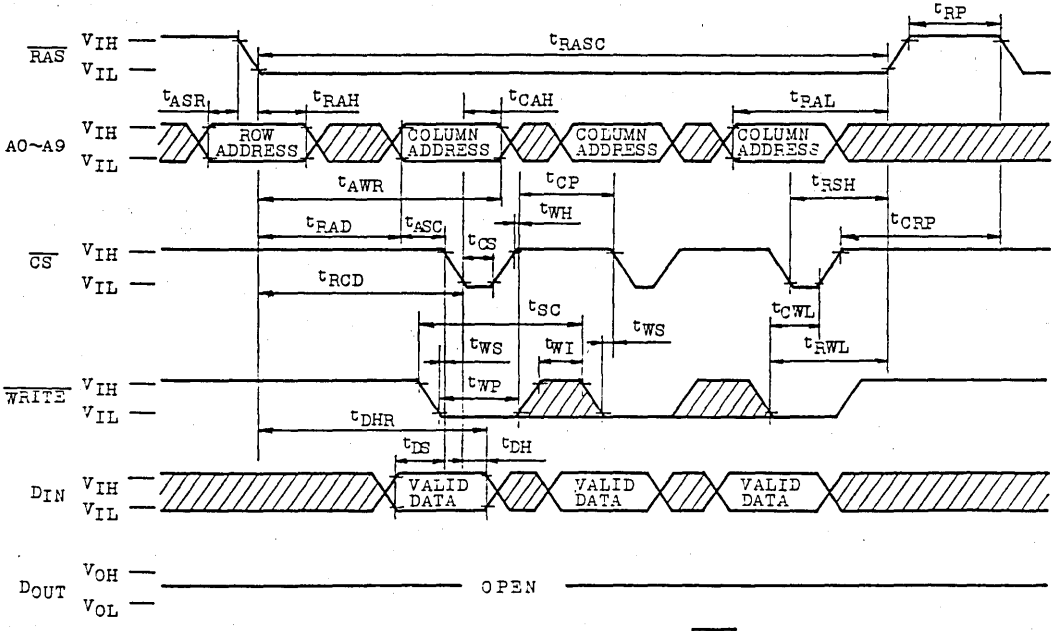


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ CYCLE

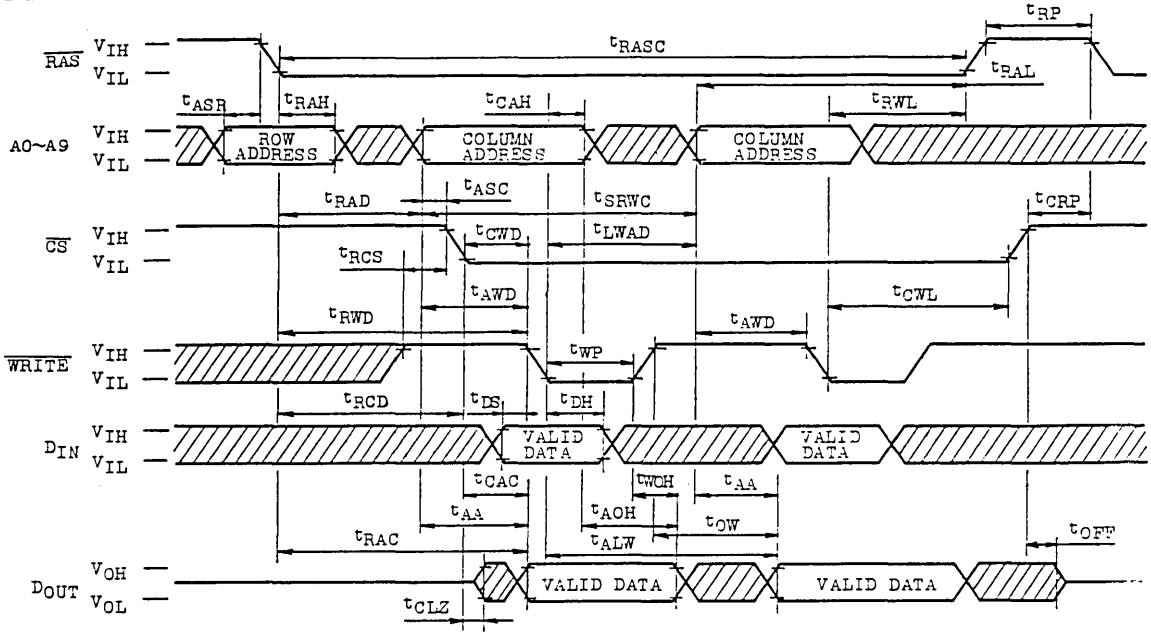


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

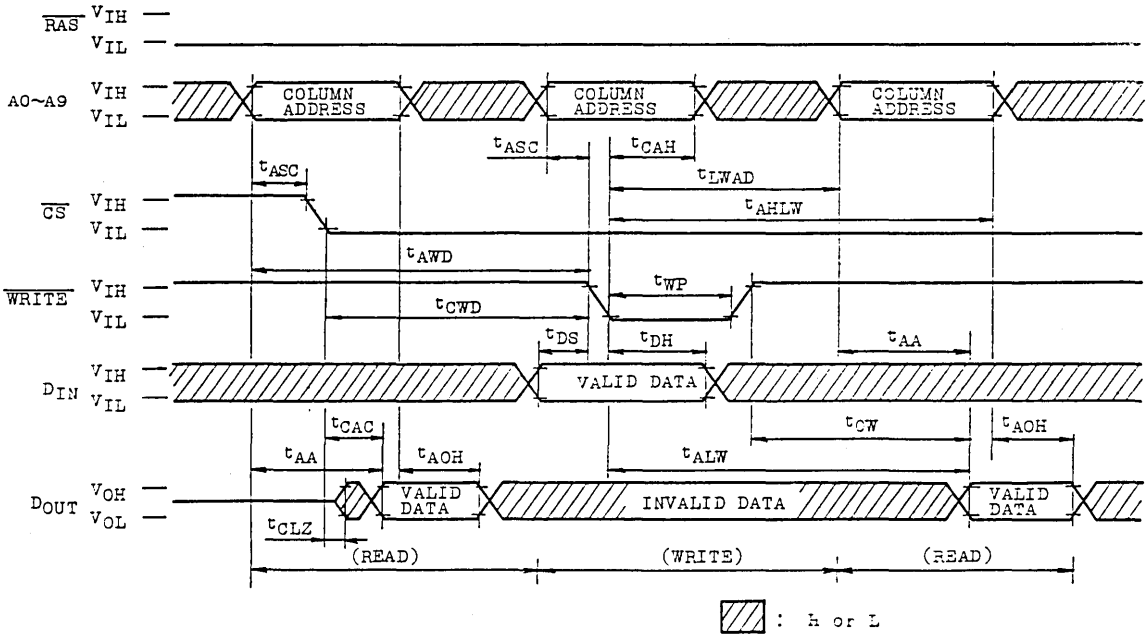


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ-WRITE CYCLE

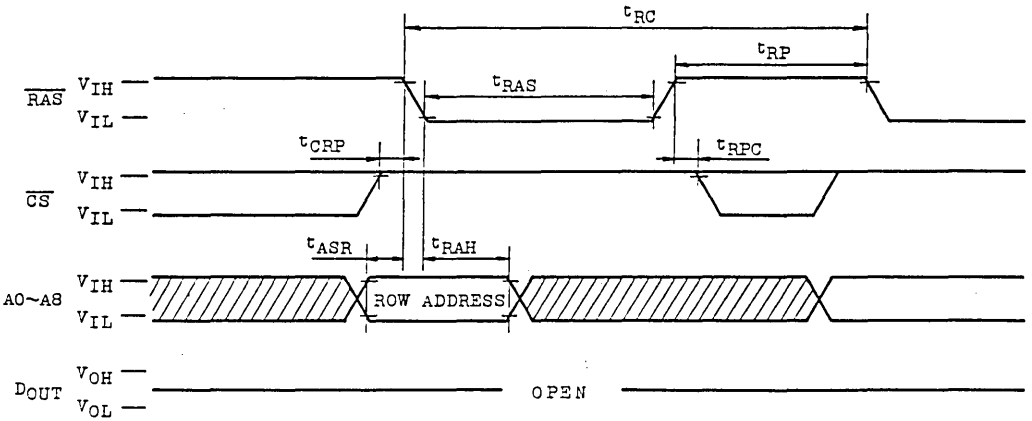


STATIC COLUMN MODE READ/WRITE MIXED CYCLE



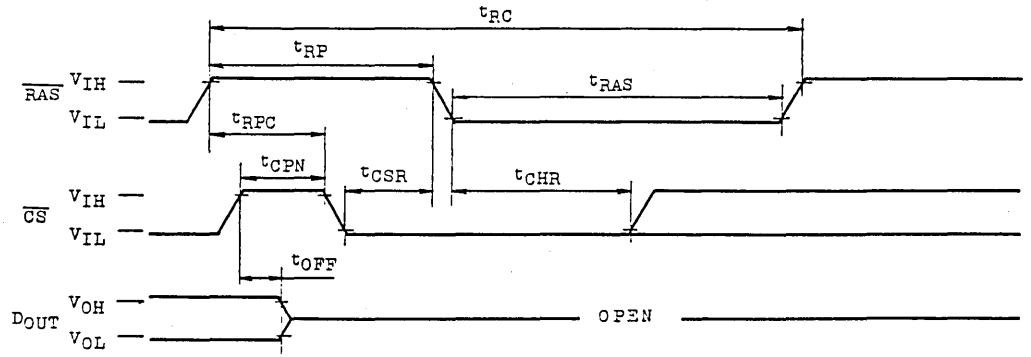
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H"or"L"

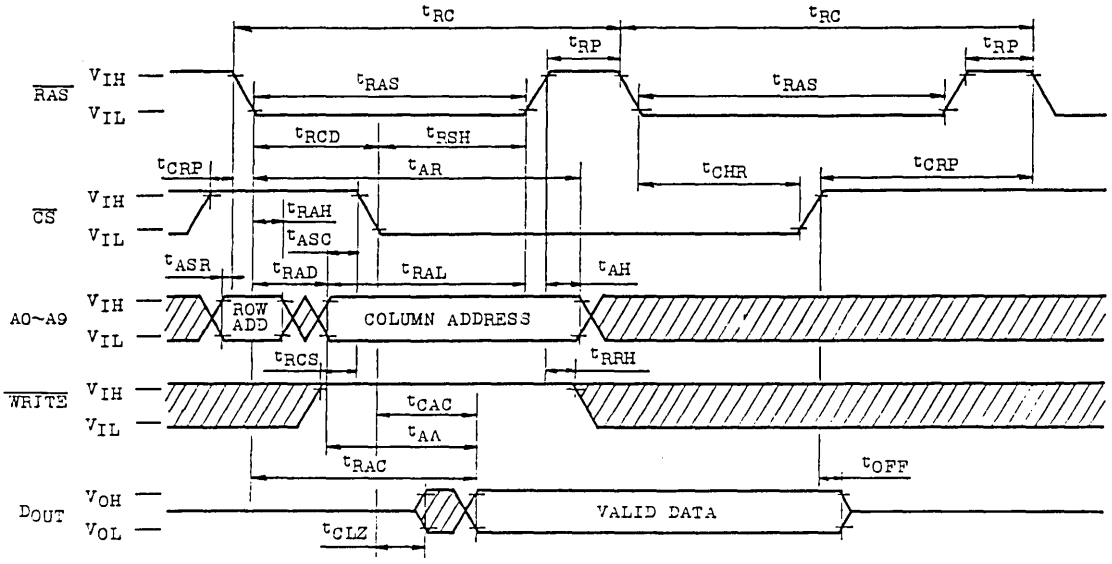
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



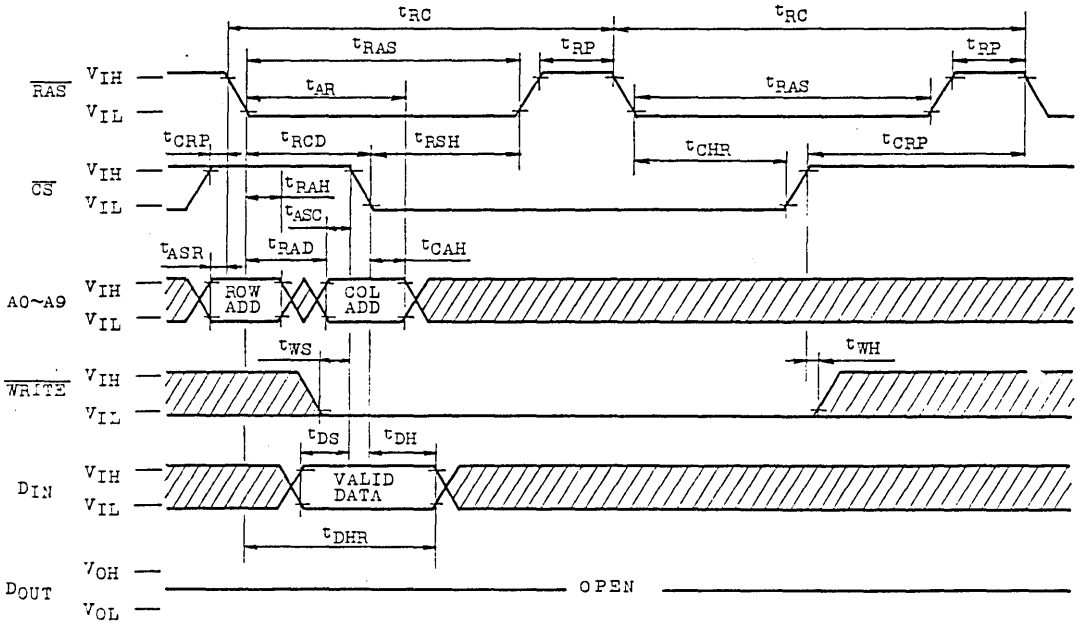
NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

"TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)

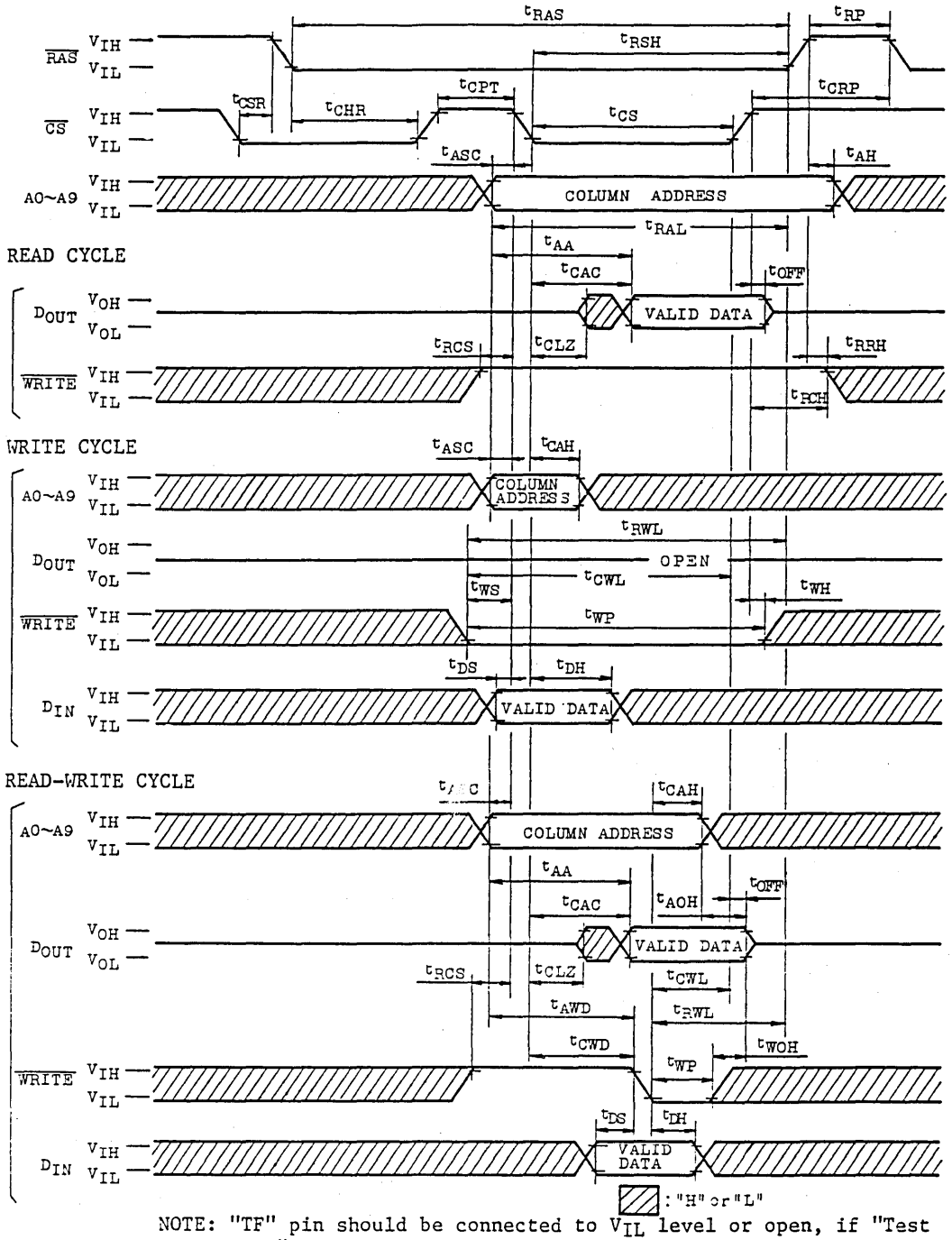


HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

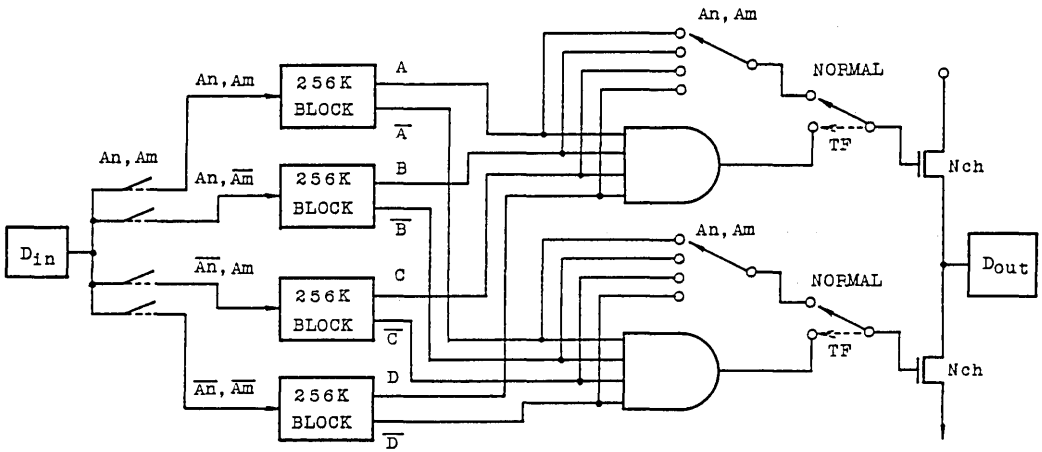
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode

TF Pin = Low level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES and tTEH as shown in figure 2). It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode"

During normal operation or when the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

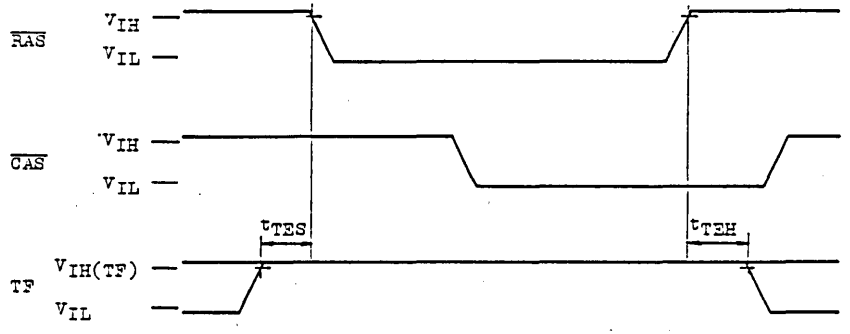
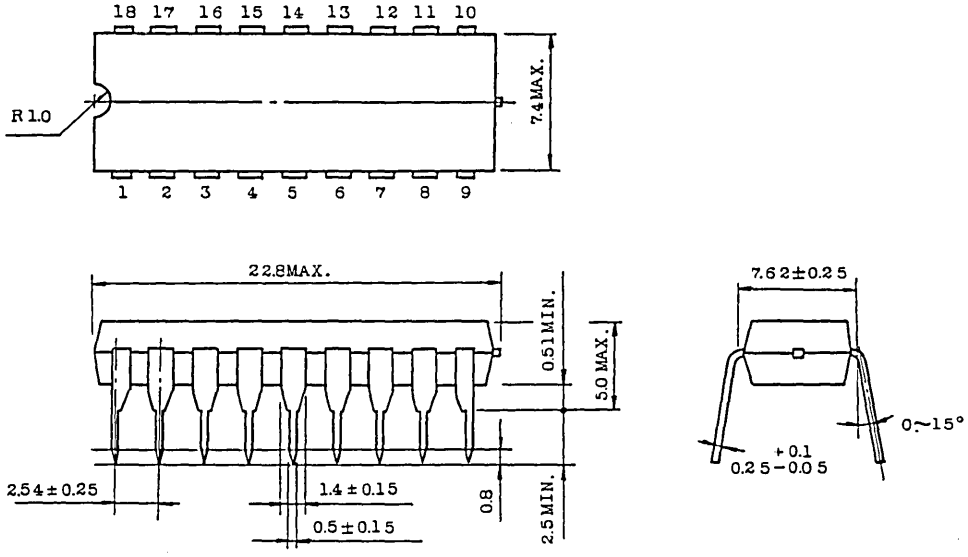


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

Plastic DIP

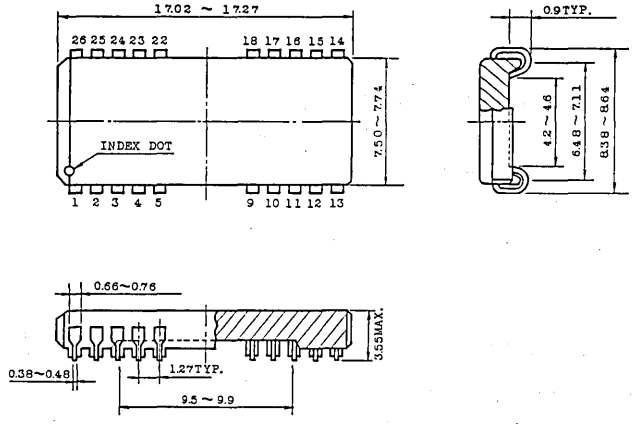
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads. All dimensions are in millimeters.

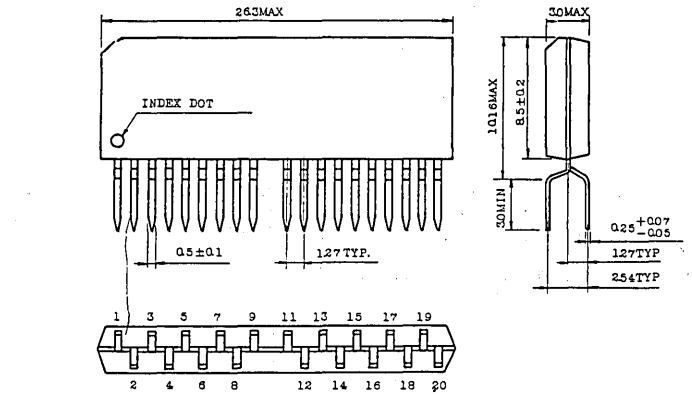
Plastic SOJ

Unit in mm



Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.