M74HC123P/FP/DP

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74HC123 is a semiconductor integrated circuit consisting of two retriggerable monostable multivibrators with direct reset inputs.

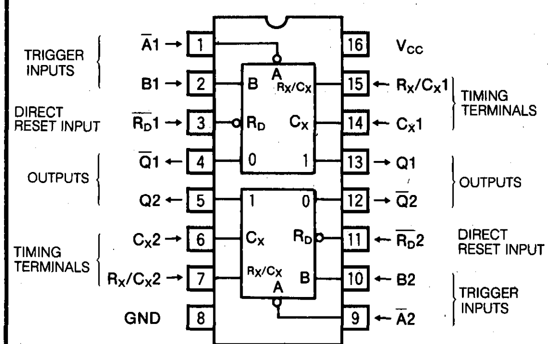
FEATURES

- Retriggerable multivibrator can generate wide output pulses.
- Direct reset input can interrupt output pulses.
- High-speed: 28ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide supply voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



16P4
Outline 16P2N
16P2P

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC123 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS123.

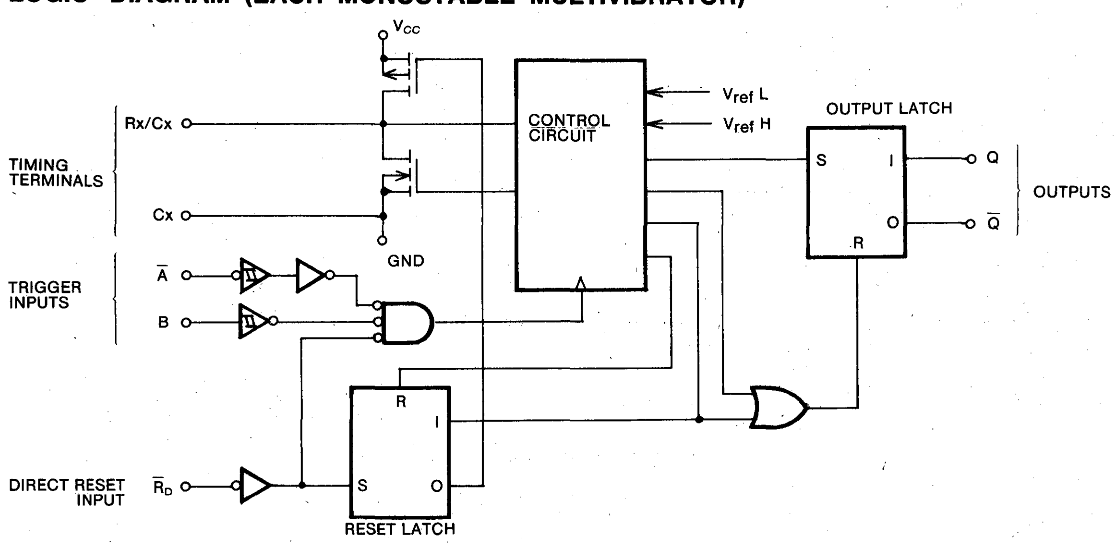
When external resistor R_X and electrostatic capacitor C_X are connected to timing terminals R_X/C_X and C_X as shown in Fig. 1, and trigger pulses are applied at inputs $\overline{A}$ or B, positive pulses will appear at Q and negative pulses at $\overline{Q}$. (Fig. 2-(a))

The pulse width t_{WQ} is set by R_X and C_X. The trigger is applied when $\overline{A}$ changes from high-level to low-level or when B changes from low-level to high-level. The retrigger function is used to obtain longer pulse width and output pulses can be extended by retriggering at $\overline{A}$ or B before the output pulse is completed. (Fig. 2-(b))

When direct reset input $\overline{R}_D$ is set low, Q will be reset low and $\overline{Q}$ will be reset high, irrespective of the output state, allowing output pulses to be narrower by $\overline{R}_D$. (Fig. 2-(c))

When $\overline{R}_D$ changes from low-level to high-level while A is low and B is high, the trigger is applied and Q and $\overline{Q}$ change state.

LOGIC DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



FUNCTION TABLE (Note 1)

Inputs			Outputs	
$\overline{R_D}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔
↑	L	H	⎍	⊔

Note 1 : ↑ : Change from low to high level
↓ : Change from high to low level
⎍ : Positive one-shot operation
⊔ : Negative one-shot operation
X : Irrelevant

OPERATION

1. How to use the timing terminals

Resistor R_X and capacitor C_X are connected to timing terminals R_X/C_X and C_X, as shown in Fig. 1. If C_X is polar, the positive lead should be connected to the R_X/C_X side, and the negative lead to the C_X side. A diode is connected to prevent latchup.

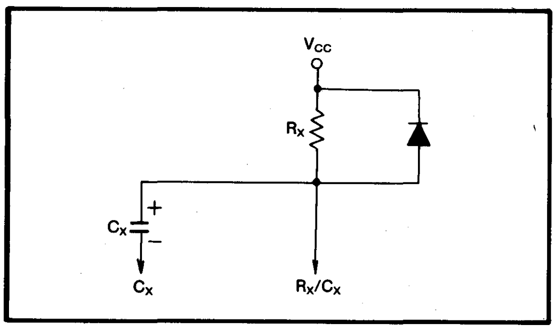


Fig.1 Connection of external resistor R_X and capacitor C_X to timing terminals R_X/C_X and C_X

2. Output Pulse Width t_{WQ}

The output pulse width t_{WQ} is determined as follows:
When $C_X > 100000\text{pF}$, $R_X \geqq 10\text{k}\Omega$
$t_{WQ} = 0.46 C_X \cdot R_X$ (ns)
C_X is given in pF, and R_X in kΩ.

3. Output Pulse Width Control

The output pulse width can be controlled in the following three ways.

3—1 Normal Use
Fig. 2-(a) is the directions as ordinary monostable multivibrator operation and the output pulse width t_{WQ} can be set by using the formula and figure shown in section 2 above.

3—2 Extendtion of the output pulse width with retrigger function
As shown in Fig. 2-(b), the output pulse width can be extended at will by applying additional trigger pulses before the output is completed.

3—3 Shortening of the output pulse width with $\overline{R_D}$ signal
As shown in Fig. 2-(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as reguired.

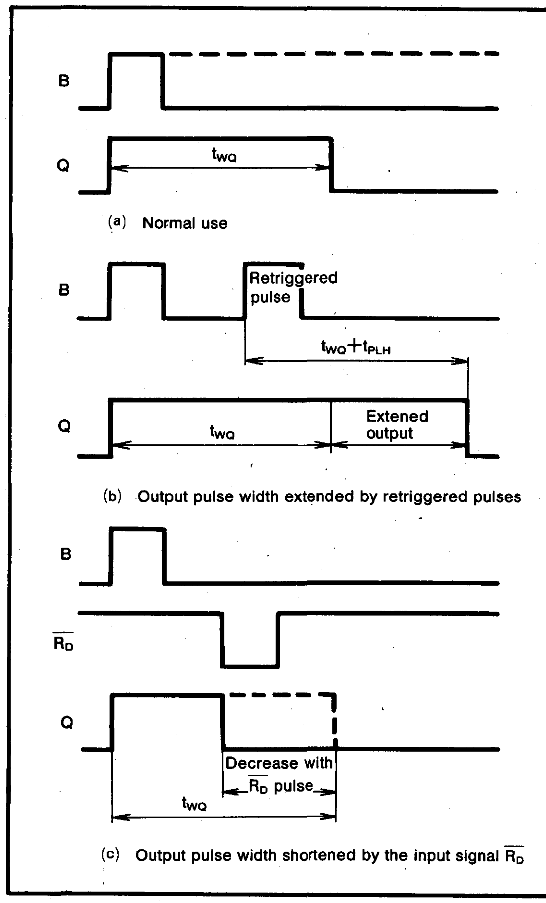


Fig.2 Outnut pulse width control

4. Precations for Use

4—1 Additional trigger pulses must be applied at least trr later after the previous trigger pulse has been applied. The retrigger pulse during this period is ineffective.

4—2 The lead length of external resistor R_X and capacitor C_X should be as short as possible (less than 3cm) to minimize stray wiring capacitance and to prevent misoperation due to noise. Care should also be taken to isolate this circuit from noise sources as far as possible.

4—3 Insert a capacitor of 0.01 ~ 0.1μF with good high-frequency characteristics between V_{CC} and GND.

4—4 Output pulses may be generated when the power is switched on.

4—5 Capacitor discharge when the power is turned off may cause thermal breakdown or latchup, so a diode should be connected as shown in Fig. 1.

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	$V_I < 0V$	−20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	−20	mA
		$V_O > V_{CC}$	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65~+150	℃

Note 2: M74HC123FP, T_a = −40~+70℃ and T_a = 70~85℃ are derated at −6mW/℃.
M74HC123DP, T_a = −40~+50℃ and T_a = 50~85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime ($\overline{A}$, B)		no restriction			ns
	Input risetime, falltime ($\overline{R_D}$)	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	
R_X	External timing resistance	V_{CC}=2.0V	5		1000	kΩ
		V_{CC}≧3.0V	1		1000	
C_X	External timing capacitance		no restriction			F

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40∼+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert=20\mu A$		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$ $\lvert I_O \rvert=20\mu A$		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I=V_{IH}$, V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9			1.9		V
			$I_{OH}=-20\mu A$	4.5	4.4			4.4		
			$I_{OH}=-20\mu A$	6.0	5.9			5.9		
			$I_{OH}=-4.0mA$	4.5	4.18			4.13		
			$I_{OH}=-5.2mA$	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	$V_I=V_{IH}$, V_{IL}	$I_{OL}=20\mu A$	2.0			0.1		0.1	V
			$I_{OL}=20\mu A$	4.5			0.1		0.1	
			$I_{OL}=20\mu A$	6.0			0.1		0.1	
			$I_{OL}=4.0mA$	4.5			0.26		0.33	
			$I_{OL}=5.2mA$	6.0			0.26		0.33	
I_{IH}	High-level input current ($\overline{A}$, B, $\overline{R_D}$)	$V_I=6V$		6.0			0.1		1.0	μA
I_{IL}	Low-level input current ($\overline{A}$, B, $\overline{R_D}$)	$V_I=0V$		6.0			−0.1		−1.0	μA
I_{IH}	High-level input current (R_X/C_X)	$V_I=6V$		6.0			0.5		5.0	μA
I_{IL}	Low-level input current (R_X/C_X)	$V_I=0V$		6.0			−0.5		−5.0	
I_{CC}	Quiescent supply current	$V_I=V_{CC}$, GND, $I_O=0\mu A$		6.0			4.0		40.0	μA
I_{CC}	Active supply current	$V_I=V_{CC}$, GND, $R_X/C_X=0.5V_{CC}$		2.0			120		160	μA
				4.5			300		400	
				6.0			600		800	

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25℃$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L=15pF$ (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{A}$, B−Q, $\overline{Q}$)				43	ns
t_{PHL}					43	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Trigger input)($\overline{R_D}$−Q, $\overline{Q}$)				46	ns
t_{PHL}					46	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Reset input)($\overline{R_D}$−Q, $\overline{Q}$)				35	ns
t_{PHL}					35	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

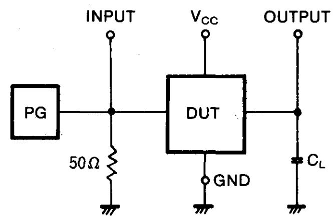
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{A}$, B−Q, $\overline{Q}$)		2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PHL}			2.0			240		300	ns
			4.5			48		60	
			6.0			41		51	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Trigger input) ($\overline{R_D}$−Q, $\overline{Q}$)		2.0			265		330	ns
			4.5			53		66	
			6.0			45		55	
t_{PHL}			2.0			265		330	ns
			4.5			53		66	
			6.0			45		55	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (Reset input) ($\overline{R_D}$−Q, $\overline{Q}$)		2.0			195		245	ns
			4.5			39		49	
			6.0			33		42	
t_{PHL}			2.0			195		245	ns
			4.5			39		49	
			6.0			33		42	
Δt_{WQ}	Pulse width difference between circuits in the same package								%
t_{WQ} (MIN)	Minimum output pulse width	C_X=0pF (Note 4)	2.0			1000		1250	ns
		R_X=5kΩ (V_{CC}=2V)	4.5			200		250	
		R_X=1kΩ (V_{CC}=4.5, 6V)	6.0			180		230	
t_{WQ}	Output pulse width	C_X=100pF	2.0	47		67		67	μs
		R_X=10kΩ	4.5	47		57		57	
		C_L=50pF (Note 4)	6.0	47		57		57	
		C_X=0.1μF	2.0	0.42		0.54	0.42	0.50	ms
		R_X=10kΩ	4.5	0.42		0.50	0.42	0.50	
		C_L=50pF (Note 4)	6.0	0.42		0.50	0.42	0.50	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)								pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIERMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W ($\overline{A}$, B)	Minimum trigger pulse width		2.0			100		120	ns
			4.5			20		24	
			6.0			17		21	
t_W ($\overline{R_D}$)	Minimum direct reset pulse width		2.0			75		90	ns
			4.5			15		18	
			6.0			13		16	
trr	Minimum retrigger time	C_X=100pF	4.5						ns
		R_X=1kΩ	6.0						
		C_X=0.1μF	4.5						ns
		R_X=1kΩ	6.0						

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM