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GEC PLESSEY
SEMICONDUCTORS

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SP8655A 200MHz÷32, SP8657A 200MHz÷20, SP8659B 200MHz÷16

The SP8655A, SP8657A and SP8659B are low power ECL counters with open collector output capable of driving TTL or CMOS and have internally biased inputs.

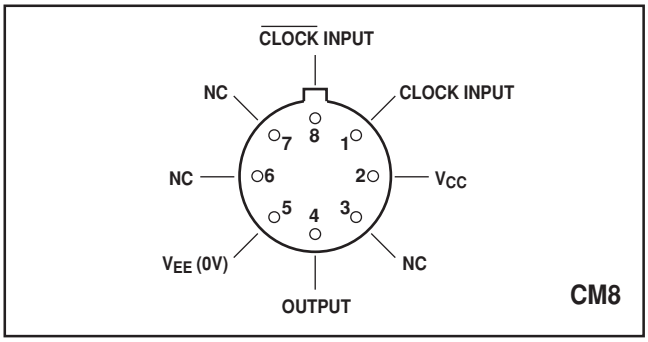

Fig. 1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- CMOS/TTL Compatible Open Collector Output

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QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 50mW
- Temperature Range: −55°C to +125°C (SP8655A, SP8657A)
  −30°C to +70°C (SP8659B)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8655 A CM
SP8657 A CM
SP8659 B CM

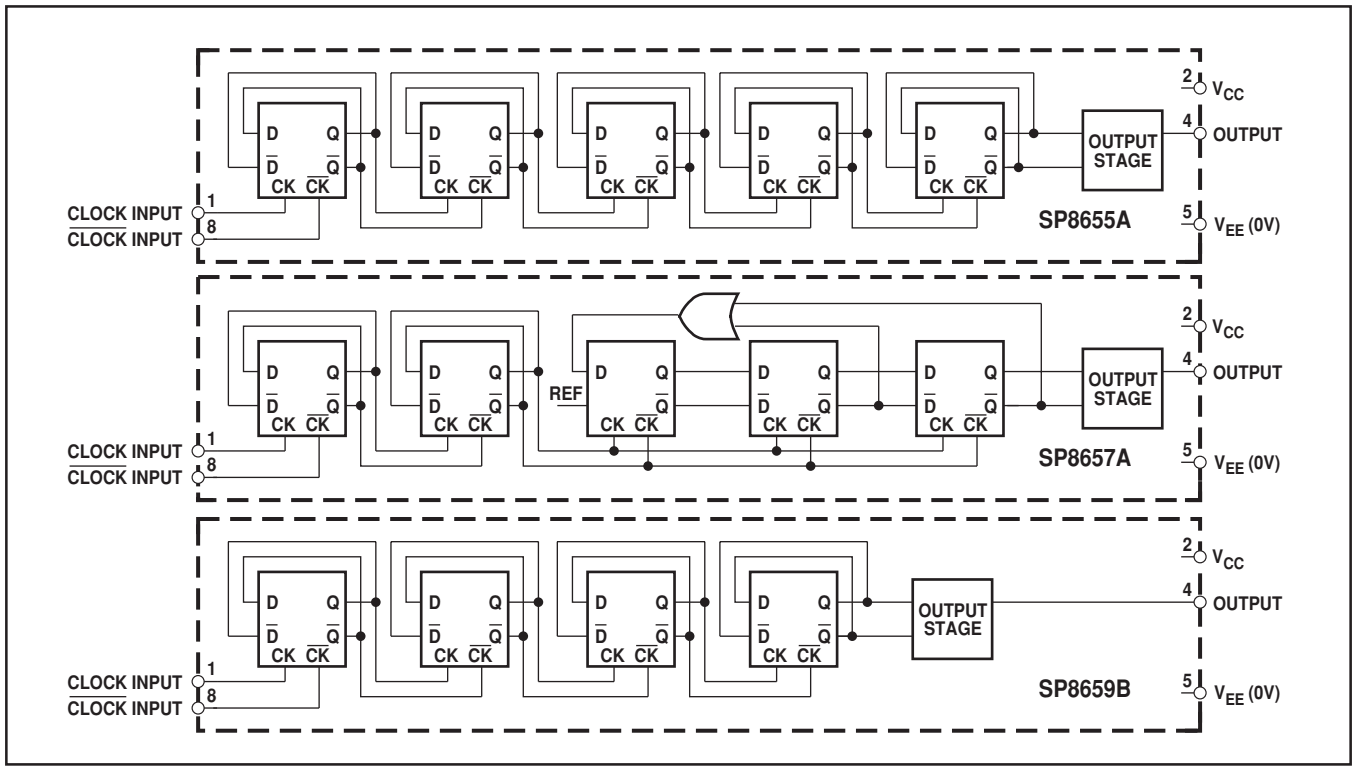

Fig. 2 Functional diagrams

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ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage, V_{CC} = 5·0V±0·25V, V_{EE} = 0V

Temperature, T_{AMB} = −55°C to +125°C (SP8655A, SP8657A), −30°C to +70°C (SP8659B)

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p
Power supply current	I_{CC}		13	mA	
Output high voltage	V_{OH}	7·5		V	V_{CC} = 5V, $C_{LOAD} \leqslant$ 5pF, pin 4 = 1·5kΩ to 10V
Output low voltage	V_{OL}		0·45	V	V_{CC} = 5V, pin 4 = 1·5kΩ to 10V

NOTES

1. The test configuration for dynamic testing is shown in Fig.5.
2. Above characteristics are not tested at 25°C (tested at low and high temperatures only).

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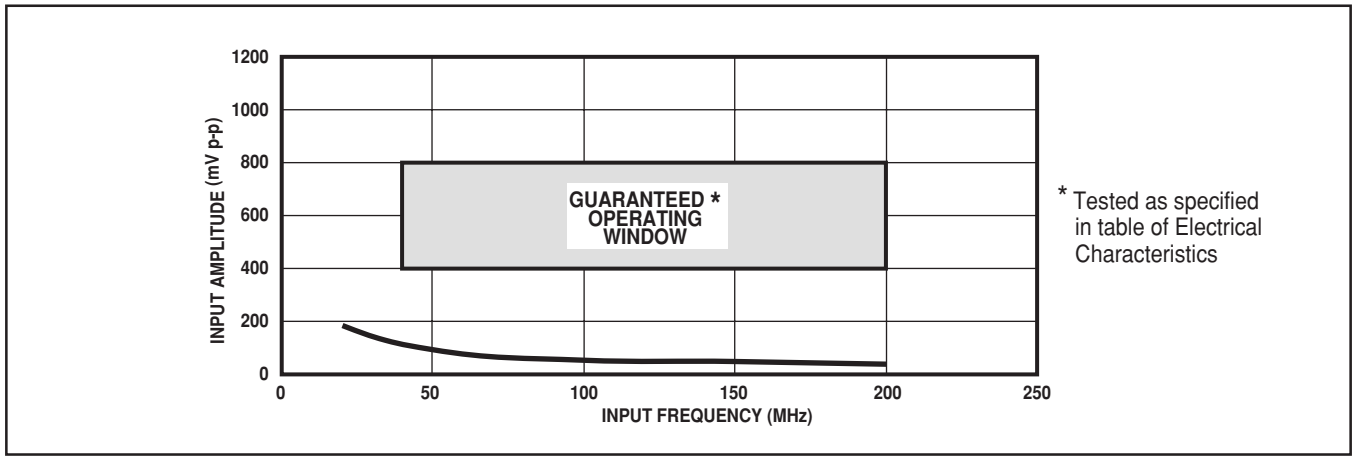

Fig. 3 Typical input characteristic

OPERATING NOTES

1.The clock inputs (pins 1 and 8) should be capacitively coupled to the signal source. When driven single ended, the input signal path is completed by a capacitor from the unused input to ground.

2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39kΩ resistor from either input to ground. If the device is driven single ended, it is recommended that the pull-down resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.

3. The device will operate down to DC but input slew rate must be better than 100V/µs.

4. The open collector output will drive three TTL loads, and therefore requires a a suitable resistor to V_{CC} to maintain noise immunity. In order to maintain noise immunity on transitions, this resistor should not exceed 4·7kΩ. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3·3kΩ resistor.

5. Input impedance varies as a function of frequency; see Fig. 4.

6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore, the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements.

In the test configuration of Fig. 5, the output rise time is approximately 20ns and the fall time is typically 10ns.

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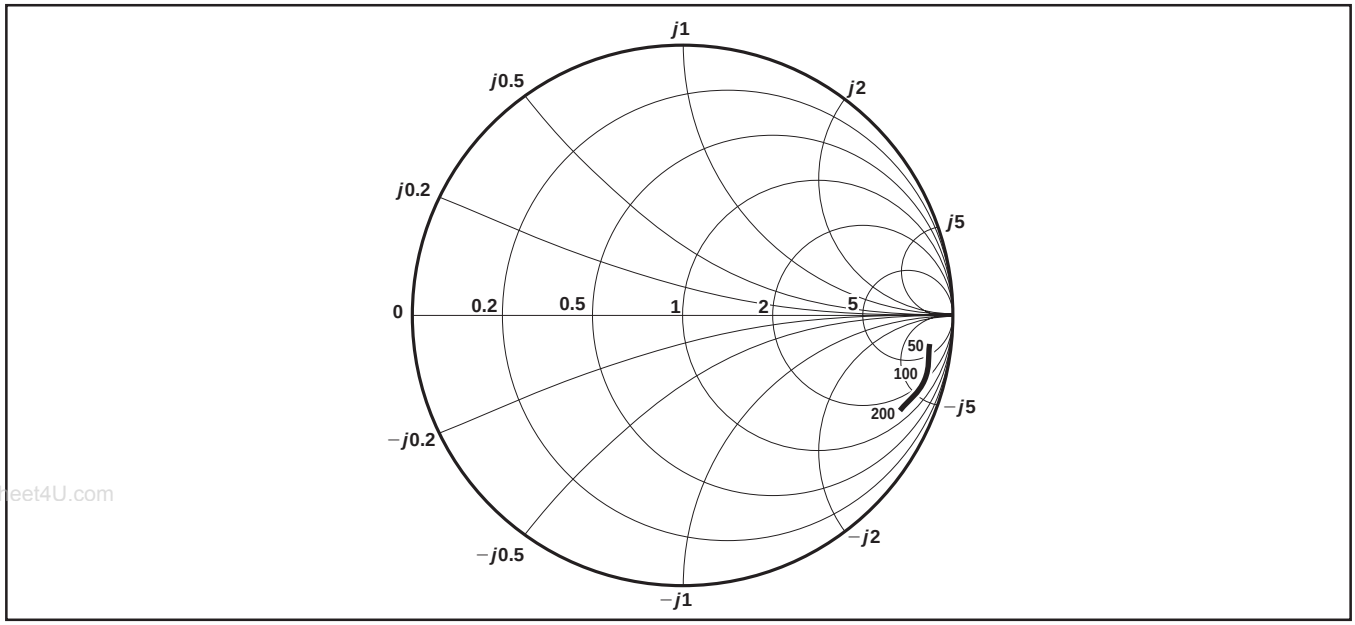

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Fig. 4 Typical input impedance. Test conditions: supply voltage = 5·0V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

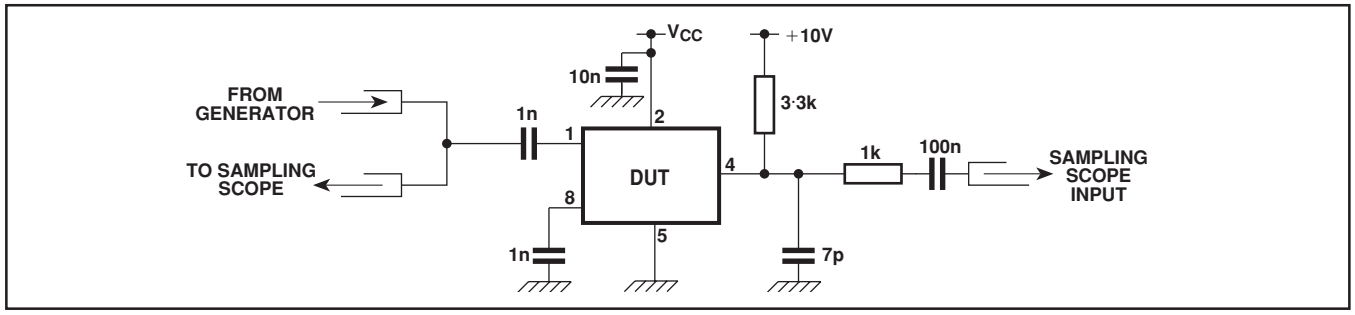

Fig. 5 Test circuit

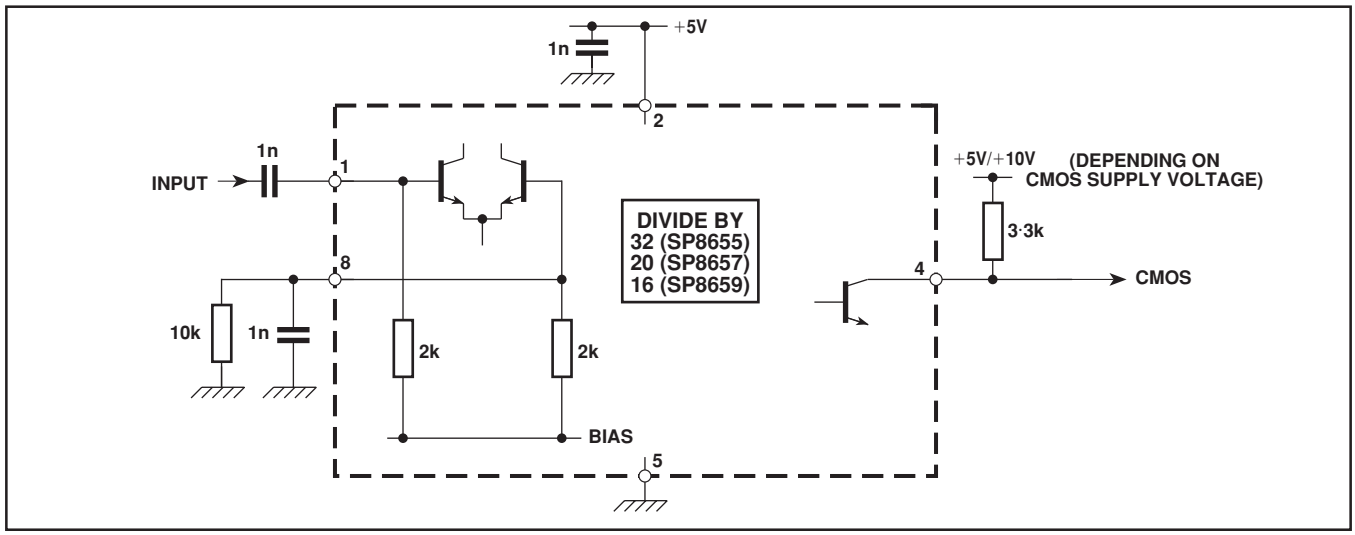

Fig. 6. Typical application circuit showing interfacing

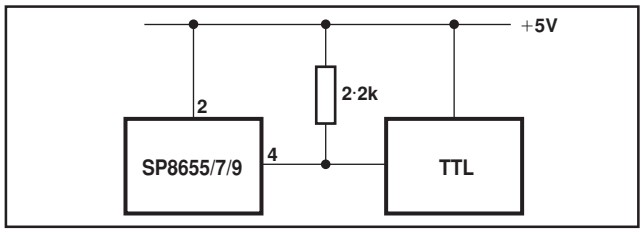

Fig. 7. Interfacing to TTL. Load not to exceed 3 TTL unit loads

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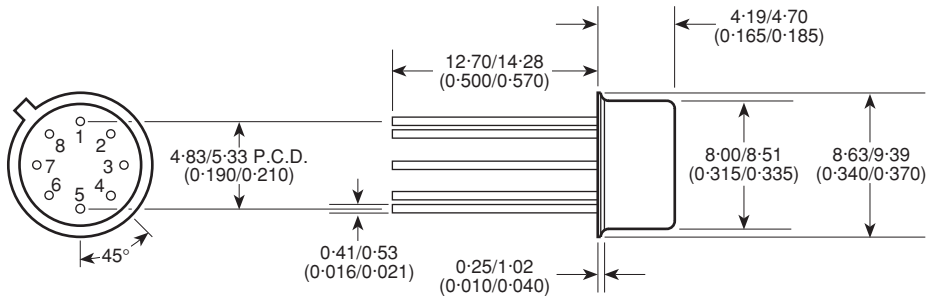
PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

8-LEAD METAL CAN - CM8

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