Features

- 3.3V operating voltage
- Up to 120MSPS for 6-channel inputs
- 9-bit programmable gain amplifier
- 8-bit programmable offset
- 4-bit programmable line-clamping bias
- Internal voltage reference
- 3-wire serial control interface
- 48-pin LQFP-EP package

Applications

- Currency Scanner Double Sided Scanners

General Description

The HT82V48 is a fully integrated, dual high performance 16-bit 3-channel 60MSPS analog signal processor for high-speed double-sided scanner applications.

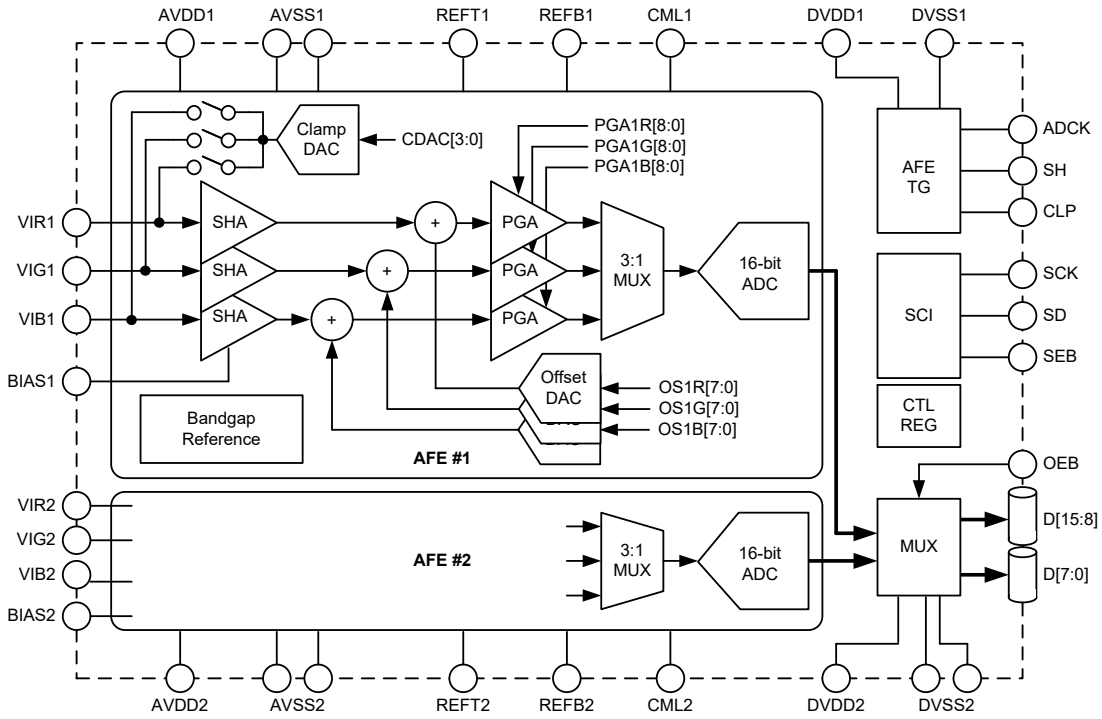
Each channel consist a Sample and Hold Amplifier, a 9-bit Programmable Gain Amplifier and an 8-bit offset correction Digital to Analog Converter. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for the two 3-channel analog inputs. Each of the 3-channel signals are routed to a 60MHz high performance analog-to-digital converter.

For image sensor reference level stabilisation, the device also provide programmable line-clamping bias internally.

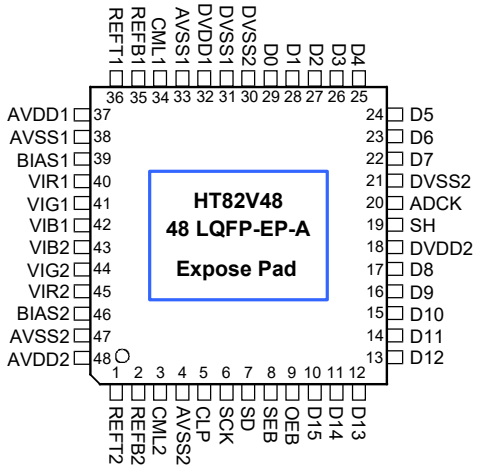
The internal registers are programmed through a 3-wire serial interface, which provides timing control, gain, offset and operating mode adjustments.

The device operates from a single 3.3V power supply with a typical power consumption of 925mW.

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Description
DVDD1	P	AFE Digital Supply
VSS1	P	AFE Digital Ground
DVDD2	P	Data Bus Digital Supply
VSS2	P	Data Bus Digital Ground
AVDD1	P	AFE #1 Analog Supply
AVSS1	P	AFE #1 Analog Ground
AVDD2	P	AFE #2 Analog Supply
AVSS2	P	AFE #2 Analog Ground
ADCK	DI	System Master Clock and ADC Sampling Clock
SH	DI	Sample-Hold Clock
CLP	DI	Clamping Interval
SCK	DI	Serial Control Interface (SCI) Clock
SD	DIO	SCI Data
SEB	DI	SCI Enable, Active Low
VIR1	AI	Analog Input , AFE #1 Channel R
VIG1	AI	Analog Input , AFE #1 Channel G
VIB1	AI	Analog Input , AFE #1 Channel B
BIAS1	AIO	AFE #1 Bias Decoupling
REFB1	AO	AFE #1 ADC Bottom Reference Voltage Decoupling
REFT1	AO	AFE #1 ADC Top Reference Voltage Decoupling
CML1	AO	AFE #1 Internal Bias Level Decoupling
VIR2	AI	Analog Input , AFE #2 Channel R
VIG2	AI	Analog Input , AFE #2 Channel G
VIB2	AI	Analog Input , AFE #2 Channel B
BIAS2	AIO	AFE #2 Bias Decoupling
REFB2	AO	AFE #2 ADC Bottom Reference Voltage Decoupling
REFT2	AO	AFE #2 ADC Top Reference Voltage Decoupling
CML2	AO	AFE #2 Internal Bias Level Decoupling

Pin Name	I/O	Description
OEB	DI	Output Data Enable, Active Low
D[15:8]	DO	Data Output
D[7:0]	DO	Data Output

Type: AI=Analog Input; AO=Analog Output; AIO=Analog In/out, DI=Digital Input; DO=Digital Output; DIO=Digital In/out, P=Power

Absolute Maximum Ratings

Supply Voltage .....V_{SS}-0.3V to V_{SS}+4.3V

Input Voltage .....V_{SS}-0.3V to V_{DD}+0.3V
Analogue Supply Power .....3.0V to 3.6V

Storage Temperature .....-50°C to 125°C
Operating Temperature.....0°C to 70°C
Digital supply power.....3.0V to 3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
AV_{DD}	Analogue Supply Power	—	3.0	3.3	3.6	V
DV_{DD}	Digital Supply Power	—	3.0	3.3	3.6	V
Digital Inputs						
V_{IH}	High level input voltage	—	0.7×DV_{DD}	—	—	V
V_{IL}	LOR level input voltage	—	—	—	0.2×DV_{DD}	V
I_{IH}	High level input current	—	—	—	1	μA
I_{IL}	LOR level input current	—	—	—	1	μA
C_I	Input capacitance	—	—	5	—	pF
Digital Outputs						
V_{OH}	High level output voltage	I_{OH}=1mA	DV_{DD}-0.5	—	—	V
V_{OL}	LOR level output voltage	I_{OL}=1mA	—	—	0.5	V
I_{OZ}	High impedance output current	—	—	—	1	μA

AV_{DD}=DV_{DD}=3.3V, AV_{SS}=DV_{SS}=0V, Ta=25°C, ADCK=60MHz unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Overall system specification (including 16-bit ADC, PGA, Offset and SHA functions)						
	Maximum Conversion rate	—	—	60	—	MSPS
	Full-scale input voltage range	LOR=0; Max Gain	—	0.33	—	V_{P-P}
		LOR=0; Min Gain	—	3.03	—	V_{P-P}
		LOR=1; Max Gain	—	0.20	—	V_{P-P}
		LOR=1; Min Gain	—	1.82	—	V_{P-P}
V_{IN}	Input signal limits	—	AV_{SS}-0.3	—	AV_{DD}+0.3	
	Full-scale transition error	Gain=0dB	—	30	—	mV

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Zero-scale transition error	Gain=0dB	—	30	—	mV
DNL	Differential non-linearity	—	—	2	—	LSB
INL	Integral non-linearity	—	—	50	—	LSB
	Channel to channel gain matching	—	—	1.5	—	%
	Total output noise	Min Gain	—	30	—	LSB_{rms}
		Max Gain	—	300	—	LSB_{rms}
References						
V_{RT}	Upper reference voltage	LOR=0	1.95	2.05	2.25	V
		LOR=1	—	1.85	—	V
V_{RB}	LORer reference voltage	LOR=0	0.95	1.05	1.25	V
		LOR=1	—	1.25	—	V
CML	Input return bias voltage	—	—	1.5	—	V
V_{RTB}	Differential reference voltage	LOR=0	0.90	1.0	1.10	V
		LOR=1	—	0.6	—	V
Clamping(CLP) DAC						
	Resolution	—	—	4	—	bits
V_{CSTEP}	Step size	CRNG=0	—	0.173	—	V/step
		CRNG=1	—	0.11	—	
V_{CBOT}	Output voltage at code 0h	—	—	0.4	—	V
V_{CTOP}	Output voltage at code Fh	CRNG=0	—	2.76	—	V
		CRNG=1	—	2.05	—	
DNL	Differential non-linearity	—	-0.5	—	+0.5	LSB
INL	Integral non-linearity	—	—	+/-1	—	LSB
Offset DAC						
	Resolution	—	—	8	—	bits
	Step size	—	—	2.274	—	mV/step
	Output voltage	Code 0x00	—	-290	—	mV
		Code 0xFF	—	+290	—	mV
Programmable Gain Amplifier						
	Resolution	—	—	9	—	bits
	Gain equation	—	0.67 + PGA[8:0] × 5.35/511			V/V
G_{MAX}	Max gain, each channel	—	—	6.0	—	V/V
G_{MIN}	Min gain, each channel	—	—	0.65	—	V/V
	Channel Matching	—	—	5	15	%
A/D Converter						
	Resolution	—	—	16	—	bits
	Speed	—	—	60	—	MSPS
	Full-scale input range	LOR=0	—	2	—	V
		LOR=1	—	1.2	—	V
Digital Inputs						
V_{IH}	High level input voltage	—	$0.7\times DV_{DD}$	—	—	V
V_{IL}	LOR level input voltage	—	—	—	$0.2\times DV_{DD}$	V
I_{IH}	High level input current	—	—	—	1	μA
I_{IL}	LOR level input current	—	—	—	1	μA
C_I	Input capacitance	—	—	5	—	pF
Digital Outputs						

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	I_{OH}=1mA	DV_{DD}-0.5	—	—	V
V_{OL}	LOR level output voltage	I_{OL}=1mA	—	—	0.5	V
I_{OZ}	High impedance output current	—	—	—	1	μA
Digital I/O Pins						
V_{IH}	Applied high level input voltage	—	0.7×DV_{DD}	—	—	V
V_{IL}	Applied low level input voltage	—	—	—	0.2×DV_{DD}	V
V_{OH}	High level output voltage	I_{OH}=1mA	DV_{DD}-0.5	—		V
V_{OL}	Low level output voltage	I_{OL}=1mA	—	—	0.5	V
I_{IL}	Low level input current	—	—	—	1	μA
I_{IH}	High level input current	—	—	—	1	μA
I_{OZ}	High impedance output current	—	—	—	1	μA
Supply Currents						
	Total supply current	—	—	290	—	mA
	Analogue supply current	—	—	240	—	mA
	Digital supply current	—	—	50	—	mA
	Power down mode	—	—	400	—	μA

A.C. Characteristics

AV_{DD}=DV_{DD}=3.3V, AV_{SS}=DV_{SS}=0V, Ta=25°C, ADCK=60MHz unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Clock Parameter						
t_{ADCK}	ADCK period	—	16.67	—	—	ns
DUTY	ADCK duty	—	45	50	55	%
t_{SSH}	SH setup time	—	0	—	4	ns
t_{HSH}	SH hold time	—	0	—	4	ns
t_{SH}	SH width	—	—	1/2	—	ADCK
Serial Control Interface						
t_{SSCK}	SCK setup time	—	10	—	—	ns
t_{HSCK}	SCK hold time	—	10	—	—	ns
t_{SSD}	SD setup time	—	10	—	—	ns
t_{HSD}	SD hold time	—	10	—	—	ns
t_{TSD}	SD transition time; input/output alternated	—	5	—	—	ns
Data Output						
t_{VD}	3-state to data valid	—	—	3	4	ns
t_{ZD}	Output enable high to 3-state	—	—	3	4	ns
t_{DD}	Data output propagation delay	—	—	8	10	ns
LAT	Output latency (Pipeline delay)	—	—	—	7	ADCK

Note: Parameters are measured at 50% of the rising/falling edge.

Functional Description

Introduction

The HT82V48 can sample up to two groups of three inputs, namely VIR1, VIG1, VIB1, VIR2, VIG2 and VIB2 simultaneously. After sampling the device then processes the sampled video signals with respect to an external reference level. Each processing channel consists of an input sampling block, a 4-bit programmable RLC DAC, an 8-bit programmable offset DAC and 9-bit Programmable Gain Amplifier. The ADC then converts each resulting analogue signal to a 16-bit digital word. The digital output from the ADC is then presented on an 8-bit or 16-bit wide bus. Internal control registers determine the configuration of the device, including the bias, offsets and gain applied on each channel. These registers are programmable via the devices' Serial Control Interface.

Internal Power-On-Reset Circuit

The internal POR Circuit power is supplied on AV_{DD} and is used to reset digital logic into a default state after power-up. The POR circuit is active from a voltage equal to $0.6V_{Typ.}$ of AV_{DD} and is released when the voltage reaches $1.2V_{Typ.}$ of $AV_{DD.}$ (or $0.7V_{Typ.}$ of DV_{DD} if AV_{DD} powers up before DV_{DD}). When AV_{DD} or DV_{DD} returns to $0.6V_{Typ.}$ the POR will again re-active. To ensure the control registers contents are at their default values before carrying out any other register writes it is recommended that a software reset is issued each time the power is cycled.

Power Management

After the device is powered up, the register bit, PDNB, allows the device to be fully powered down when cleared to zero. Individual blocks can be powered down using the bits in System Setup Register 1.

References

The ADC reference voltages are derived from an internal bandgap reference and buffered to pins REFT and REFB, where they must be decoupled to ground. Pin CML is driven by a similar buffer and also requires decoupling. The output buffer from the CLP DAC also requires decoupling on pins BIAS1 and BIAS2.

S/H Processing

The video level is processed with respect to the voltage on pins BIAS1 and BIAS2. BIAS1 and BIAS2 voltage are sampled at the same time as SH samples the video level.

Bias and Clamping

External Bias

The S/H circuit reference levels are supplied by the BIAS1 and BIAS2 pins.

Internal Bias

The S/H circuit reference level is supplied by the CLP DAC when CDACB=1. The level is programmed by the CDAC[3:0] bits. The operation is shown in Figure 1.

Line Clamping

In situations where the input video signal does not have a stable reference level it may be necessary to clamp only when those pixels which have a known state (e.g. the dummy, or black pixels at the start or end of a line of most image sensors). Use the CLP pin to identify the black pixels and enable the clamp at the same time as when the input is being sampled (i.e. when SH is high and CLP is high). This mode is enabled by setting CLPEN=1. The operation is shown in Figure 2.

Analog Input Signal Sampling

There is only one S/H mode supported by the device. The ADCK:SH ratio is maintained at 3:1.

For AFE #1, VIR1, VIG1 and VIB1 video inputs are sampled at the same time and converted by a high-speed A/D converter to multiplexed digital data. The AFE #2 video inputs, VIR2, VIG2 and VIB2 are also sampled at the same time. The reference timing diagram is shown in Figure 3.

Output Formats

The device output can be presented in several different formats under control of the ODFM[1:0] register bits as shown in Figure 3.

The device supports 8-bit (ODFM[1:0]=[0,0]) resolution when AFE #1 and AFE #2 are operated at the same time during video signal processing. For DC level calibration, 16-bit resolution is enabled by setting ODFM[1:0] = [0, 1] or [1, 0] for AFE #1 or AFE #2.

Offset Adjust and Programmable Gain

An 8-bit Offset DAC is provided to compensate for offsets and then amplified by a 9-bit PGA. The gain and offset for each channel are independently programmable by control bits OS<u>XY</u>[7:0] and PGA<u>XY</u>[7:0].

ADC Input Black Level Adjust

The output from the PGA can be offset to match the full-scale range of the differential ADC($2\times(V_{RT}-V_{RB})$).

Serial Control Interface

SCK, SD and SEB are used both for register writing and reading. The R/WB bit for SD is used to determine whether the control is data write (R/WB=0) or data read (R/WB=1). The procedure is initiated on an SEB falling edge.

For a register write, an address A[4:0] is clocked in through SD, followed by 2 dummy clocks and a data word D[7:0]. Each bit is latched on the SCK rising edge. The dummy clocks are used for internal address data latch and decoding.

For a register read-back operation, the SD address and dummy clocks are the same as for the register write procedure. Here SD will change from an input to an output port and send out an output data word D[7:0] on the SCK falling edge after the end of a dummy clock. Then SD will change from an output to an input port after an SEB rising edge.

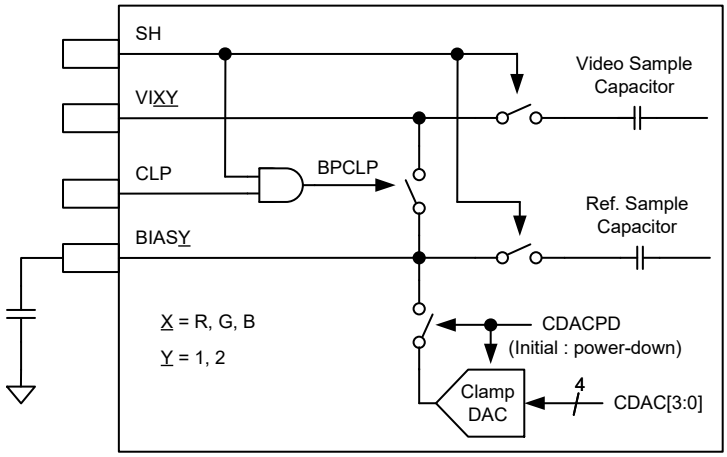


Figure 1 Bias and Clamping Configuration

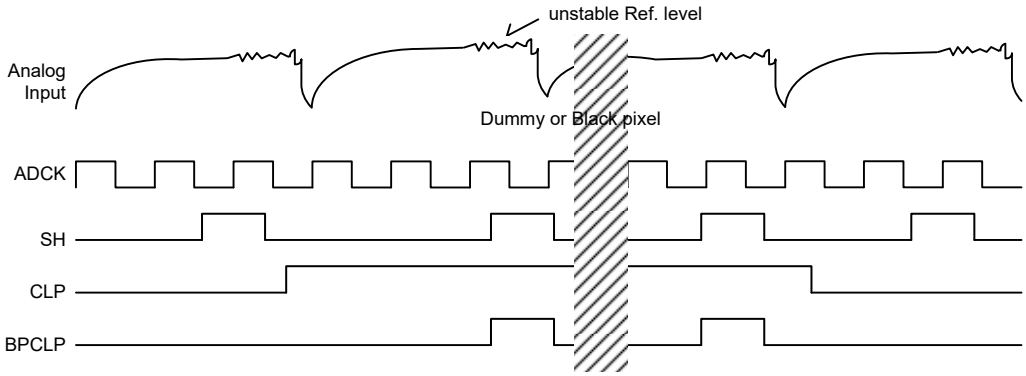
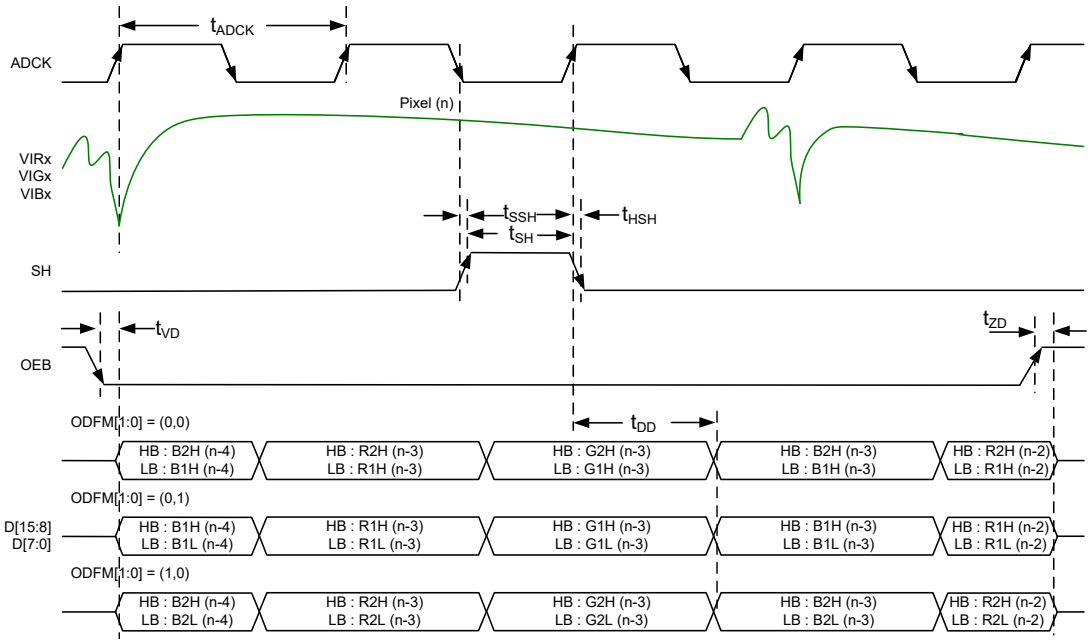


Figure 2 Clamping Operation



Where LB(or HB) denote low-byte(or high-byte), "R(or G, B)" denote channel R(or G, B), "1(or 2)" denote AFE #1(or #2), "L(or H)" denote low-byte (or high-byte) data and "n" denote pixel number.

Figure 3 S/H and Data Output Control Timing

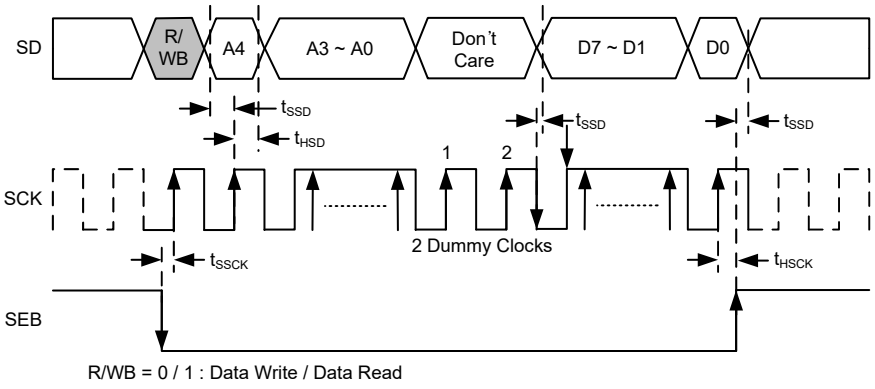


Figure 4 Serial Control Interface Timing

Control Registers

Register Mapping

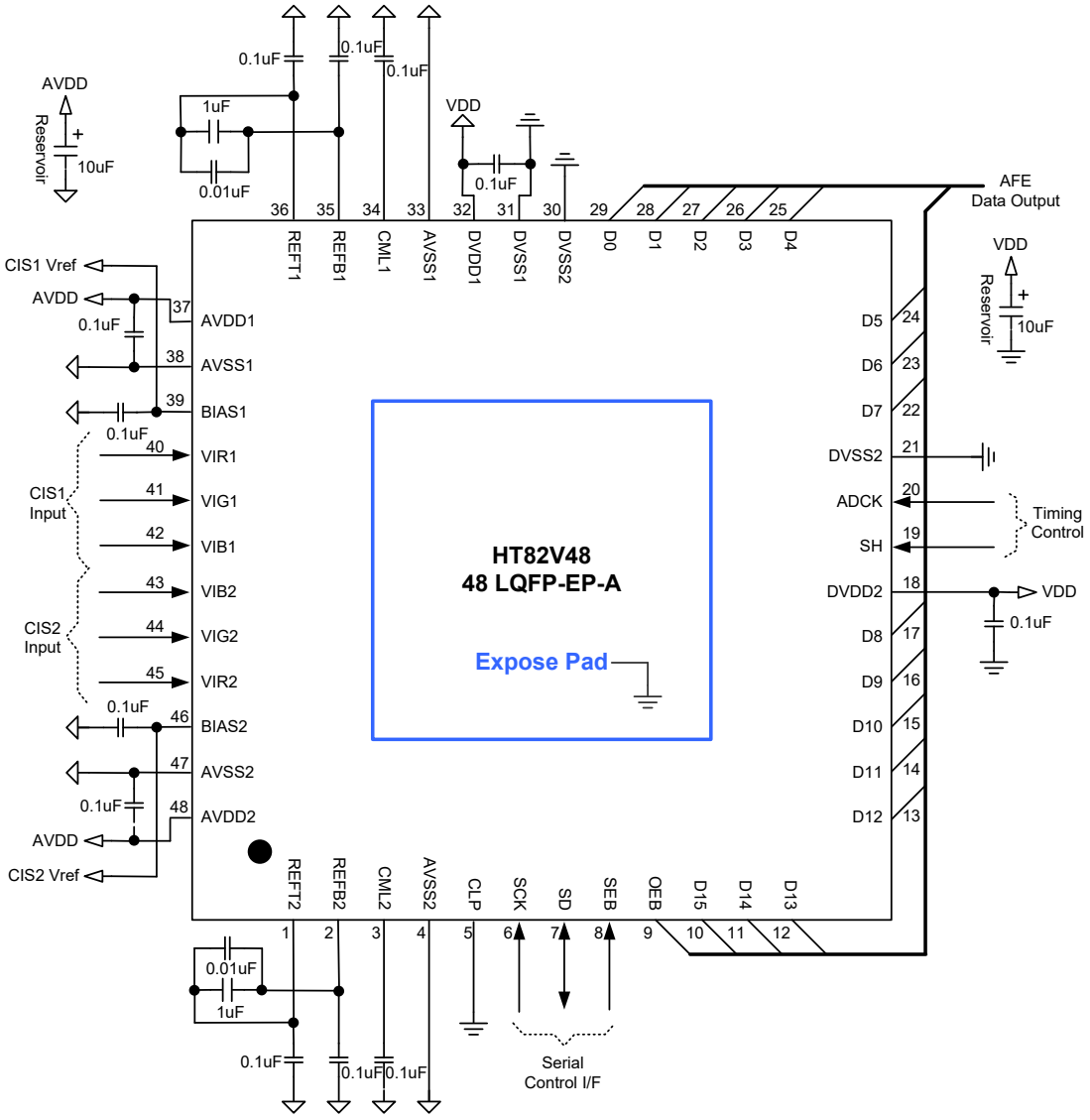
Here X denotse AFE #1 and AFE #2; Y denotse channel R, channel G and channel B

Address	Description	POR	D7	D6	D5	D4	D3	D2	D1	D0
00h	System Setup Register 1	07h	ODFM[1:0]		0	0	60M	AFE2B	AFE1B	PDNB
01h	AFE Setup Register 1	00h	CDAC[3:0]				CLPEN	CRNG	CDACB	LOR
02h	AFE_1 CH_R PGA gain	00h	PGA1R[7:0]							
03h		00h	—							PGA1R[8]
04h	AFE_1 CH_G PGA gain	00h	PGA1G[7:0]							
05h		00h	—							PGA1G[8]
06h	AFE_1 CH_B PGA gain	00h	PGA1B[7:0]							
07h		00h	—							PGA1B[8]
08h	AFE_2 CH_R PGA gain	00h	PGA2R[7:0]							
09h		00h	—							PGA2R[8]
0Ah	AFE_2 CH_G PGA gain	00h	PGA2G[7:0]							
0Bh		00h	—							PGA2G[8]
0Ch	AFE_2 CH_B PGA gain	00h	PGA2B[7:0]							
0Dh		00h	—							PGA2B[8]
0Eh	AFE_1 CH_R Offset value	00h	OS1R[7:0]							
0Fh	AFE_1 CH_G Offset value	00h	OS1G[7:0]							
10h	AFE_1 CH_B Offset value	00h	OS1B[7:0]							
11h	AFE_2 CH_R Offset value	00h	OS2R[7:0]							
12h	AFE_2 CH_G Offset value	00h	OS2G[7:0]							
13h	AFE_2 CH_B Offset value	00h	OS2B[7:0]							
14h	Reserved	50h								

Register Description

Register	Bit	Name	POR	Description
System Setup Register 1	0	PDNB	1	0=fully power down 1=fully active
	1	AFE1B	1	0=AFE #1 power down 1=AFE #1 active
	2	AFE2B	1	0=AFE #2 power down 1=AFE #2 active
	3	60M	0	Maximum operating speed 0=50Msps 1=60Msps
	4	Reserved	0	—
	5	Reserved	0	—
	7:6	ODFM[1:0]	00b	Output data format 0,0=D[15:8] : AFE #2 high-byte data; D[7:0] : AFE #1 high-byte data 0,1=D[15:8] : AFE #1 high-byte data; D[7:0] : AFE #1 low-byte data 1,0=D[15:8] : AFE #2 high-byte data; D[7:0] : AFE #2 low-byte data
AFE Setup Register 1	0	LOR	0	Reduces the ADC reference range 2×(V_{RT} - V_{RB}), thus changing the max/min input voltages. 0=ADC reference range=2V 1=ADC reference range=1.2V
	1	CDACB	0	0=CLP DAC power down 1=CLP DAC active
	2	CRNG	0	Sets CLP DAC output range 0=CLP DAC ranges from 0 to AVDD 1=CLP DAC ranges from 0 to V_{RT}
	3	CLPEN	0	Enable clamping function. Clamping switch is controlled by CLP pin.
	7:4	CDAC[3:0]	0	Controls CLP DAC driving BIAS1/BIAS2 pins to define voltage or clamping voltage.
AFE #1 CH_R PGA gain	0	PGA1A[8]	0	AFE #1 channel R PGA gain setting
	7:0	PGA1A[7:0]	00h	
AFE #1 CH_G PGA gain	0	PGA1B[8]	0	AFE #1 channel G PGA gain setting.
	7:0	PGA1B[7:0]	00h	
AFE #1 CH_B PGA gain	0	PGA1C[8]	0	AFE #1 channel B PGA gain setting.
	7:0	PGA1C[7:0]	00h	
AFE #2 CH_R PGA gain	0	PGA1A[8]	0	AFE #2 channel R PGA gain setting.
	7:0	PGA2A[7:0]	00h	
AFE #2 CH_G PGA gain	0	PGA2B[8]	0	AFE #2 channel G PGA gain setting.
	7:0	PGA2B[7:0]	00h	
AFE #2 CH_B PGA gain	0	PGA2C[8]	0	AFE #2 channel B PGA gain setting.
	7:0	PGA2C[7:0]	00h	
AFE_1 CH_R Offset value	7:0	OS1A[7:0]	00h	AFE #1 channel R offset DAC value.
AFE_1 CH_G Offset value	7:0	OS1B[7:0]	00h	AFE #1 channel G offset DAC value.
AFE_1 CH_B Offset value	7:0	OS1C[7:0]	00h	AFE #1 channel B offset DAC value.
AFE_2 CH_R Offset value	7:0	OS2R[7:0]	00h	AFE #2 channel R offset DAC value.
AFE_2 CH_G Offset value	7:0	OS2G[7:0]	00h	AFE #2 channel G offset DAC value.
AFE_2 CH_B Offset value	7:0	OS2B[7:0]	00h	AFE #2 channel B offset DAC value.
Reserved	3:0	—	—	Reserved
	5:4	TEST0[1:0]	01b	Test Mode
	7:6	TEST1[1:0]	01b	Test Mode

Application Circuits



Notes: 1. All decoupling capacitors should be located as close as possible to the HT82V48 AFE.

2. AVSS and DVSS should be connected as close as possible to the HT82V48 AFE.

3. Any exposed pads should be connected to DVSS.

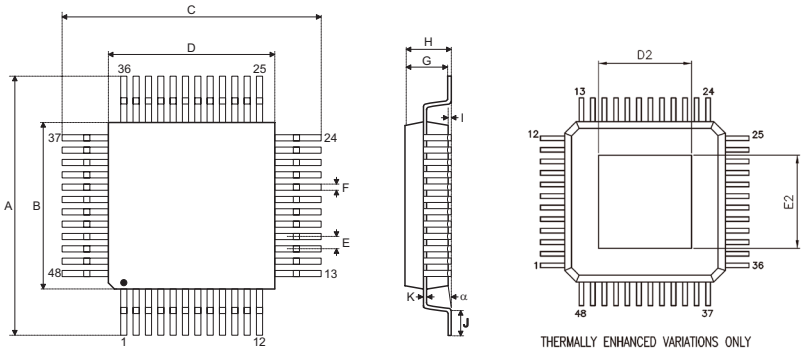
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

48-pin LQFP-EP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
D2	0.079	—	—
E	—	0.020 BSC	—
E2	0.079	—	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
D2	2.00	—	—
E	—	0.50 BSC	—
E2	2.00	—	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°