STP2001QFP

SUN MICROELECTRONICS

July 1997

Slave I/O

DATA SHEET — Integrated SBus Interface Slave I/O Controller

DESCRIPTION

The STP2001Slave I/O Controller is a highly integrated, low-cost, low-power device designed for use in single-processor systems with an SBus interface. The STP2001 provides serial I/O for keyboard, mouse and general-purpose use. In addition, a floppy disk interface, an external byte-wide expansion bus (EBus) for TOD and EPROM, I/O registers and reset control logic are integrated. Together, the STP2001 and the STP2000 Master I/O Controller, provide a complete I/O subsystem.

The two serial ports for keyboard/mouse and general purpose use are compatible with the AMD AM85C30, rev C Serial Communications Controller. The TTY A/B serial ports are fully synchronous, while the keyboard/mouse ports are asynchronous only. All ports support data rates up to 38.4 Kb/s. The NCR82077 floppy disk interface is compatible with the Intel 8077A-1 single-chip floppy controller, supporting up to a 1 MBit/sec transfer rate.

Features	*Benefits*
• Integrates two dual serial controllers, a high-speed floppy controller, uniprocessor interrupt, reset, and counter/timer circuitry, power-down control and an EBus in a single package	• Saves cost, power, board space, and weight
• Directly interfaces to CPU through the SBus	• Improved performance
• Auxiliary I/O registers (used for LED, floppy and system power-down)	• High level of system integration; ease of design
• Interrupt Controller for single-processor SBus system	• High level of system integration; ease of design
• System reset control	• High level of system integration; ease of design
• Counter/timers for single-processor SBus system	• High level of system integration; ease of design
• EBus interface	• Generic 8-bit interface available
• JTAG internal and boundary SCAN logic	• Improved chip and board level testability
• 160-pin PQFP packaging	• Cost effective packaging
• IC is also available from NCR Corp. (PN - NCR89105)	• Second source

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BLOCK, APPLICATION, AND LOGIC DIAGRAMS

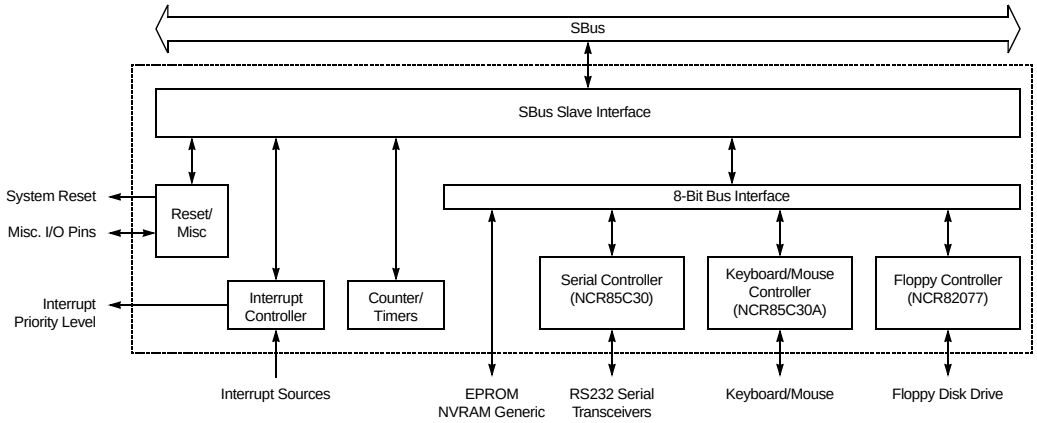

Figure 1. STP2001 Block Diagram

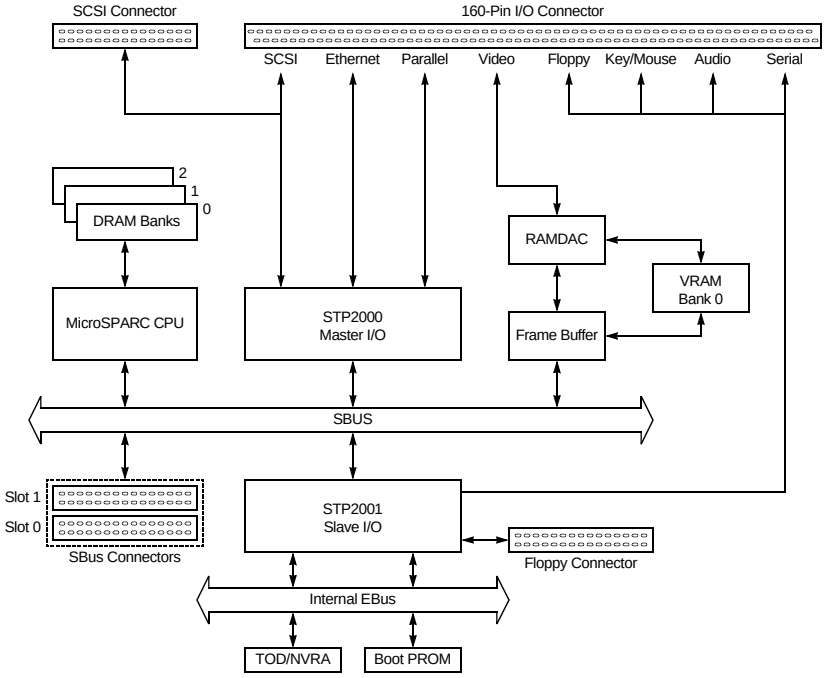

Figure 2. STP2001 Typical Application

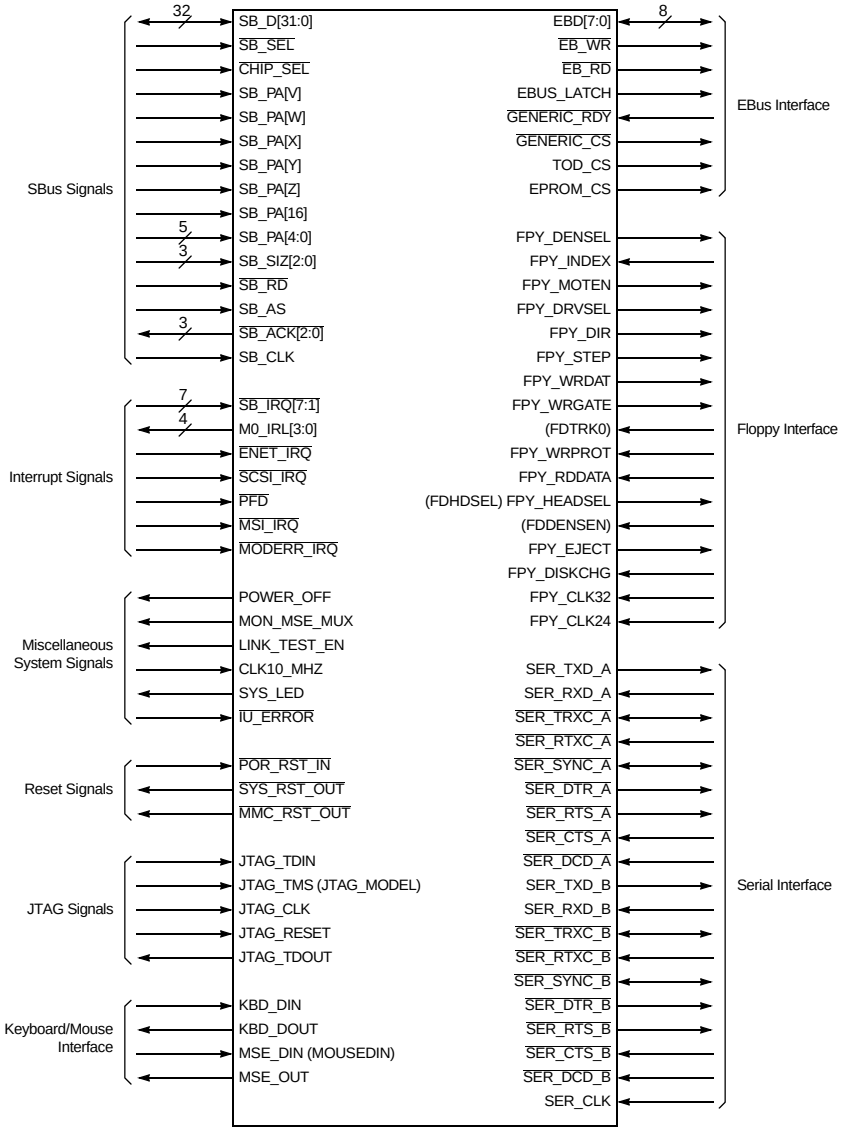

Figure 3. STP2001 Logical Connections

SIGNAL DESCRIPTIONS

SBus Interface: 54 Pins

Signal	Type	Description
SB_D[31:0]	I/O	SBus Data Bus
$\overline{\text{SB\_ACK}}$[2:0]	3-State	SBus Acknowledge
SB_CLK	Input	SBus Clock Input
SB_RD	Input	SBus Read/Write
$\overline{\text{SB\_SEL}}$	Input	SBus Select
SB_SIZ[2:0]	Input	SBus Transfer Size
$\overline{\text{SB\_AS}}$	Input	SBus Address Strobe (address is valid)
$\overline{\text{CHIP\_SEL}}$ [1]	Input	High order physical address bits (for slave decodes)
SB_PA[V:Z] [2]	Input	High order physical address bits (for slave decodes)
SB_PA[16]	Input	PA[16] (for system/user selection in INT/TMR)
SB_PA[4:0]	Input	Low order physical address bits

1. The $\overline{\text{CHIP\_SEL}}$ pin is an additional qualifier (active low) to the $\overline{\text{SB\_SEL}}$ line. When sharing a single SBus select line with another device (such as the STP2000QFP), one of the high order SBus physical address lines, such as PA[27], can be tied to the $\overline{\text{CHIP\_SEL}}$ pin to distinguish between the two devices.
2. In some system configurations, the high order physical address bits can be connected as follows: SB_A[V, W, X, Y, Z]=PA[24:20].

EBus Interface: 15 pins

Signal	Type	Description
EB_D[7:0]	I/O	EBus data
EB_ADDRLATCH	Output	EBus address latch
$\overline{\text{EB\_RD}}$	Output	EBus read
$\overline{\text{EB\_WR}}$	Output	Ebus write
$\overline{\text{TOD\_CS}}$	Output	TOD chip select
$\overline{\text{EPROM\_CS}}$	Output	EPROM chip select
$\overline{\text{GENERIC\_CS}}$	Output	Generic port chip select
$\overline{\text{GENERIC\_RDY}}$	Input	Generic port ready (25 µA pull-up)

Floppy Interface: 17 pins

Signal	Type	Description
FPY_CLK32	Input	32 MHz clock for floppy DDS
FPY_CLK24	Input	24 MHz clock for floppy ASF
FPY_DENSENSE	Input	Density sense input (auxio1 register bit)
FPY_DISKCHG	Input	Disk change
FPY_WRPROT	Input	Write protect
FPY_TRACK0	Input	Track 0 indicator
FPY_RDDATA	Input	Read data
FPY_INDEX	Input	Track index
FPY_EJECT	Output	Floppy eject (ME[3] of 82077 ASF)
FPY_HEADSEL	Output	Head select
FPY_STEP	Output	Drive step pulse
FPY_DIR	Output	Head step direction
FPY_WRDATA	Output	Write data
FPY_WRGATE	Output	Write enable
FPY_DRVSEL	Output	Floppy drive select (DS[0] of 82077 ASF)
FPY_MOTEN	Output	Floppy motor enable (ME[0] of 82077 ASF)
FPY_DENSEL	Output	Density select (ME[2] or DENSEL of 82077 ASF)

Keyboard/Mouse Interface: 4 pins

Signal	Type	Description
KBD_DIN	Input	Keyboard data in
KBD_DOUT	Output	Keyboard data out
MSE_DIN	Input	Mouse data in
MSE_OUT	Output	Mouse data out

Reset Signals: 3 pins

Signal	Type	Description
$\overline{\text{POR\_RST\_IN}}$	Input	Power-up reset input
$\overline{\text{SYS\_RST\_OUT}}$	Output	System (SBus) reset output
$\overline{\text{MMC\_RST\_OUT}}$	Output	MMC reset output

Serial Interface: 19 pins

Signal	Type	Description
SER_CLK	Input	19.66 MHz serial clock
$\overline{\text{SER\_RTXC\_A}}$	Input	Receive/transmit clock A
$\overline{\text{SER\_CTS\_A}}$	Input	Clear to send A
SER_RXD_A	Input	Receive data A
$\overline{\text{SER\_DCD\_A}}$	Input	Data carrier detect A
$\overline{\text{SER\_DTR\_A}}$	Output	Data terminal ready A
SER_TXD_A	Output	Transmit data A
$\overline{\text{SER\_RTS\_A}}$	Output	Request to send A
$\overline{\text{SER\_SYNC\_A}}$	I/O	Sync IO, A
$\overline{\text{SER\_TRXC\_A}}$	I/O	Transmit clock A
$\overline{\text{SER\_RTXC\_B}}$	Input	Receive/transmit clock B
$\overline{\text{SER\_CTS\_B}}$	Input	Clear to send B
SER_RXD_B	Input	Receive data B
$\overline{\text{SER\_DCD\_B}}$	Input	Data carrier detect B
$\overline{\text{SER\_DTR\_B}}$	Output	Data terminal ready B
SER_TXD_B	Output	Transmit data B
$\overline{\text{SER\_RTS\_B}}$	Output	Request to send B
$\overline{\text{SER\_SYNC\_B}}$	I/O	Sync IO, B
$\overline{\text{SER\_TRXC\_B}}$	I/O	Transmit clock B

Interrupt Signals: 16 pins

Signal	Type	Description
MO_IRL[3:0]	Output	Module 0 encoded interrupt level
$\overline{\text{SB\_IRQ}}$[7:1]	Input	SBus interrupt requests
$\overline{\text{ENET\_IRQ}}$	Input	Ethernet interrupt request
$\overline{\text{SCSI\_IRQ}}$	Input	SCSI interrupt request
$\overline{\text{PFD}}$	Input	Power fail detect (level 15 interrupt)
$\overline{\text{MSI\_IRQ}}$	Input	MSI interrupt
$\overline{\text{MODERR\_IRQ}}$	Input	Processor level 15 interrupt (async error)

Miscellaneous System Signals: 6 pins

Signal	Type	Description
CLK_10MHZ	Input	10 MHz clock for counter/ timer block
MON_MSE_MUX	Output	Monitor/mouse mux select
POWER_OFF	Output	Power off output (to power supply)
LINK_TEST_EN	Output	T7213 link test enable
SYS_LED	Output	System LED output
$\overline{\text{IU\_ERROR}}$	Input	Processor watchdog reset/Video interrupt

JTAG Signals: 5 pins

Signal	Type	Description
JTAG_TDO	Output	JTAG test data output
JTAG_TDI	Input	JTAG test data input (100 µA pull-up)
JTAG_CLK	Input	JTAG clock
JTAG_TMS	Input	JTAG test mode select (100 µA pull-up)
JTAG_RST	Input	JTAG reset (100 µA pull-up)

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	7.0	V
V_{IN}	Input voltage	$0 \le V_{IN} \le V_{CC}$	V
I_I	Current Drain V_{CC} and GND	100	mA
T_L	Lead temperature (less than 10 second soldering)	250	°C
T_J	Operating temperature	0 to +70	°C
T_S	Storage temperature	-55 to +150	°C
P_D	Power dissipation	560	mW

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage	4.75	5.0	5.25	V
T_A	Operating Temperature	0	25	70	°C
P_D	Power dissipation	–	280	560	mW

Capacitance

Symbol	Parameter	Typ	Max	Units
C_{IN}	Input capacitance	6	–	pF
C_{OUT}	Output capacitance	6	–	pF
C_{BI}	Bidirectional pin capacitance	6	–	pF

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units
V_{IH}	Input high voltage		2.0	–	–	V
V_{IL}	Input Low voltage		–	–	0.8	V
V_{OH}	High level output voltage		4.4	4.5	–	V
V_{OL}	Low level output voltage		–	0	0.1	V
I_{IN}	Input leakage current		-10	–	10	µA
I_{OH}	High level source current (V_{OH} = 2.4 V)	I_{OH} = 2.0 mA	2	–	–	mA
		I_{OH} = 4.0 mA	4	–	–	mA
		I_{OH} = 8.0 mA	8	–	–	mA
		I_{OH} = 16.0 mA	16	–	–	mA
		I_{OH} = 24.0 mA	24	–	–	mA
I_{OL}	Low level sink current (V_{OL} = 0.4 V)	I_{OL} = -2.0 mA	2	–	–	mA
		I_{OL} = -4.0 mA	4	–	–	mA
		I_{OL} = -8.0 mA	8	–	–	mA
		I_{OL} = -16.0 mA	16	–	–	mA
		I_{OL} = -24.0 mA	24	–	–	mA
		I_{OL} = -48.0 mA	48	–	–	mA
		SCSIPAD (V_{OL} = 0.5 V)	48	–	–	mA
		SCSIPADF (V_{OL} = 0.5 V)	48	–	–	mA
I_{OZ}	Hi-Z output leakage current		-10	–	10	µA

AC Characteristics: SBus Timing

Signal #	Parameter	Conditions	Min	Max	Units
f_{SB}	SBus clock frequency		16.7	25.0	ns
1	Clock period		40.0	60.0	ns
2	Clock high		17.0	–	ns
3	Clock low		17.0	–	ns
4	Hold WRT CLK rising		0.0	–	ns
5	Setup to CLK rising		15.0	–	ns
6	Setup to CLK rising		15.0	–	ns
7	Hold WRT CLK rising [1]		–	1.0	ns
8	CLK rising to output valid	100 pF load	–	22.5	ns
9	CLK rising to output invalid	100 pF load	–	22.5	ns
10	CLK rising to output valid	100 pF load	–	22.5	ns
11	CLK rising to output invalid	100 pF load	2.5	25.0	ns
12	CLK rising to output low	100 pF load	–	22.5	ns
13	CLK rising to output high	100 pF load	–	22.5	ns

1. This is the only violation of SBus Specification B.0. No known implementation to date provides less than 1.0 ns hold time on these signals.

AC Characteristics: EBus Timing

Signal #	Parameter	Conditions	Min	Max	Units
14	Setup to CLK rising		15.0	–	ns
15	Hold WRT CLK rising		–	2.0	ns
16	CLK rising to output valid	100 pF load	–	22.5	ns
17	CLK rising to output invalid	100 pF load	–	22.5	ns
18	CLK rising to output valid	100 pF load	–	22.5	ns

AC Characteristics: Miscellaneous Timing

Signal #	Parameter	Conditions	Min	Max	Units
19	CLK rising to output valid	100 pF load	–	22.5	ns
20	10 MHz clock period [1]		50	–	ns

1. This clock must be run at 10 MHz (100 ns period) for correct software operation.

AC Characteristics: Floppy Controller Timing

Signal #	Parameter	Conditions	Min	Max	Units
21	FPY_CLK32 clock period [1]		31.3	31.3	ns
22	FPY_CLK24 clock high time		16.7	25	ns
23	FPY_CLK24 clock low time		16.7	25	ns
24	FPY_CLK24 clock period [1]		41.7	41.7	ns
25	Internal clock period (t_{CI}) [2]		62.5	250	ns
26	FPY_DIR change to FPY_STEP setup time		1.0	–	µs
27	FPY_STEP pulse width		7	8	µs
28	FPY_STEP rate [3]		1	15	ms
29	FPY_INDEX pulse width		4	–	t_{CI}
30	FPY_RDDATA pulse width		50	–	ns
31	FPY_RDDATA data rate [4]		250 K	1 M	bit/s
32	FPY_WRGATE to FPY_WRDATA setup time		250	–	ns
33	FPY_WRDATA pulse width [5]		125	500	ns

1. The NCR82077 core uses a digital data separator to read the data off of the disk. Any variation from the nominal input clock frequencies will shift the capture range of the cell.
2. NOTE 4: Internal clock period is a function of the selected data rate.

Data Rate	Frequency	Period
1 Mbs	16 MHz	62.5 ns
500 Kbs	8 MHz	125 ns
300 Kbs	4.8 MHz	208 ns
250 Kbs	4 MHz	250 ns

3. FPY_STEP Rate time is selected by a SPECIFY command. Failure to issue a specify command before issuing a Recalibrate or Seek command or implied seek will cause unpredictable results.
4. FPY_RDDATA data rate is determined by the floppy tape drive or tape drive. The values are:
   - 1 Mbs – 1.0 µs minimum
   - 500 Kbs – 2.0 µs minimum
   - 300 Kbs – 3.3 µs minimum
   - 250 Kbs – 4.0 µs minimum
5. FPY_WRDATA pulse width is based on the selected data rate. The values are 2 x t_{CI}:
   - 1 Mbs - 2 x 62.5 = 125 ns
   - 500 Kbs - 2 x 125 = 250 ns
   - 300 Kbs - 2 x 208 = 416 ns
   - 250 Kbs - 2 x 250 = 500 ns

AC Characteristics: Serial/Keyboard/Mouse Controllers Timing

Signal #	Parameter	Conditions	Min	Max	Units
34	SER_CLK low width [1]		50	–	ns
35	SER_CLK high width		50	–	ns
36	SER_CLK cycle time (t_{PC})		122	–	ns
37	$\overline{\text{SER\_RTXC}}$ width		150	–	ns
38	$\overline{\text{SER\_RTXC}}$ cycle time		4	–	t_{PC}
39	$\overline{\text{SER\_TRXC}}$ width		150	–	ns
40	$\overline{\text{SER\_TRXC}}$ cycle time		4	–	t_{PC}
41	$\overline{\text{SER\_DCD}}$ or $\overline{\text{SER\_CTS}}$ width		200	–	ns
42	$\overline{\text{SER\_SYNC}}$ width		200	–	ns
43	SER_RXD to $\overline{\text{SER\_RTXC}}$ setup time		0	–	ns
44	SER_RXD to $\overline{\text{SER\_RTXC}}$ hold time		150	–	ns
45	$\overline{\text{SER\_SYNC}}$ to $\overline{\text{SER\_RTXC}}$ setup time		-200	–	ns
46	$\overline{\text{SER\_SYNC}}$ to $\overline{\text{SER\_RTXC}}$ hold time		5	–	t_{PC}
47	$\overline{\text{SER\_TRXC}}$ to SER_TXD delay		–	200	ns
48	SER_TXD to $\overline{\text{SER\_TRXC}}$ delay		–	200	ns

1. The input SER_CLK is used to clock the serial controllers and the keyboard/mouse controller. The timing numbers in this section apply to both of these controllers.

TIMING DIAGRAMS

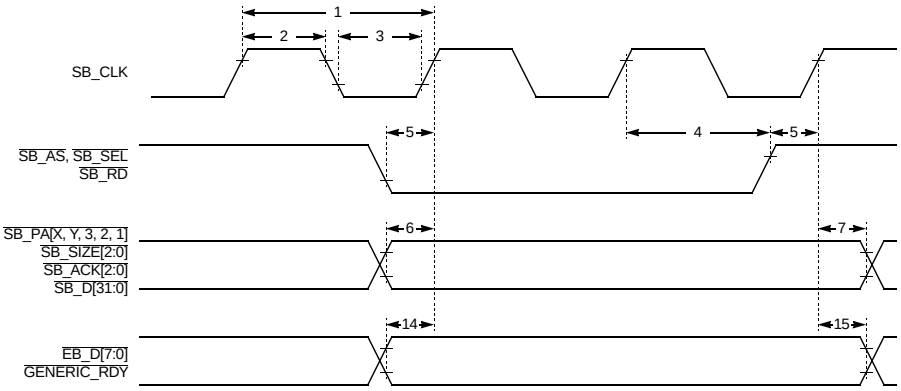

Figure 4. SBus/EBus Input Timing

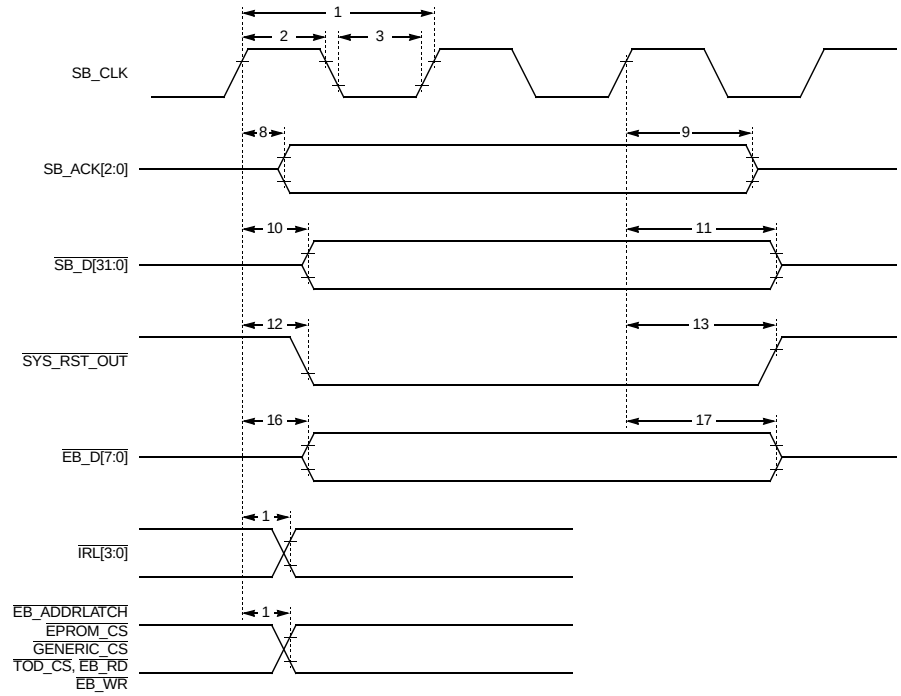

Figure 5. SBus/EBus Output Timing

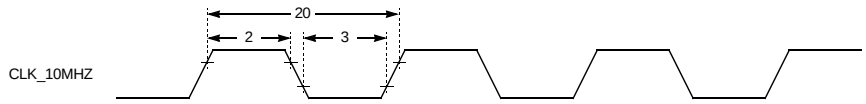

Figure 6. Counter/Timer Input Clock

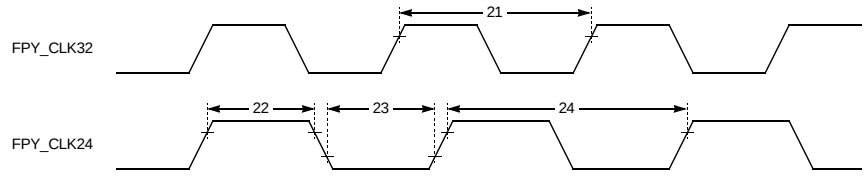

Figure 7. Floppy Controller Clock Inputs

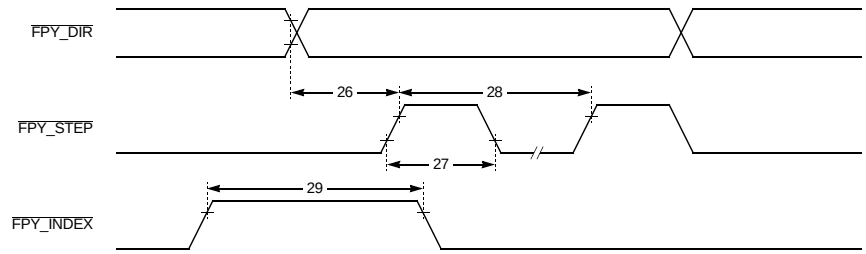

Figure 8. Floppy Drive Interface Timing

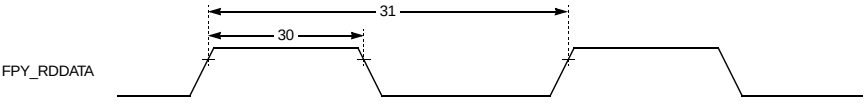

Figure 9. Floppy Read Data

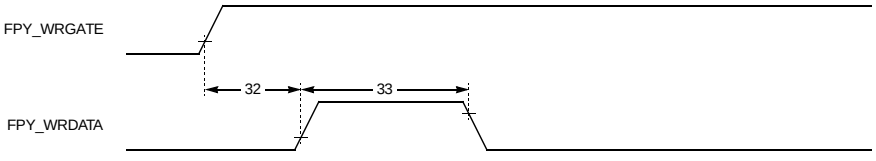

Figure 10. Floppy Write Data

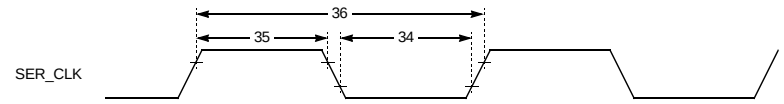

Figure 11. Serial/Keyboard/Mouse Clock Input

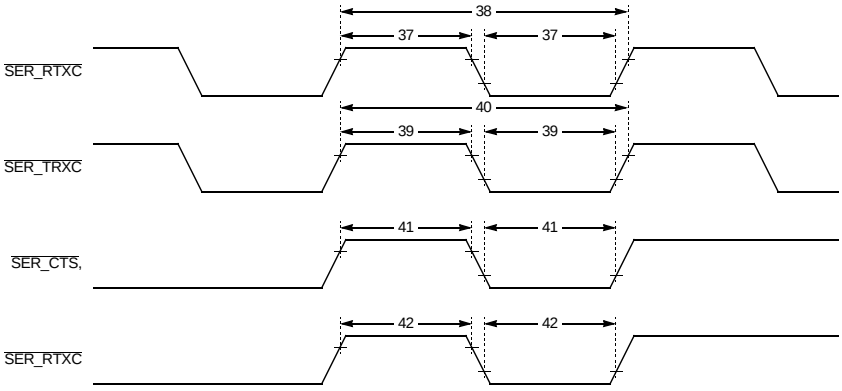

Figure 12. Serial Pulse Widths

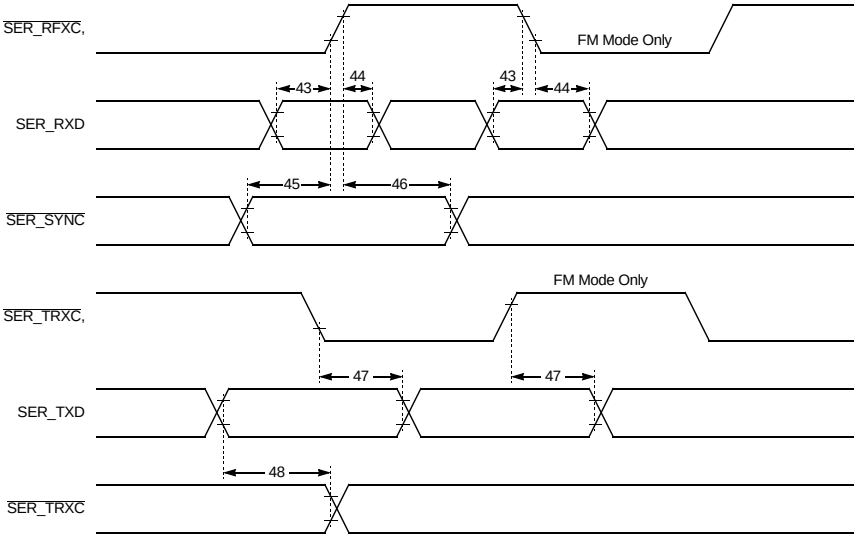

Figure 13. Serial Data Timing

STP2001QFP

Slave I/O
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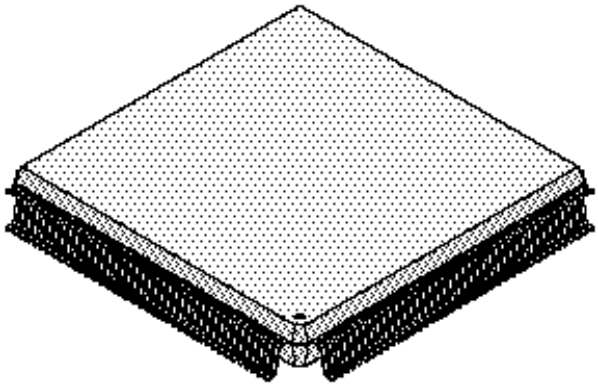
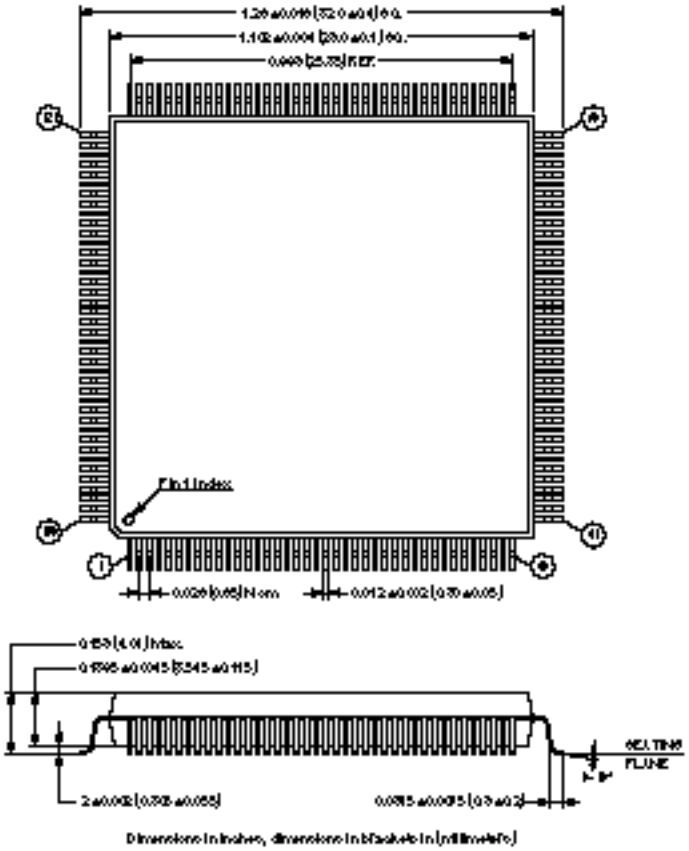
PACKAGE INFORMATION

160-Pin PQFP Pin Assignment

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	ENET_IRQ	33	SB_PA[y]	65	SB_D[19]	97	SER_DTR_B	129	TOD_CS
2	SCSI_IRQ	34	SB_PA[x]	66	SB_D[20]	98	SER_SYNC_B	130	EB_RD
3	FPY_DENSENSE	35	SB_PA[w]	67	SB_D[21]	99	KBD_DOUT	131	EB_WR
4	FPY_DISKCHG	36	SB_PA[v]	68	VCC	100	MSE_OUT	132	EB_D[0]
5	FPY_WRPROT	37	GND	69	SB_D[22]	101	POWER_OFF	133	GND
6	FPY_TRACK0	38	CHIP_SEL	70	SB_D[23]	102	JTAG_TDO	134	EB_D[1]
7	FPY_RDDATA	39	SB_RD	71	SB_D[24]	103	VCC	135	EB_D[2]
8	FPY_INDEX	40	SB_AS	72	SB_D[25]	104	SER_CLK	136	EB_D[3]
9	FPY_CLK24	41	SB_SEL	73	SB_D[26]	105	SER_RTXC_B	137	EB_D[4]
10	GND	42	SB_D[0]	74	SB_D[27]	106	SER_CTS_B	138	EB_D[5]
11	FPY_EJECT	43	SB_D[1]	75	GND	107	GND	139	EB_D[6]
12	FPY_HEADSEL	44	SB_D[2]	76	SB_D[28]	108	SER_RXD_B	140	VCC
13	FPY_STEP	45	SB_D[3]	77	SB_D[29]	109	SER_DCD_B	141	EB_D[7]
14	FPY_DIR	46	GND	78	SB_D[30]	110	SER_RTXC_A	142	EB_ADDRLATCH
15	GND	47	SB_D[4]	79	SB_D[31]	111	SER_CTS_A	143	SYS_RST_OUT
16	FPY_WRDATA	48	SB_D[5]	80	SB_SIZ[2]	112	VCC	144	MMC_RST_OUT
17	FPY_WRGATE	49	SB_D[6]	81	SB_SIZ[1]	113	SER_RXD_A	145	M0_IRL[0]
18	FPY_DRVSEL	50	SB_D[7]	82	SB_SIZ[0]	114	SER_DCD_A	146	M0_IRL[1]
19	VCC	51	SB_D[8]	83	GND	115	LINK_TEST_EN	147	GND
20	FPY_MOTEN	52	SB_D[9]	84	SB_ACK[2]	116	MSE_DIN	148	M0_IRL[2]
21	FPY_DENSEL	53	VCC	85	SB_ACK[1]	117	KBD_DIN	149	M0_IRL[3]
22	VCC	54	SB_D[10]	86	SB_ACK[0]	118	MON_MSE_MUX	150	CLK_10MHZ
23	FPY_CLK32	55	SB_D[11]	87	SER_DTR_A	119	JTAG_TDI	151	SB_IRQ[1]
24	SB_PA[0]	56	SB_D[12]	88	SER_TXD_A	120	JTAG_CLK	152	SB_IRQ[2]
25	SB_PA[1]	57	SB_D[13]	89	GND	121	JTAG_TMS	153	SB_IRQ[3]
26	SB_PA[2]	58	SB_D[14]	90	SER_RTS_A	122	JTAG_RST	154	SB_IRQ[4]
27	GND	59	SB_D[15]	91	SER_SYNC_A	123	GENERIC_RDY	155	SB_IRQ[5]
28	SB_PA[3]	60	GND	92	SER_TRXC_A	124	IU_ERROR	156	SB_IRQ[6]
29	SB_PA[4]	61	SB_CLK	93	SER_TXD_B	125	POR_RST_IN	157	SB_IRQ[7]
30	SB_PA[16]	62	SB_D[16]	94	SER_TRXC_B	126	GENERIC_CS	158	PFD
31	SB_PA[z]	63	SB_D[17]	95	VCC	127	SYS_LED	159	MODERR_IRQ
32	VCC	64	SB_D[18]	96	SER_RTS_B	128	EPROM_CS	160	MSI_IRQ

160-Pin PQFP Package Dimensions





Dimensions in inches, dimensions in brackets in [millimeters]

Slave I/O
Integrated SBus Interface Slave I/O Controller

ORDERING INFORMATION

Part Number	Description
STP2001QFP	160-Pin Plastic Leaded Chip Carrier (PQFP)

Document Part Number: STP2001