

PCA9548A Low Voltage 8-Channel I²C Switch With Reset

1 Features

- 1-of-8 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Active-Low Reset Input
- Three Hardware Address Pins for Use of up to Eight PCA9548A Devices on the I²C Bus
- Channel Selection Via I²C Bus
- Power-Up with All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

3 Description

The PCA9548A has eight bidirectional translating switches that can be controlled via the I²C bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register.

The system master can reset the PCA9548A in the event of a timeout or other improper operation by asserting a low in the **RESET** input. Similarly, the power-on reset deselected all channels and initializes the I²C/SMBus state machine. Asserting **RESET** causes the same reset/initialization to occur without powering down the part.

Device Information⁽¹⁾

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
PCA9548A	TSSOP (24)	7.80 mm x 4.40 mm
	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

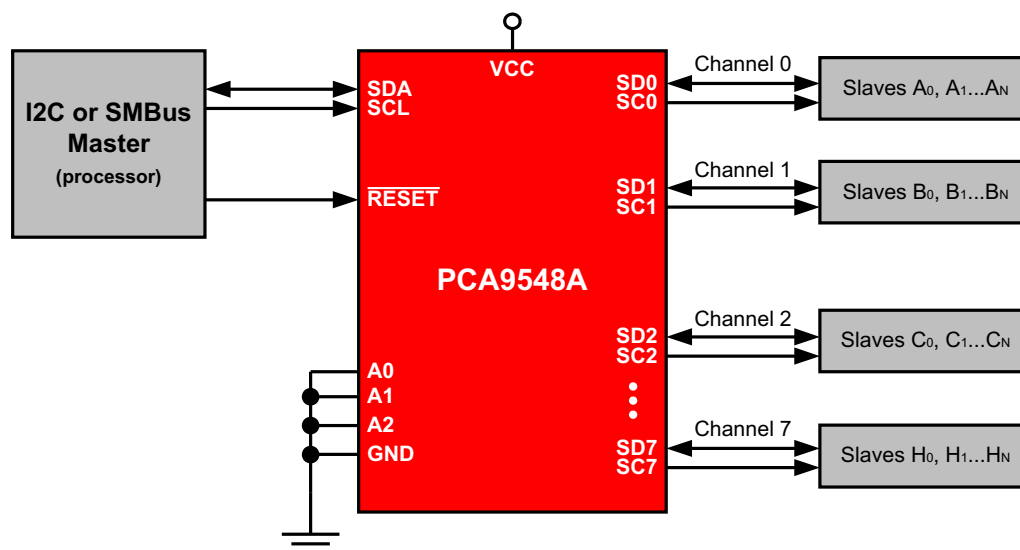


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

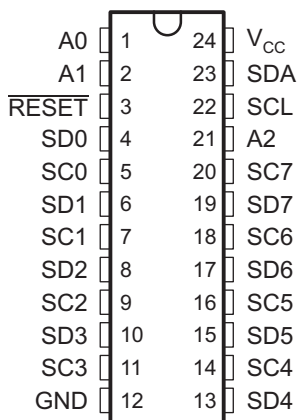
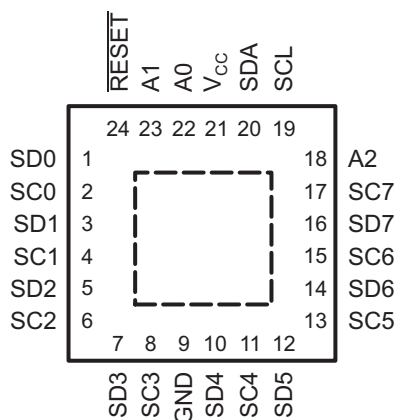
Changes from Revision D (June 2014) to Revision E	Page
• Changed front page image	1
• Added <i>Thermal Information</i>	4
• Added <i>Layout Example</i>	21

Changes from Revision C (June 2007) to Revision D	Page
• Added $\overline{\text{RESET}}$ Errata section	11
• Updated Typical Application schematic	17
• Added Power-On Reset Errata section	20

5 Description (continued)

The pass gates of the switches are constructed so that the V_{CC} pin can be used to limit the maximum high voltage, which is passed by the PCA9548A. This allows the use of different bus voltages on each pair, so that 1.8-V or 2.5-V or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5-V tolerant.

6 Pin Configuration and Functions

**DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)**

**RGE PACKAGE
(TOP VIEW)**


Pin Functions

NAME	PIN		DESCRIPTION
	NO.		
	DW, DB, TPW, AND DGV	QFN (RGE)	
A0	1	22	Address input 0. Connect directly to V_{CC} or ground.
A1	2	23	Address input 1. Connect directly to V_{CC} or ground.
RESET	3	24	Active-low reset input. Connect to V_{CC} through a pull-up resistor, if not used.
SD0	4	1	Serial data 0. Connect to V_{CC} through a pull-up resistor.
SC0	5	2	Serial clock 0. Connect to V_{CC} through a pull-up resistor.
SD1	6	3	Serial data 1. Connect to V_{CC} through a pull-up resistor.
SC1	7	4	Serial clock 1. Connect to V_{CC} through a pull-up resistor.
SC2	8	5	Serial data 2. Connect to V_{CC} through a pull-up resistor.
SC2	9	6	Serial clock 2. Connect to V_{CC} through a pull-up resistor.
SD3	10	7	Serial data 3. Connect to V_{CC} through a pull-up resistor.
SC3	11	8	Serial clock 3. Connect to V_{CC} through a pull-up resistor.
GND	12	9	Ground
SD4	13	10	Serial data 4. Connect to V_{CC} through a pull-up resistor.
SC4	14	11	Serial clock 4. Connect to V_{CC} through a pull-up resistor.
SD5	15	12	Serial data 5. Connect to V_{CC} through a pull-up resistor.
SC5	16	13	Serial clock 5. Connect to V_{CC} through a pull-up resistor.
SD6	17	14	Serial data 6. Connect to V_{CC} through a pull-up resistor.
SC6	18	15	Serial clock 6. Connect to V_{CC} through a pull-up resistor.
SD7	19	16	Serial data 7. Connect to V_{CC} through a pull-up resistor.
SC7	20	17	Serial clock 7. Connect to V_{CC} through a pull-up resistor.
A2	21	18	Address input 2. Connect directly to V_{CC} or ground.
SCL	22	19	Serial clock bus. Connect to V_{CC} through a pull-up resistor.
SDA	23	20	Serial data bus. Connect to V_{CC} through a pull-up resistor.
V_{CC}	24	21	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
V _I	Input voltage ⁽²⁾	-0.5	7	V
I _I	Input current		±20	mA
I _O	Output current		±25	mA
I _{CC}	Supply current		±100	mA
T _{stg}	Storage temperature range	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	5.5	V
V _{IH}	High-level input voltage	SCL, SDA	0.7 × V _{CC}	6
		A2–A0, $\overline{\text{RESET}}$	0.7 × V _{CC}	V _{CC} + 0.5
V _{IL}	Low-level input voltage	SCL, SDA	-0.5	0.3 × V _{CC}
		A2–A0, $\overline{\text{RESET}}$	-0.5	0.3 × V _{CC}
T _A	Operating free-air temperature	-40	85	°C

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	PCA9548A					UNIT	
	DB	DGV	DW	PW	RGE		
	24 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	89.1	99.6	73.2	100.6	49.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.1	31.1	41.3	46.2	53.2	
R _{θJB}	Junction-to-board thermal resistance	46.6	53.1	42.9	54.5	26.4	
ψ _{JT}	Junction-to-top characterization parameter	18.5	0.9	15.3	6.8	1.7	
ψ _{JB}	Junction-to-board characterization parameter	46.3	52.6	42.6	54.0	26.4	
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	8.5	

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

 $V_{CC} = 2.3\text{ V to }3.6\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{POR}	Power-on reset voltage ⁽²⁾	No load, $V_I = V_{CC}$ or GND		V_{POR}	1.6	2.1		V
$V_{O(sw)}$	Switch output voltage	$V_{I(sw)} = V_{CC}$, $I_{SWout} = -100\ \mu\text{A}$	5 V	3.6				V
			4.5 V to 5.5 V	2.6	4.5			
			3.3 V	1.9				
			3 V to 3.6 V	1.6	2.8			
			2.5 V	1.5				
I_{OL}	SDA	$V_{OL} = 0.4\text{ V}$	2.3 V to 5.5 V	3	6		mA	
		$V_{OL} = 0.6\text{ V}$		6	9			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			± 1	μA	
	SC7–SC0, SD7–SD0					± 1		
	A2–A0					± 1		
	RESET					± 1		
I_{CC}	Operating mode	$f_{SCL} = 400\text{ kHz}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	50	80	μA	
				3.6 V	20	35		
				2.7 V	11	20		
		$f_{SCL} = 100\text{ kHz}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	9	30		
				3.6 V	6	15		
				2.7 V	4	8		
	Standby mode	Low inputs	$V_I = \text{GND}$, $I_O = 0$	5.5 V	0.2	1		
				3.6 V	0.1	1		
		High inputs	$V_I = V_{CC}$, $I_O = 0$	5.5 V	0.2	1		
				3.6 V	0.1	1		
ΔI_{CC}	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V	3	20	μA	
					SCL or SDA input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND	3		20
C_i	A2–A0	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V	4	5	pF		
	RESET			4	5			
	SCL			20	28			
$C_{iO(off)}$ ⁽³⁾	SDA	$V_I = V_{CC}$ or GND, Switch OFF	2.3 V to 5.5 V	20	28	pF		
	SC7–SC0, SD7–SD0			5.5	7.5			
R_{ON}	Switch-on resistance	$V_O = 0.4\text{ V}$, $I_O = 15\text{ mA}$	4.5 V to 5.5 V	4	10	20	Ω	
			3 V to 3.6 V	5	12	30		
			2.3 V to 2.7 V	7	15	45		

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), $T_A = 25^\circ\text{C}$.

(2) The power-on reset circuit resets the I²C bus logic with $V_{CC} < V_{POR}$. V_{CC} must be lowered to 0.2 V to reset the device.

(3) $C_{iO(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channel(s) are ON.

7.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	
f _{scl}	I ² C clock frequency	0	100	0	400	kHz
t _{sch}	I ² C clock high time	4		0.6		μs
t _{scl}	I ² C clock low time	4.7		1.3		μs
t _{sp}	I ² C spike time		50		50	ns
t _{sds}	I ² C serial-data setup time	250		100		ns
t _{sdh}	I ² C serial-data hold time	0 ⁽¹⁾		0 ⁽¹⁾		μs
t _{icr}	I ² C input rise time		1000	20 + 0.1C _b ⁽²⁾	300	ns
t _{icf}	I ² C input fall time		300	20 + 0.1C _b ⁽²⁾	300	ns
t _{ocf}	I ² C output (SDn) fall time (10-pF to 400-pF bus)		300	20 + 0.1C _b ⁽²⁾	300	ns
t _{buf}	I ² C bus free time between stop and start	4.7		1.3		μs
t _{sts}	I ² C start or repeated start condition setup	4.7		0.6		μs
t _{sth}	I ² C start or repeated start condition hold	4		0.6		μs
t _{sps}	I ² C stop condition setup	4		0.6		μs
t _{vdL(Data)}	Valid-data time (high to low) ⁽³⁾	SCL low to SDA output low valid		1	1	μs
t _{vdH(Data)}	Valid-data time (low to high) ⁽³⁾	SCL low to SDA output high valid		0.6	0.6	μs
t _{vd(ack)}	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1	1	μs
C _b	I ² C bus capacitive load		400		400	pF

- (1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal), to bridge the undefined region of the falling edge of SCL.
- (2) C_b = total bus capacitance of one bus line in pF
- (3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see Figure 2)

7.7 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pd} ⁽¹⁾	Propagation delay time	R _{ON} = 20 Ω, C _L = 15 pF	SDA or SCL	SDn or SCn	0.3	ns
		R _{ON} = 20 Ω, C _L = 50 pF			1	
t _{rst} ⁽²⁾	RESET time (SDA clear)	RESET	SDA	500		ns

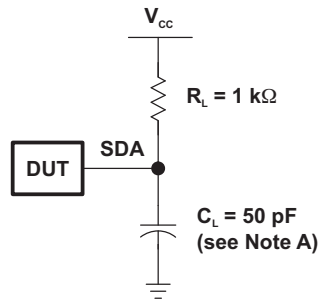
- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- (2) t_{rst} is the propagation delay measured from the time the RESET pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

7.8 Reset Timing Requirements

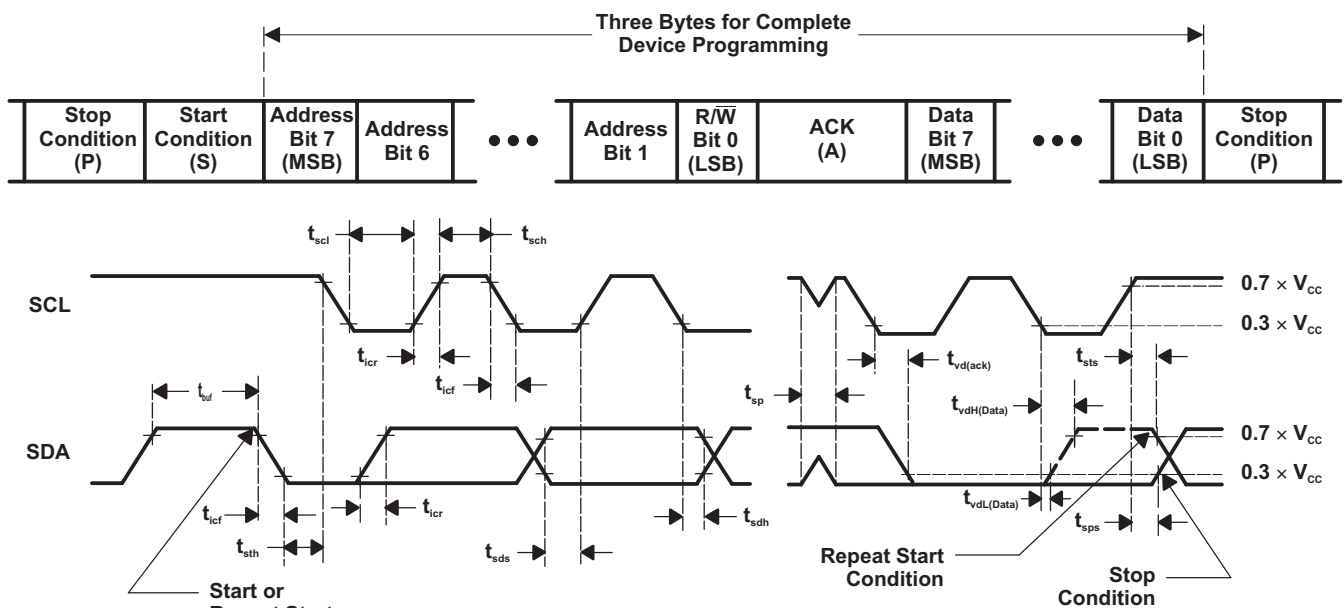
over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t _{W(L)}	Pulse duration, RESET low	6		ns
t _{REC(STA)}	Recovery time from RESET to start	0		ns

8 Parameter Measurement Information



SDA LOAD CONFIGURATION

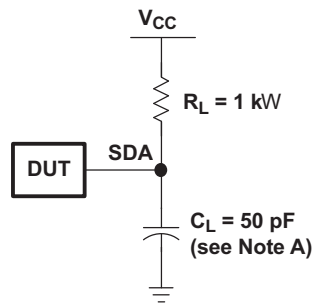
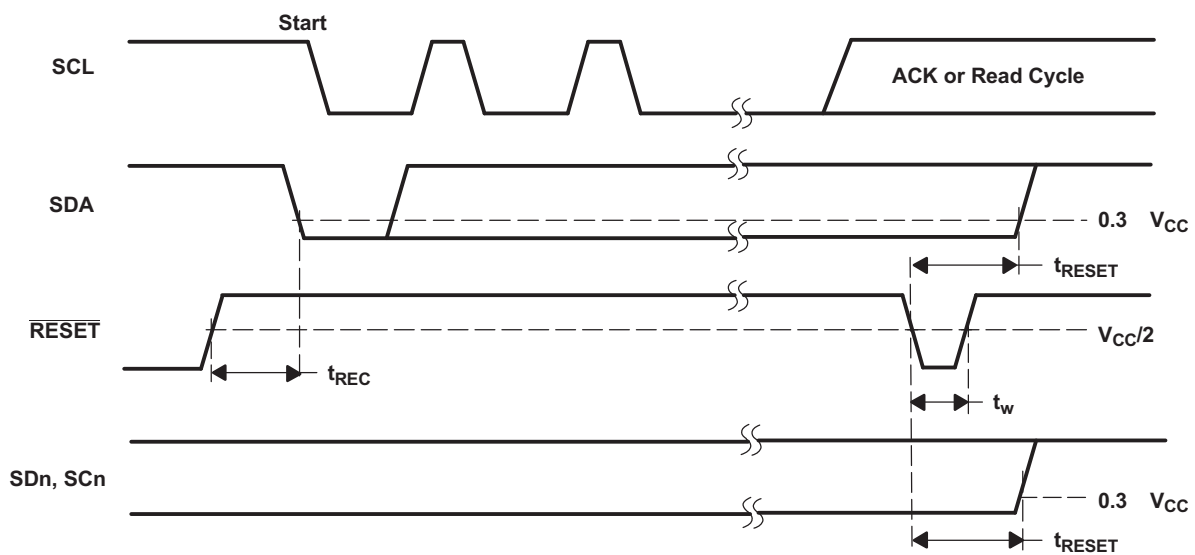


VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I ² C address
2, 3	P-port data

- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. Not all parameters and waveforms are applicable to all devices.

Figure 1. I²C Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

SDA LOAD CONFIGURATION


- C_L includes probe and jig capacitance.
- All inputs are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f \leq 30\text{ ns}$.
- I/Os are configured as inputs.
- Not all parameters and waveforms are applicable to all devices.

Figure 2. Reset Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The PCA9548A is a 8-channel, bidirectional translating I²C switch. The master SCL/SDA signal pair is directed to eight channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the eight channels.

The device offers an active-low $\overline{\text{RESET}}$ input which resets the state machine and allows the PCA9548A to recover should one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC} , also known as a power-on reset (POR). Both the $\overline{\text{RESET}}$ function and a POR will cause all channels to be deselected.

The connections of the I²C data path are controlled by the same I²C master device that is switched to communicate with multiple I²C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 pins), a single 8-bit control register is written to or read from to determine the selected channels.

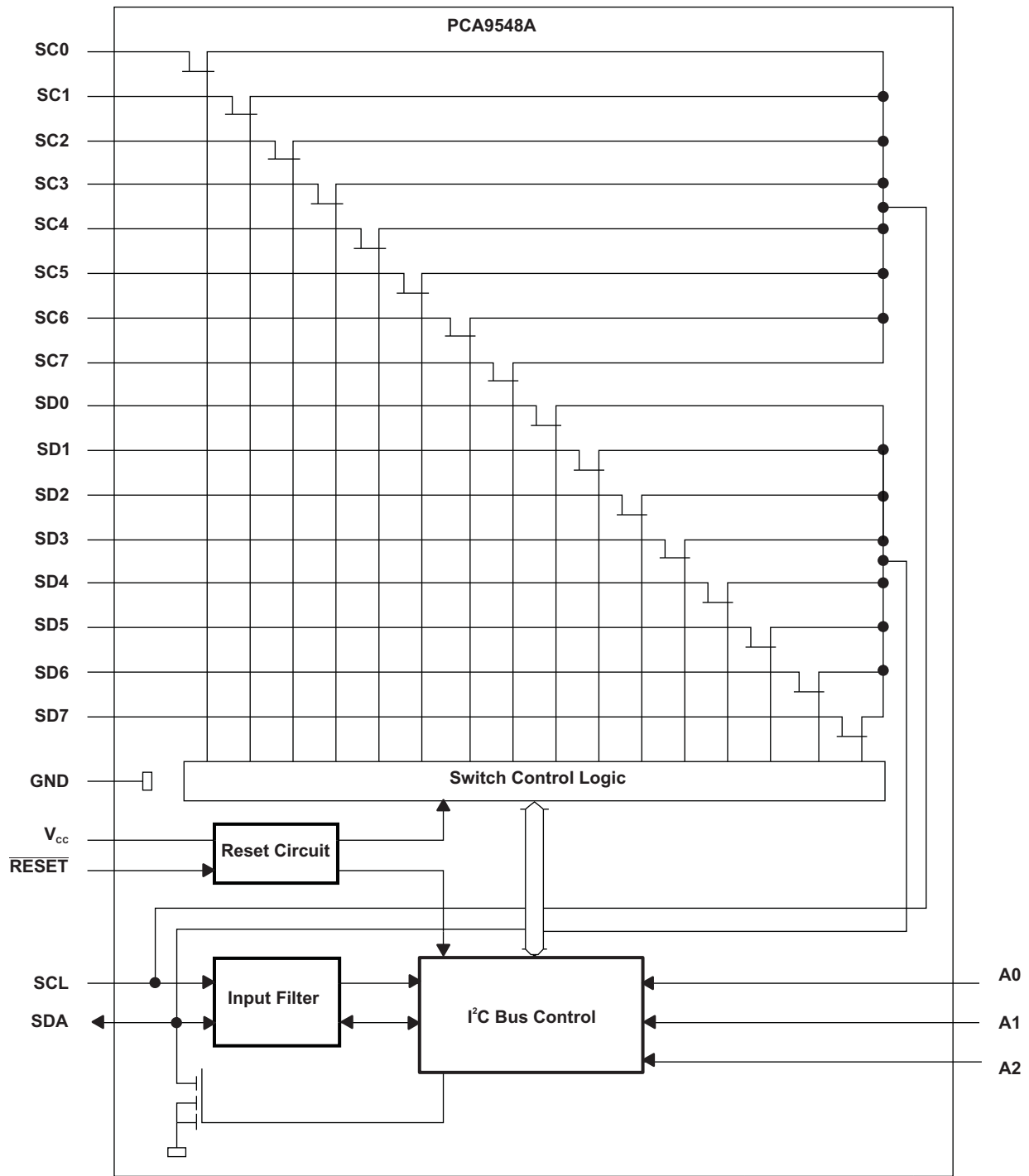
The PCA9548A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

PCA9548A

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9.2 Functional Block Diagram



9.3 Feature Description

The PCA9548A is an 8-channel, bidirectional translating switch for I²C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9548A features I²C control using a single 8-bit control register in which each bit controls the enabling and disabling for one of the 8 switch channels of I²C data flow. Depending on the application, voltage translation of the I²C bus can also be achieved using the PCA9548A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I²C bus enters a fault state, the PCA9548A can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

9.4 Device Functional Modes

9.4.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL} , the PCA9548A resets its registers and I²C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

9.4.1.1 $\overline{\text{RESET}}$ Errata

If RESET voltage set higher than VCC, current will flow from RESET pin to VCC pin.

System Impact

VCC will be pulled above its regular voltage level

System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC

9.4.2 Power-On Reset

When power (from 0 V) is applied to V_{CC} , an internal power-on reset holds the PCA9548A in a reset condition until V_{CC} has reached V_{POR} . At that point, the reset condition is released and the PCA9548A registers and I²C state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{POR} and then back up to the operating voltage for a power-reset cycle.

Refer to the [Power-On Reset Errata](#) section.

9.5 Programming

9.5.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 3](#)). After the start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see [Figure 4](#)).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 3](#)).

Programming (continued)

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 5](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

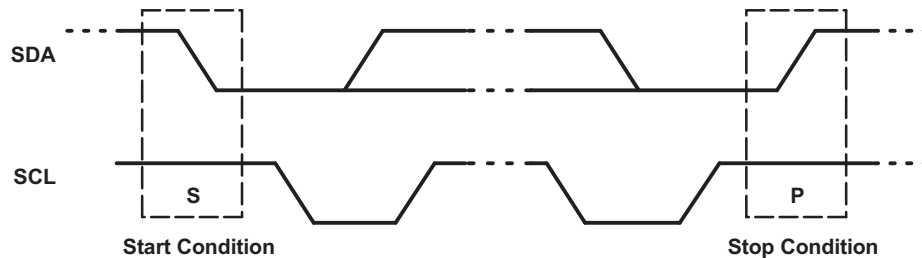


Figure 3. Definition of Start and Stop Conditions

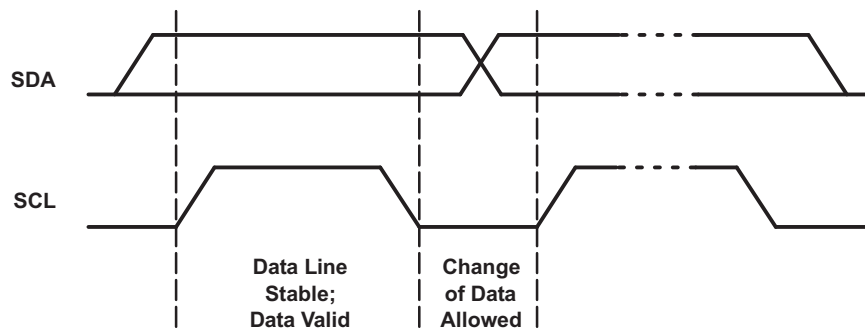


Figure 4. Bit Transfer

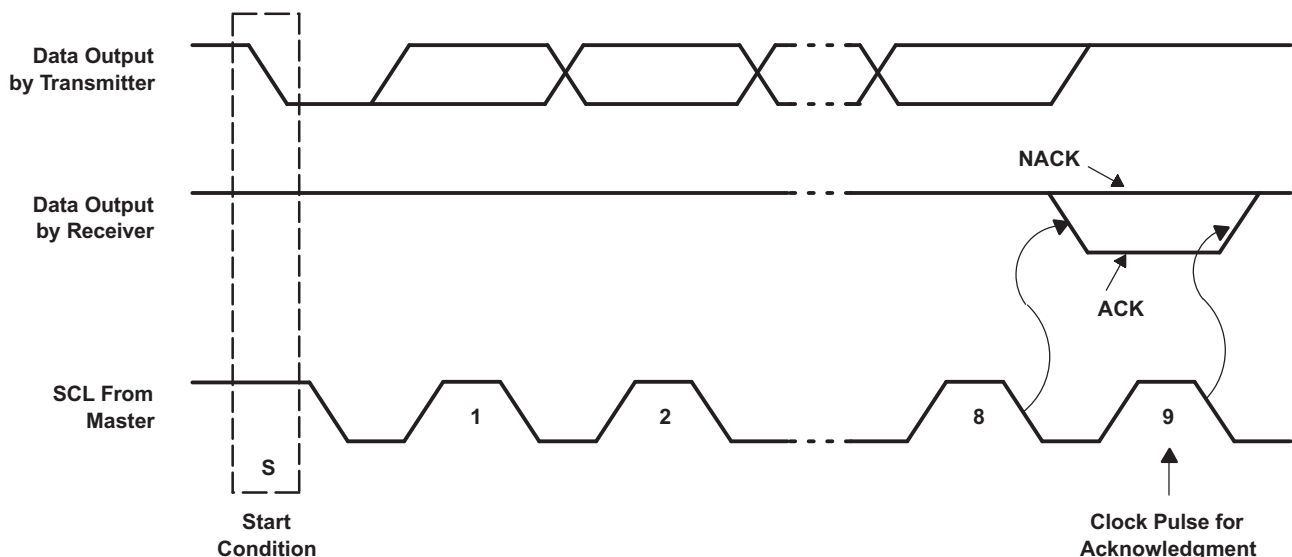


Figure 5. Acknowledgment on I²C Bus

9.6 Register Map

9.6.1 Device Address

Figure 6 shows the address byte of the PCA9548A.

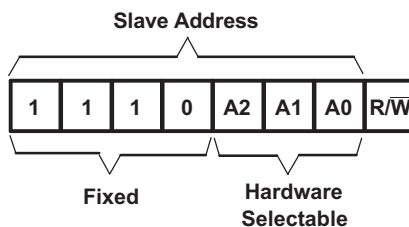


Figure 6. PCA9548A Address

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

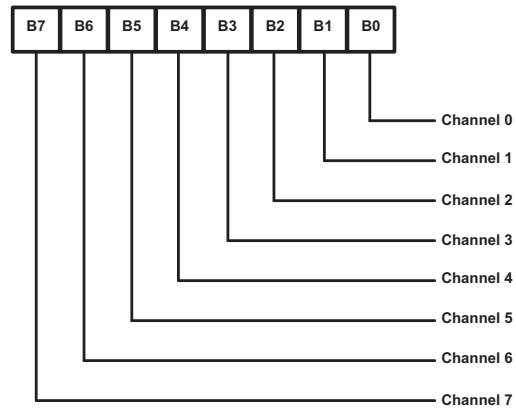
Table 1. Address Reference

INPUTS			I ² C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

9.6.2 Control Register

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9548A (see Figure 7). This register can be written and read via the I²C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the PCA9548A, it saves the last byte received.

Channel Selection Bits (Read/Write)


Figure 7. Control Register
Table 2. Command Byte Definition

CONTROL REGISTER BITS								COMMAND
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	X	0	Channel 1 disabled
							1	Channel 1 enabled
X	X	X	X	X	X	X	0	Channel 2 disabled
							1	Channel 2 enabled
X	X	X	X	X	X	X	0	Channel 3 disabled
							1	Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

9.6.3 Bus Transactions

Data is exchanged between the master and PCA9548A through write and read commands.

9.6.3.1 Writes

Data is transmitted to the PCA9548A by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 6 for device address). The command byte is sent after the address and determines which SCn/SDn channel receives the data that follows the command byte (see Figure 8). There is no limitation on the number of data bytes sent in one write transmission.

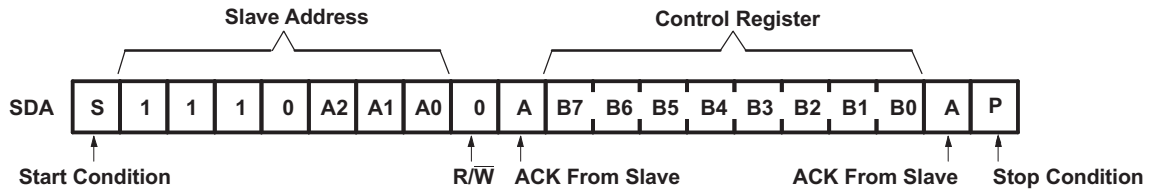


Figure 8. Write to Control Register

9.6.3.2 Reads

The bus master first must send the PCA9548A address with the LSB set to a logic 1 (see Figure 6 for device address). The command byte is sent after the address and determines which SCn/SDn channel is accessed. After a restart, the device address is sent again, but this time, the LSB is set to a logic 1. Data from the SCn/SDn channel defined by the command byte then is sent by the PCA9548A (see Figure 9). After a restart, the value of the SCn/SDn channel defined by the command byte matches the SCn/SDn channel being accessed when the restart occurred. Data is clocked into the SCn/SDn channel on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

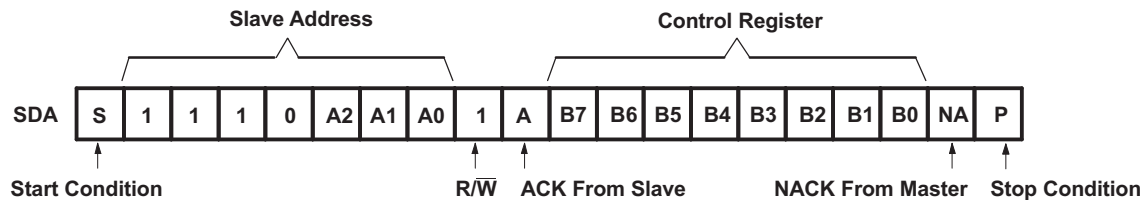


Figure 9. Read From Control Register

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Applications of the PCA9548A will contain an I²C (or SMBus) master device and up to eight I²C slave devices. The downstream channels are ideally used to resolve I²C slave address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I²C master can move on and read the next channel.

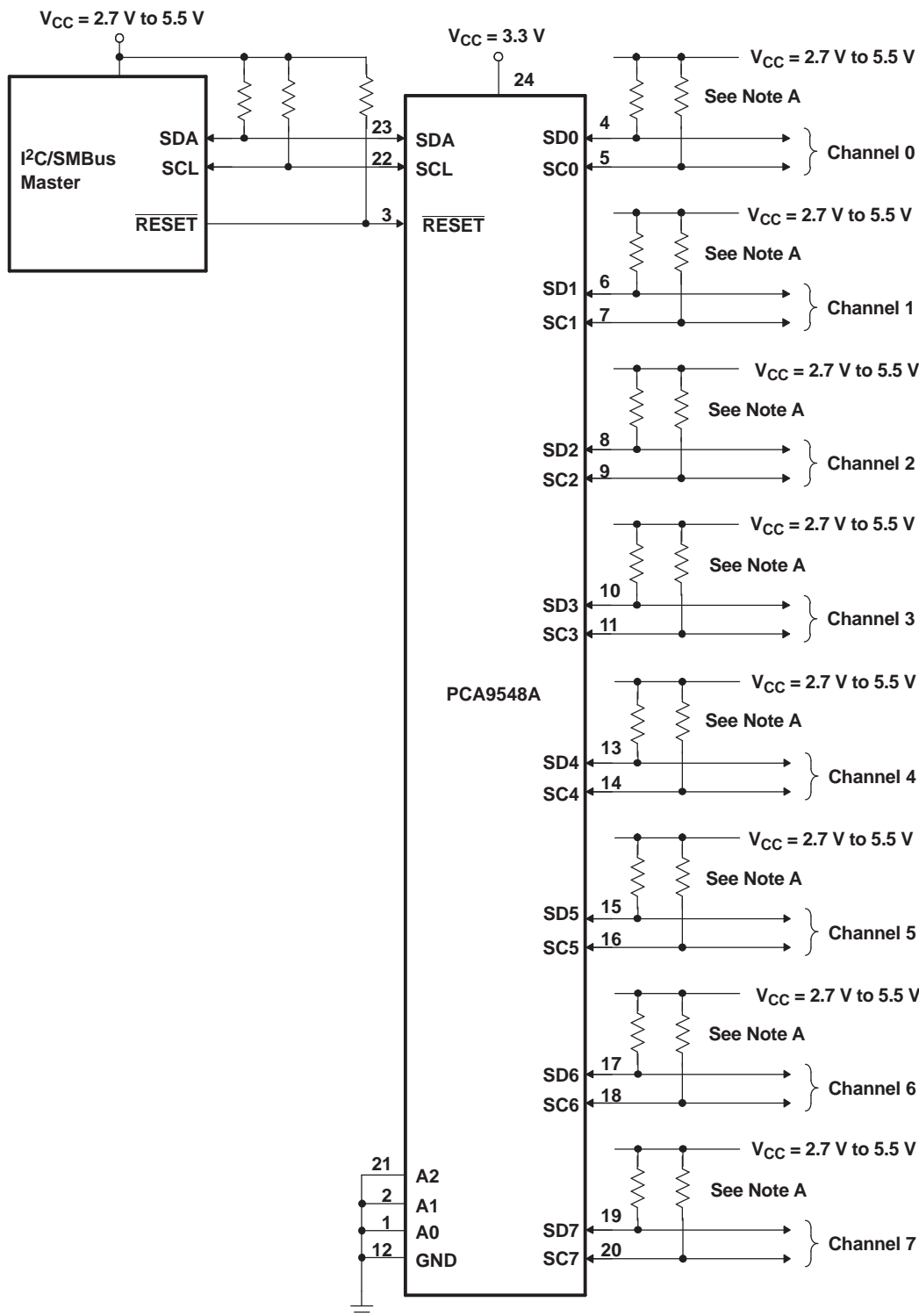
In an application where the I²C bus will contain many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See [Design Requirements](#) and [Detailed Design Procedure](#)).

10.2 Typical Application

A typical application of the PCA9548A will contain 1 or many separate data pull-up voltages, V_{CC} , one for the master device and one for each of the selectable slave channels, 0 through 7. In the event where the master device and all slave devices operate at the same voltage, then the VCC pin can be connected to this supply voltage. In an application where voltage translation is necessary, additional design requirements must be considered (See [Design Requirements](#)).

[Figure 10](#) shows an application in which the PCA9548A can be used.

Typical Application (continued)



A. Pin numbers shown are for the PW and RTW packages.

Figure 10. PCA9548A Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

The A0, A1, and A2 pins are hardware selectable to control the slave address of the PCA9548A. These pins may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p .

The pass-gate transistors of the PCA9548A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I²C bus to another.

Figure 11 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the PCA9548A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 11, $V_{pass(max)}$ is 2.7 V when the PCA9548A supply voltage is 4 V or lower, so the PCA9548A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 10).

10.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of the reference voltage of the specific I²C channel (V_{DPUX}), $V_{OL(max)}$, and I_{OL} :

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

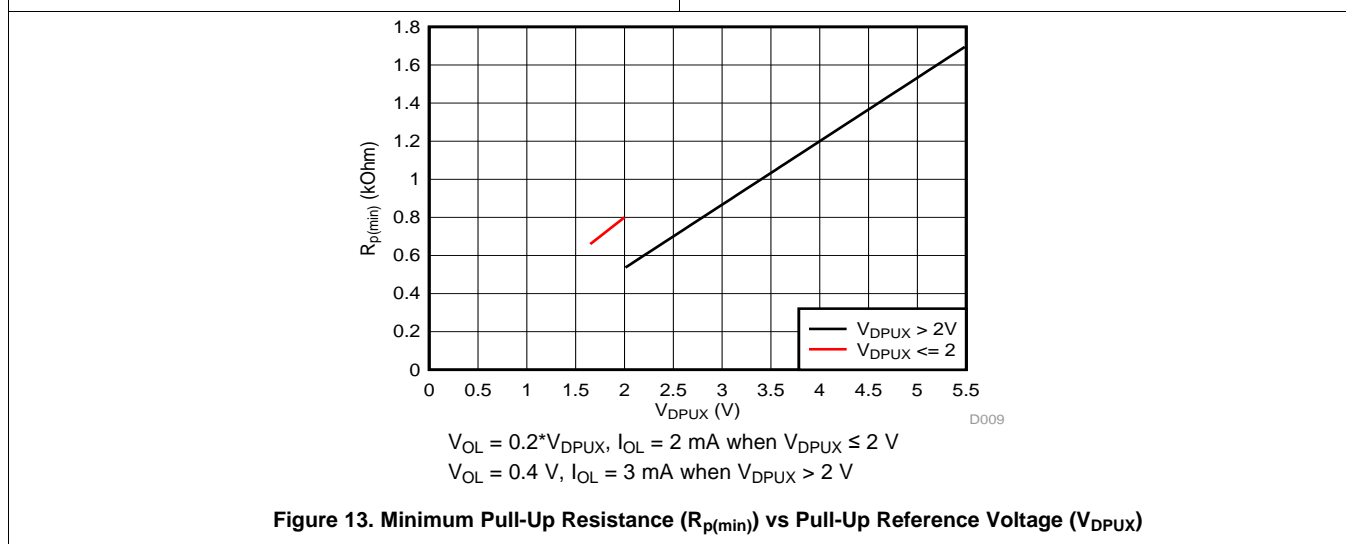
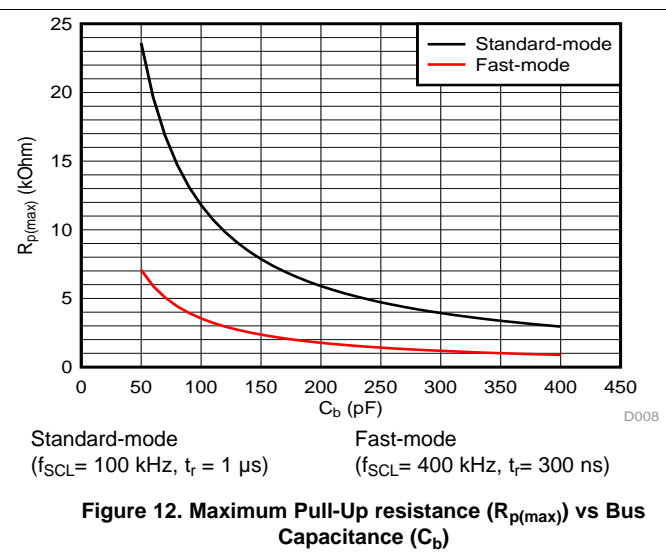
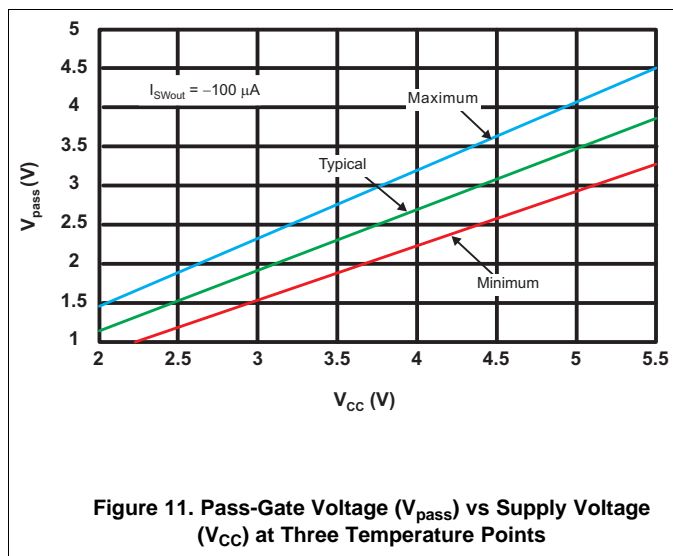
The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, C_b :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9548A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

Typical Application (continued)

10.2.3 PCA9548A Application Curves

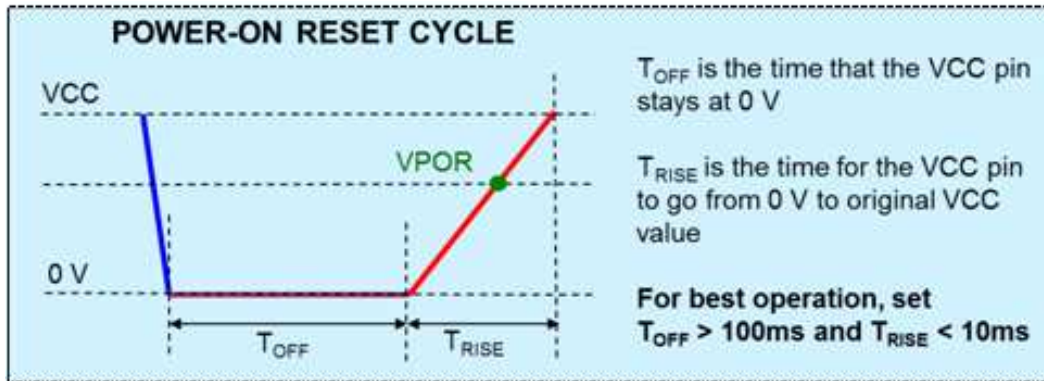


11 Power Supply Recommendations

The operating power-supply voltage range of the PCA9548A is 2.3 V to 5.5 V applied at the VCC pin. When the PCA9548A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I²C bus logic is initialized properly.

11.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

12 Layout

12.1 Layout Guidelines

For PCB layout of the PCA9548A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPU0} and V_{DPU0} - V_{DPU7} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SCn and SDn) should be as short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

12.2 Layout Example

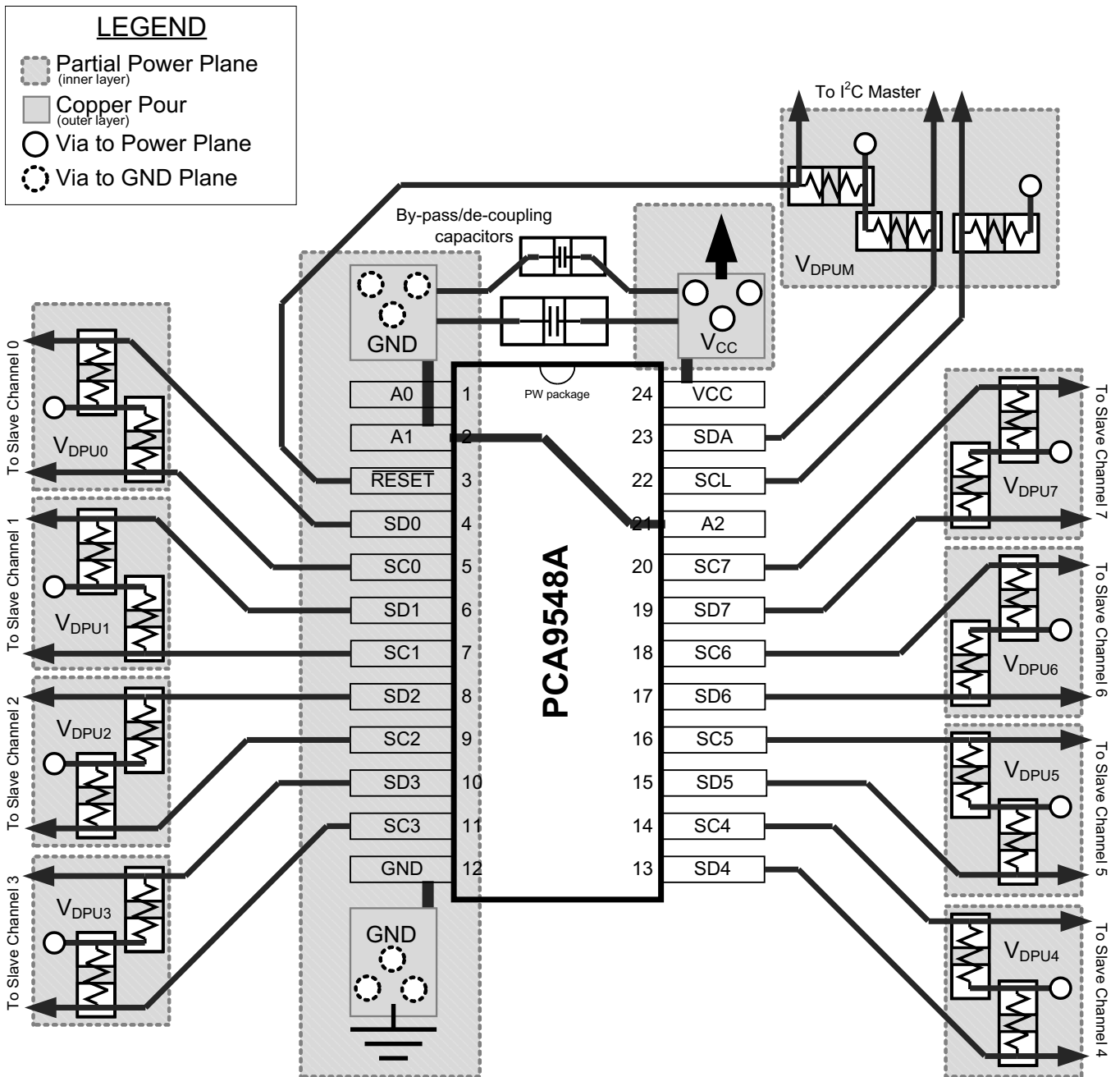


Figure 14. Layout Example

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9548ADB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	Samples
PCA9548ADBG4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	Samples
PCA9548ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	Samples
PCA9548ADGV	NRND	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		
PCA9548ADGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	Samples
PCA9548ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A	Samples
PCA9548ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A	Samples
PCA9548ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A	Samples
PCA9548APW	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	
PCA9548APWR	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	
PCA9548APWRG4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A	
PCA9548ARGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD548A	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9548ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9548ADGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9548ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9548APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9548ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

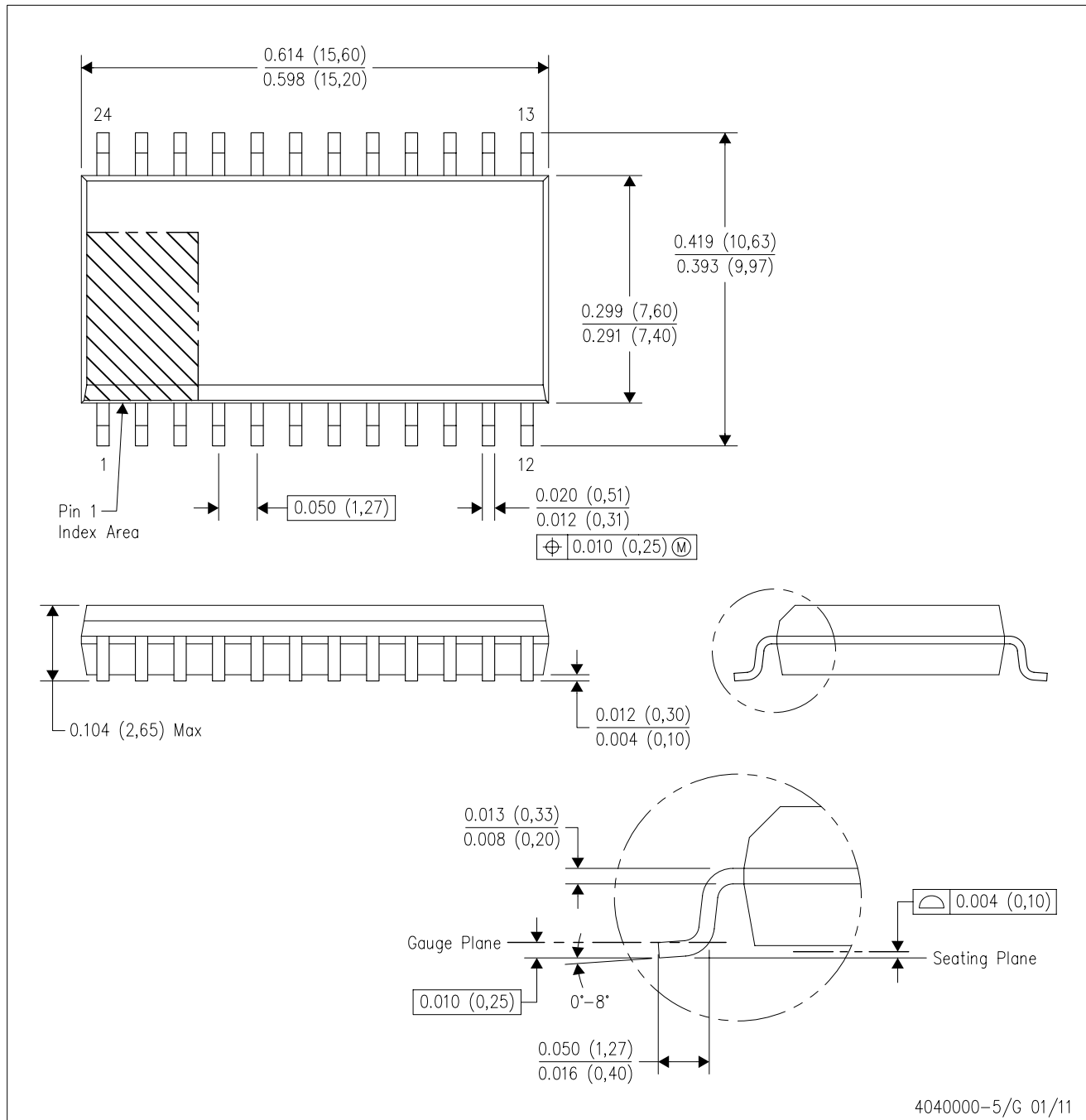
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9548ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
PCA9548ADGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
PCA9548ADWR	SOIC	DW	24	2000	367.0	367.0	45.0
PCA9548APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCA9548ARGER	VQFN	RGE	24	3000	367.0	367.0	35.0

DW (R-PDSO-G24)

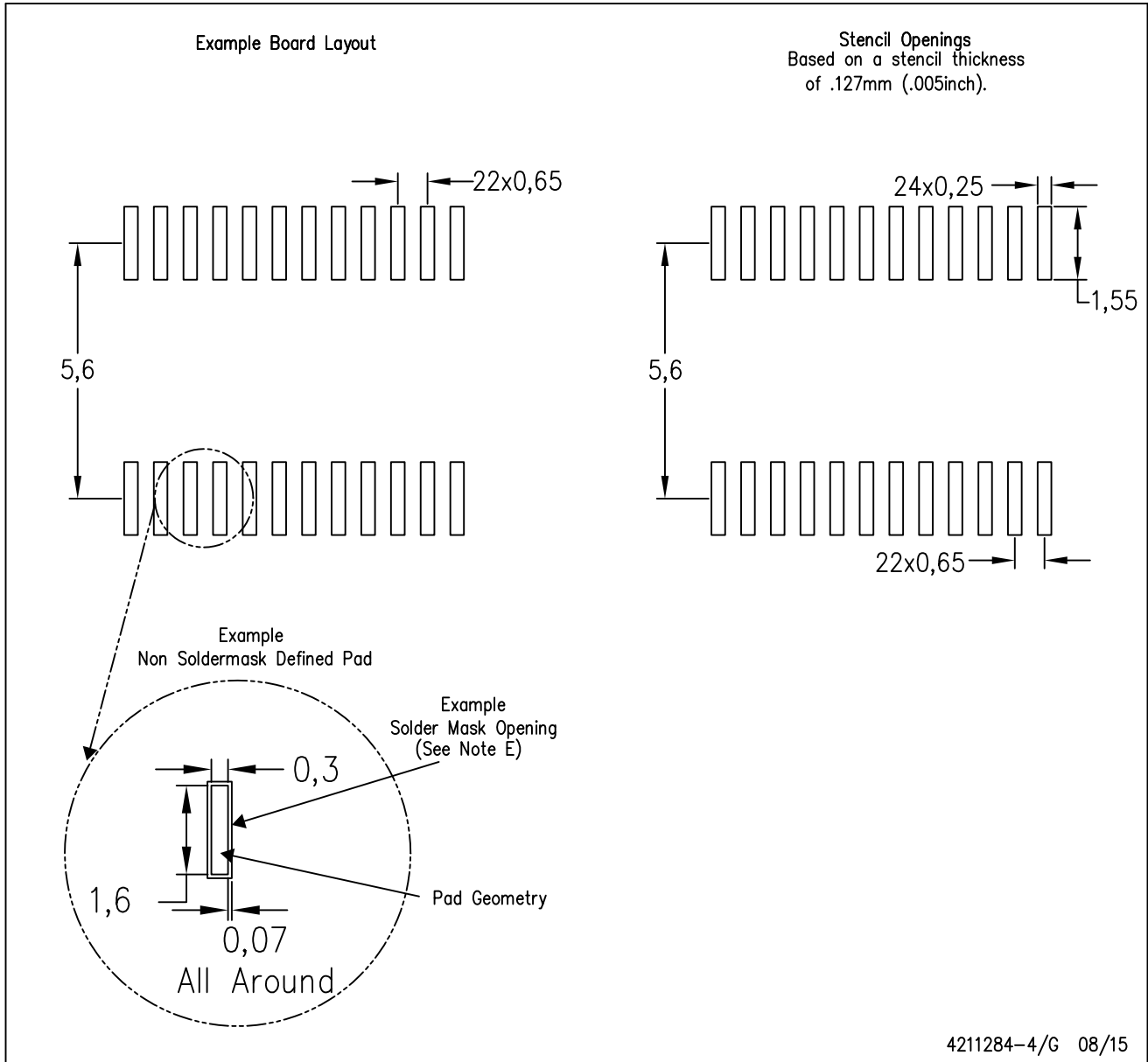
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4211284-4/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



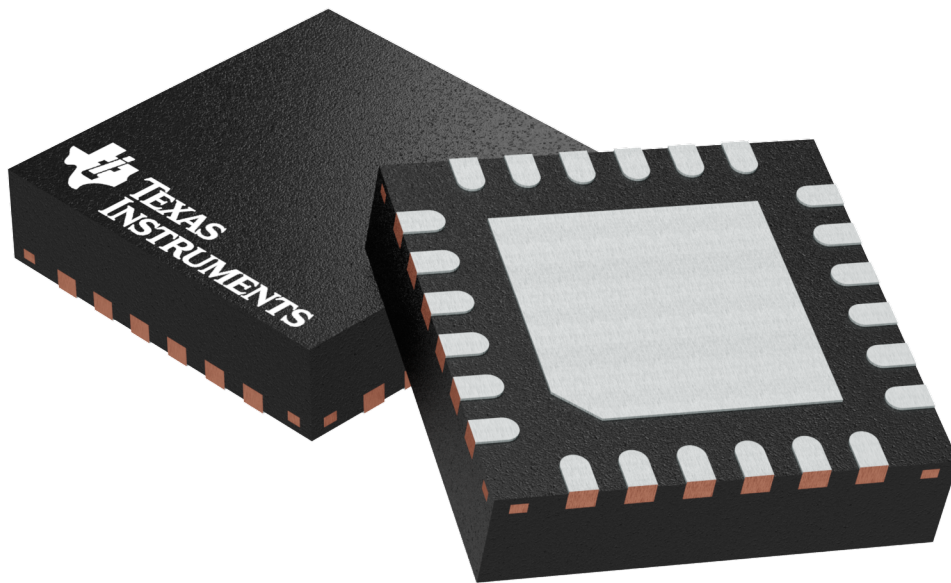
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

RGE 24

GENERIC PACKAGE VIEW

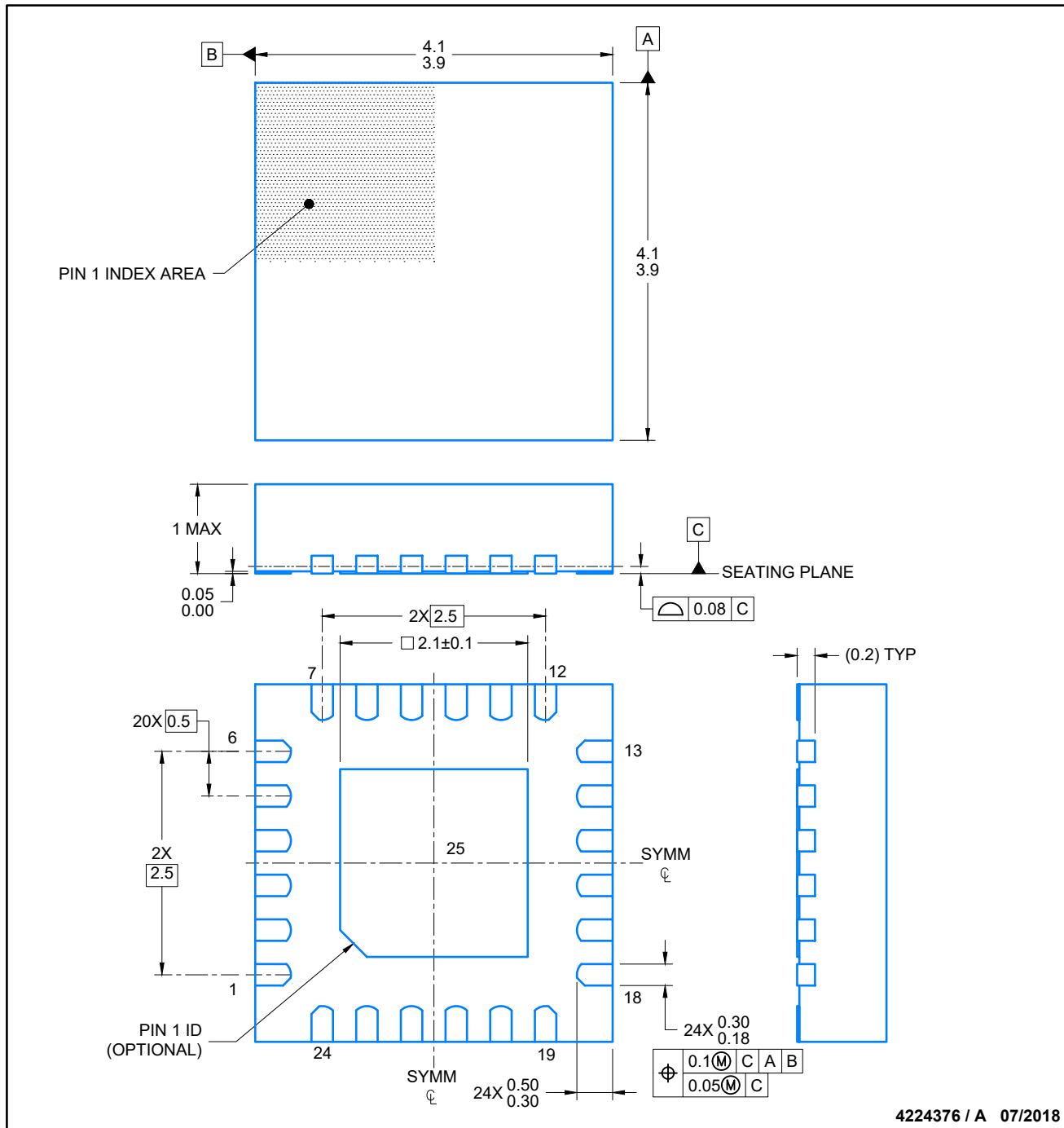
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

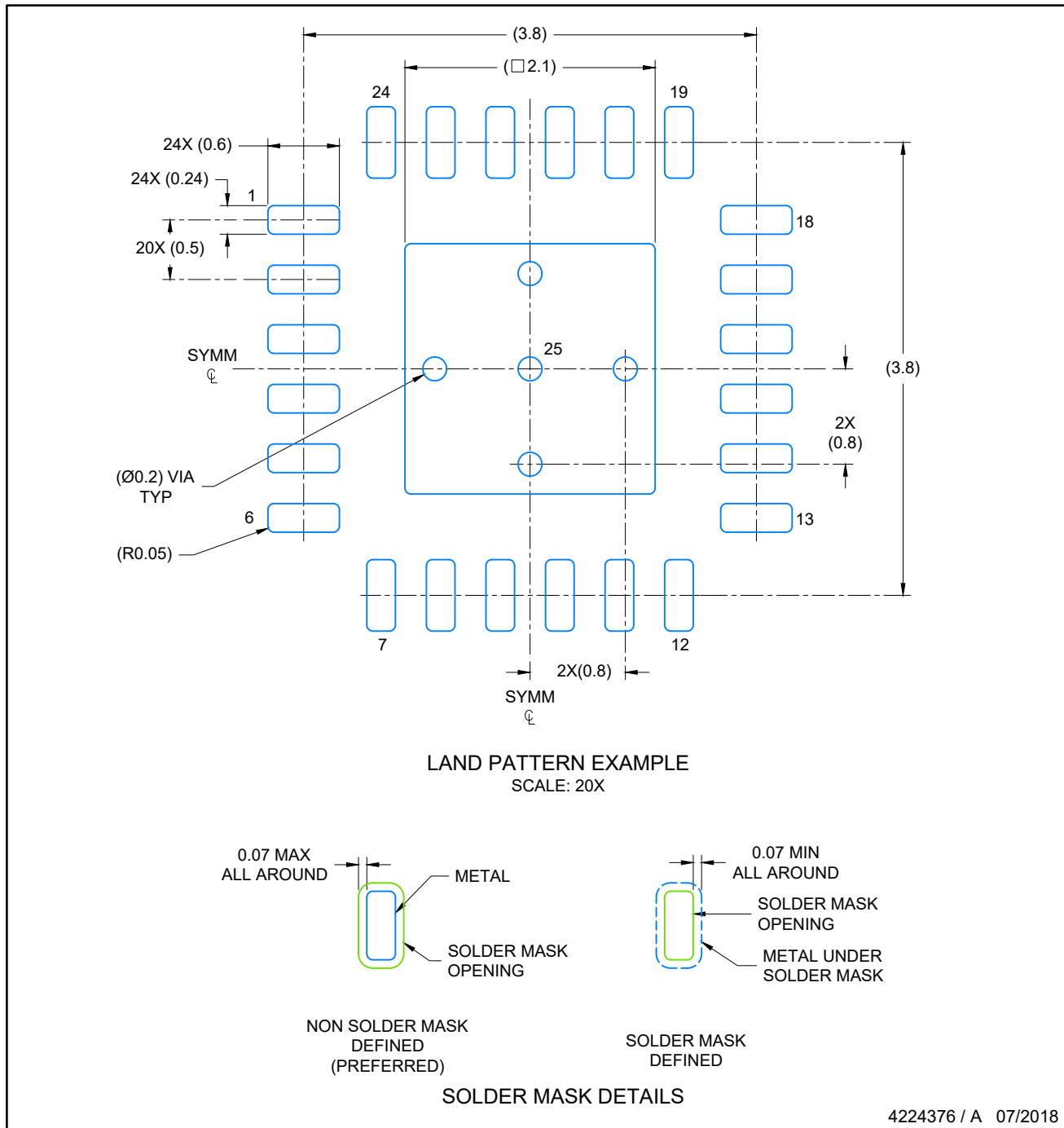
4204104/H



4224376 / A 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

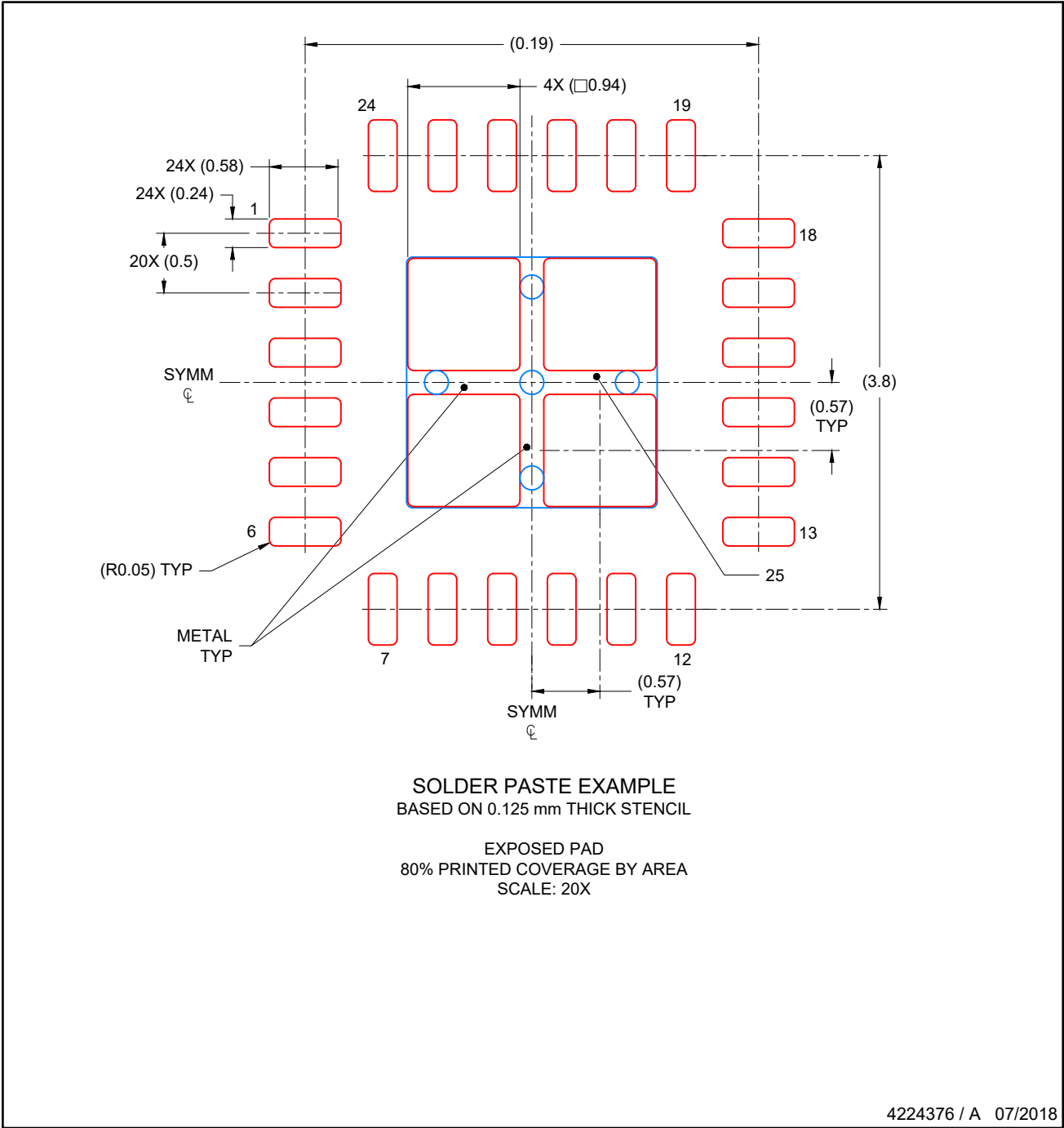
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGE0024C

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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