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AK4321

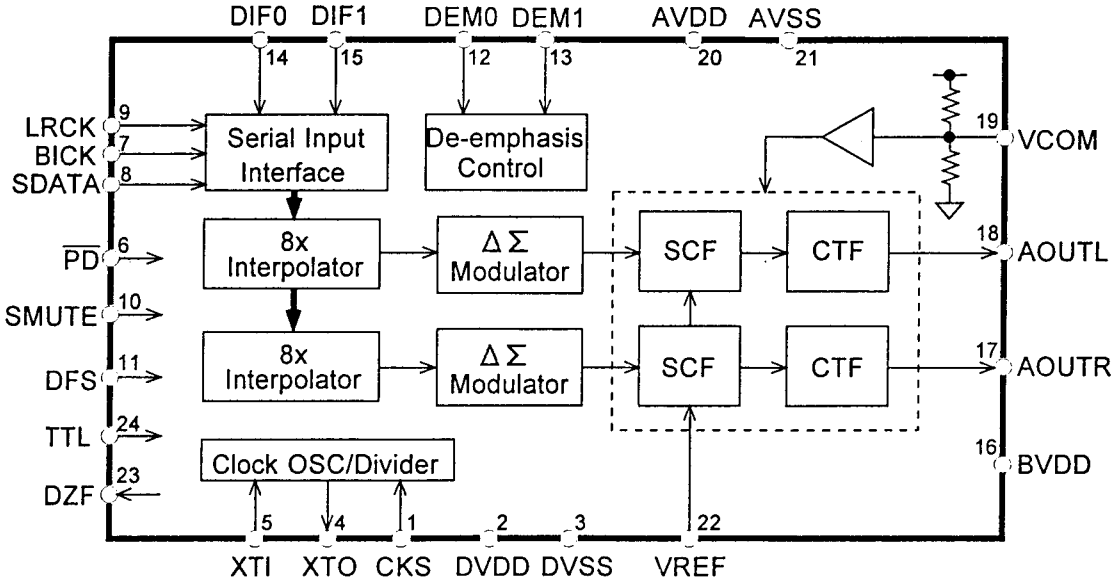
96kHz Sampling 20Bit Δ Σ DAC

General Description

The AK4321 is a high performance 1bit stereo DAC for the 96kHz sampling mode of DAT,DVD including a 20bit digital filter. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4321, the analog outputs are filtered in the analog domain by a combination of switched-capacitor filter(SCF) with high tolerance to clock jitter and continuous-time filter(CTF). Therefore, no external filters are generally required. The AK4321 can operate at the power supply from 2.7V to 5.5V and the digital I/F can also correspond to both TTL and CMOS levels.

Features

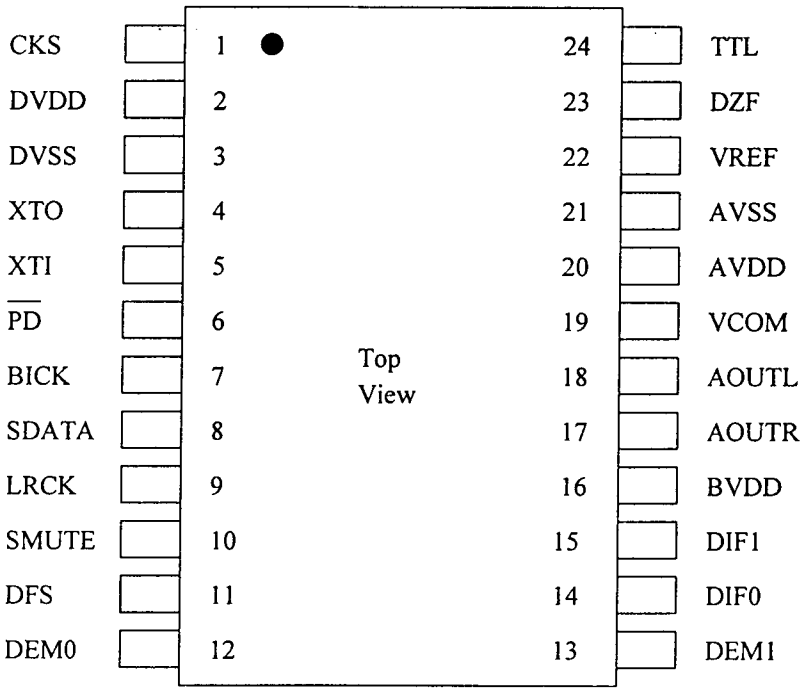
- ☐ High Performance Stereo 1bit DAC
- ☐ Sampling Rate up to 96kHz
- ☐ On chip Perfect Filtering
  - 20Bit 8 times FIR Interpolator
  - 2nd order SCF
  - 2nd order CTF
  - Total Response: ± 0.5dB at 40kHz
- ☐ On chip Buffer with Single End Output
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ Soft Mute
- ☐ High Tolerance to Clock Jitter
- ☐ THD+N: -90dB
- ☐ Dynamic Range, S/N: 100dB
- ☐ Power Supply: Normal Speed(2.7V ~ 5.5V)
  Double Speed(3.0V ~ 5.5V)
- ☐ Small Package: 24pin VSOP



■ Ordering Guide

AK4321-VF	-40 ~ +85 ℃	24pin VSOP(0.65mm pitch)
AKD4321	Evaluation Board	

■ Pin Layout



■ Pin compatibility with AK4320

The following pin functions are changed from AK4320.

Pin No.	AK4320	AK4321
11	HOLD	DFS
16	VCNT	BVDD
24	ZMUTE	TTL

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	CKS	I	Master Clock Select Pin (Pull-down pin) Normal Spped "L": XTI=256fs, "H": XTI=384fs Double Speed "L": XTI=128fs, "H": XTI=192fs
2	DVDD	-	Digital Power Supply Pin
3	DVSS	-	Digital Ground Pin
4	XTO	O	Crystal Oscillator Output Pin When an external clock is input, this pin should be left floating.
5	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external CMOS clock can be input on XTI.
6	PD	I	Power-Down Pin When at "L", the AK4321 is in power-down mode and is held in reset. The AK4321 should always be reset upon power-up.
7	BICK	I	Serial Data Clock Pin 64fs clock is recommended to be input on this pin.
8	SDATA	I	Serial Data Input Pin 2's complement MSB-first data is input on this pin.
9	LRCK	I	L/R Clock Pin
10	SMUTE	I	Soft Mute Pin (Pull-down pin) When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
11	DFS	I	Double speed sampling mode Pin (Pull-down pin) "L": Normal Speed, "H": Double Speed
12 13	DEM0 DEM1	I	De-emphasis Mode Pins This function corresponds to 3 types of sampling rate.
14 15	DIF0 DIF1	I I	Digital Input Format Pins (Pull-down pins) These two pins select one of four formats for the incoming data. When "H", these pins should be connected to DVDD.
16	BVDD	-	Substrate Pin
17	AOUTR	O	Rch Analog Output Pin
18	AOUTL	O	Lch Analog Output Pin
19	VCOM	O	Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor parallel with a 47uF electrolytic cap.
20	AVDD	-	Analog Supply
21	AVSS	-	Analog Ground Pin
22	VREF	I	Voltage Reference Input Pin The differential Voltage between this pin and AVSS sets the analog output range. Normally connected to AVSS with a 0.1uF ceramic capacitor.
23	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes to "H".
24	TTL	I	I/F Level Select Pin (Pull-down pin) "L": CMOS level (DVDD=2.7V ~ 5.5V) "H": TTL level (DVDD=4.5V ~ 5.5V)

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	AVDD	-0.3	6.0	V
Digital	DVDD	-0.3	6.0	V
Substrate	BVDD	-0.3	6.0	V
DVDD-BVDD	VDB	-	0.3	V
Input Current, Any Pin Except Supplies	IIN	-	± 10	mA
Input Voltage	VIND	-0.3	BVDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	℃
Storage Temperature	Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS(fs=44.1kHz)

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies: Analog	(Note 2)	AVDD	2.7	5.0	5.5	V
Digital		DVDD	2.7	5.0	BVDD	V
Substrate		BVDD	2.7	5.0	5.5	V
Voltage Reference	(Note 3)	VREF	2.5	-	AVDD	V

Notes:2. AVDD and BVDD are connected together on the chip through a few Ω resistance.
AVDD and BVDD should be supplied from the same power supply.
AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.
3. Analog output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)=2.8Vpp*VREF/5。

RECOMMENDED OPERATING CONDITIONS(fs=96kHz)

(AVSS,DVSS=0V; Note 4)

Parameter		Symbol	min	typ	max	Units
Power Supplies: Analog	(Note 4)	AVDD	3.0	5.0	5.5	V
Digital		DVDD	3.0	5.0	BVDD	V
Substrate		BVDD	3.0	5.0	5.5	V
Voltage Reference	(Note 5)	VREF	2.5	-	AVDD	V

Notes:4. AVDD and BVDD are connected together on the chip through a few Ω resistance.
AVDD and BVDD should be supplied from the same power supply.
AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.
5. Analog output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)=2.8Vpp*VREF/5。

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS (fs=44.1kHz)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=5.0V; VREF=AVDD; fs=44.1kHz; BICK=64fs;
Signal Frequency=1kHz; 20bit Input Data; Measurement Bandwidth=10Hz ~ 20kHz; RL ≧ 5k Ω ;
unless otherwise specified)

Parameter	min	typ	max	Units
Resolution			20	Bits
Dynamic Characteristics (Note 6)				
THD+N (0dB Output)		-90	-84	dB
(Note 7)		-90	-84	dB
Dynamic Range (-60dB Output, A weight)	96	100		dB
(Note 7)	92	96		dB
S/N (A weight)	96	100		dB
(Note 7)	92	96		dB
Interchannel Isolation(1kHz)	100	110		dB
DC Accuracy				
Interchannel Gain Mismatch		0.15	0.3	dB
Gain Drift (Note 8)		20	-	ppm/ ℃
DC Accuracy				
Output Voltage (Note 9)	2.66	2.8	2.94	Vpp
(Note 7)	1.60	1.68	1.76	Vpp
Load Resistance	5			k Ω
Power Supplies				
Power Supply Current (Note 10)				
Normal Operation ($\overline{PD}$="H")				
AVDD+BVDD		23	35	mA
DVDD		6	9	mA
Power-Down-Mode ($\overline{PD}$="L")				
AVDD+BVDD+DVDD (Note 11)		10	50	uA
Power Dissipation (AVDD+BVDD+DVDD)				
Normal Operation		145	220	mW
Power-Down-Mode (Note 11)		50	250	uW
Power Supply Rejection (Note 12)		50		dB

Notes: 6. Measured by AD725C(SHIBASOKU). Averaging mode.

7. AVDD,DVDD,BVDD=3.0V.
8. The voltage on VREF pin is held +5V externally.
9. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF pin.
   AOUT(typ.@0dB)=2.8Vpp*VREF/5.
10. The typical supply current of DVDD drops to 3mA at 3.0V supply voltage.
    The AVDD+BVDD supply current does not change.
11. Power Dissipation in the power-down mode is applied with no external clocks
    (XTI,BICK,LRCK held "H" or "L").
12. PSR is applied to AVDD,DVDD with 1kHz, 300mVpp. VREF pin is held +5V.

ANALOG CHARACTERISTICS (fs=96kHz)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=5.0V; VREF=AVDD; fs=96kHz; BICK=64fs;
Signal Frequency=1kHz; 20bit Input Data; Measurement Bandwidth=10Hz ~ 40kHz; $R_L \geqq 5k\ \Omega$;
unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				20	Bits
Dynamic Characteristics (Note 13)					
THD+N (0dB Output)			-88	-82	dB
	(Note 14)		-88	-82	dB
Dynamic Range (-60dB Output)		90	93		dB
	(Note 14)	86	90		dB
S/N		90	93		dB
	(Note 14)	86	90		dB
Interchannel Isolation(1kHz)		100	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.15	0.3	dB
Gain Drift	(Note 15)		20	-	ppm/ ℃
DC Accuracy					
Output Voltage	(Note 16)	2.66	2.8	2.94	Vpp
	(Note 14)	1.76	1.85	1.94	Vpp
Load Resistance		5			k Ω
Power Supplies					
Power Supply Current	(Note 17)				
Normal Operation ($\overline{PD}$="H")					
AVDD+BVDD			23	35	mA
DVDD			7	11	mA
Power-Down-Mode ($\overline{PD}$="L")					
AVDD+BVDD+DVDD	(Note 18)		10	50	uA
Power Dissipation (AVDD+BVDD+DVDD)					
Normal Operation			150	230	mW
Power-Down-Mode	(Note 18)		50	250	uW
Power Supply Rejection	(Note 19)		50		dB

Notes:13. Measured by AD725C(SHIBASOKU). Averaging mode.

14. AVDD,DVDD,BVDD=3.3V.
15. The voltage on VREF pin is held +5V externally.
16. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF pin.
AOUT(typ.@0dB)=2.8Vpp*VREF/5.
17. The typical supply current of DVDD drops to 5mA at 3.3V supply voltage.
The AVDD+BVDD supply current does not change.
18. Power Dissipation in the power-down mode is applied with no external clocks
(XTI,BICK,LRCK held "H" or "L").
19. PSR is applied to AVDD,DVDD with 1kHz, 300mVpp. VREF pin is held +5V.

FILTER CHARACTERISTICS(fs=44.1kHz)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=2.7V ～ 5.5V; fs=44.1kHz; DFS="0"; DEM0="1",DEM1="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ± 0.06dB (Note 20)	PB	0		20.0	kHz
-6.0dB		-	22.05	-	kHz
Stopband (Note 20)	SB	24.1			kHz
Passband Ripple	PR			± 0.06	dB
Stopband Attenuation	SA	43			dB
Group Delay (Note 21)	GD	-	14.7	-	1/fs
Digital Filter + Analog Filter					
Frequency Response 0 ～ 20.0kHz		-	± 0.2	-	dB

Note: 20. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@ ± 0.06dB), SB=0.546*fs.

21. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20bit data of both channels to input register to the output of analog signal.

FILTER CHARACTERISTICS(fs=96kHz)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=3.0V ～ 5.5V; fs=44.1kHz; DFS="1"; DEM0="1",DEM1="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ± 0.06dB (Note 22)	PB	0		43.5	kHz
-6.0dB		-	48.0	-	kHz
Stopband (Note 22)	SB	52.5			kHz
Passband Ripple	PR			± 0.06	dB
Stopband Attenuation	SA	43			dB
Group Delay (Note 23)	GD	-	14.7	-	1/fs
Digital Filter + Analog Filter					
Frequency Response 0 ～ 40.0kHz		-	± 0.5	-	dB

Note: 22. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@ ± 0.06dB), SB=0.546*fs.

23. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS (TTL level input)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=4.5V ~ 5.5V; TTL="H")

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(TTL pin)	VIH1	90%DVDD	-	-	V
	(XTI pin, Note 24)	VIH2	70%DVDD	-	-	V
	(All pins except XTI,TTL pins)	VIH3	2.2	-	-	V
Low-Level Input Voltage	(TTL pin)	VIL1	-	-	10%DVDD	V
	(XTI pin, Note 24)	VIL2	-	-	30%DVDD	V
	(All pins except XTI,TTL pins)	VIL3	-	-	0.8	V
Input Voltage at AC coupilng	(XTI pin)	VAC	1	-	BVDD	Vpp
High-Level Output Voltage	Iout=-100uA	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage	Iout=100uA	VOL	-	-	0.5	V
Input Leakage Current	(Note 25)	Iin	-	-	± 10	uA

Note: 24. The master clock should be input by AC coupling in case of TTL level.

25. DIF0,DIF1,TTL,SMUTE,DFS,CKS pins have internal pull-down devices, nominally 90k Ω .

DIGITAL CHARACTERISTICS (CMOS level input)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=2.7V ~ 5.5V; TTL="L")

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(TTL pin)	VIH1	90%DVDD	-	-	V
	(XTI pin)	VIH2	70%DVDD	-	-	V
	(All pins except XTI,TTL pins)	VIH3	70%DVDD	-	-	V
Low-Level Input Voltage	(TTL pin)	VIL1	-	-	10%DVDD	V
	(XTI pin)	VIL2	-	-	30%DVDD	V
	(All pins except XTI,TTL pins)	VIL3	-	-	30%DVDD	V
Input Voltage at AC coupilng	(XTI pin)	VAC	1	-	BVDD	Vpp
High-Level Output Voltage	Iout=-100uA	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage	Iout=100uA	VOL	-	-	0.5	V
Input Leakage Current	(Note 26)	Iin	-	-	± 10	uA

Note: 26. DIF0,DIF1,TTL,SMUTE,DFS,CKS pins have internal pull-down devices, nominally 90k Ω .

SWITCHING CHARACTERISTICS (DVDD=3.0V ~ 5.5V)

(Ta=25 °C ; AVDD,DVDD,BVDD=3.0V ~ 5.5V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Unit
Master Clock Frequency					
Crystal Resonator 256fs:	fCLK	8.192	11.2896	12.288	MHz
384fs:	fCLK	12.288	16.9344	18.432	MHz
External Clock 256fs:	fCLK	5.12	11.2896	12.288	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	7.68	16.9344	18.432	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
LRCK Frequency (Note 27)					
Normal Speed Mode (DFS="L")	fsn	20	44.1	48	kHz
Double Speed Mode (DFS="H")	fsd	64	88.2	96	kHz
Serial Interface Timing (Note 28)					
BICK Period	tBCK	160			ns
BICK Pulse Width Low	tBCKL	70			ns
Pulse Width High	tBCKH	70			ns
BICK rising to LRCK edge (Note 29)	tBLRD	30			ns
LRCK Edge to BICK rising (Note 29)	tLRBD	30			ns
SDATA Hold Time	tSDH	30			ns
SDATA Setup Time	tSDS	50			ns
Reset Timing					
PD Pulse Width (Note 30)	tRST	100			ns

Notes: 27. When the normal speed mode and the double speed mode are switched, the AK4321 should be reset by PD pin.

28. Refer to the operating overview section "Serial Data Interface".

29. SCLK rising edge must not occur at the same time as L/R edge.

30. The AK4321 can be reset by bringing PD "L" to "H" only upon power up.

SWITCHING CHARACTERISTICS (DVDD=2.7V ~ 3.0V)

(Ta=25 ℃ ; AVDD,DVDD,BVDD=2.7V ~ 3.0V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Unit
Master Clock Frequency					
Crystal Resonator 256fs:	fCLK	8.192	11.2896	12.288	MHz
384fs:	fCLK	12.288	16.9344	18.432	MHz
External Clock 256fs:	fCLK	5.12	11.2896	12.288	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	7.68	16.9344	18.432	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
LRCK Frequency (Note 31)					
Normal Speed Mode (DFS="L")	fsn	20	44.1	48	kHz
Serial Interface Timing (Note 32)					
BICK Period	tBCK	312			ns
BICK Pulse Width Low	tBCKL	120			ns
Pulse Width High	tBCKH	120			ns
BICK rising to LRCK edge (Note 33)	tBLRD	50			ns
LRCK Edge to BICK rising (Note 33)	tLRBD	50			ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Reset Timing					
PD Pulse Width (Note 34)	tRST	100			ns

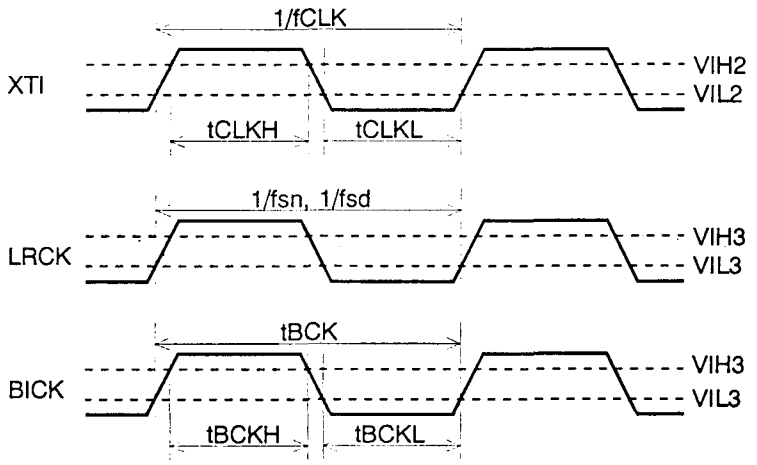
Notes: 31. In this condition, AK4321 corresponds to only the normal speed mode.

32. Refer to the operating overview section "Serial Data Interface".

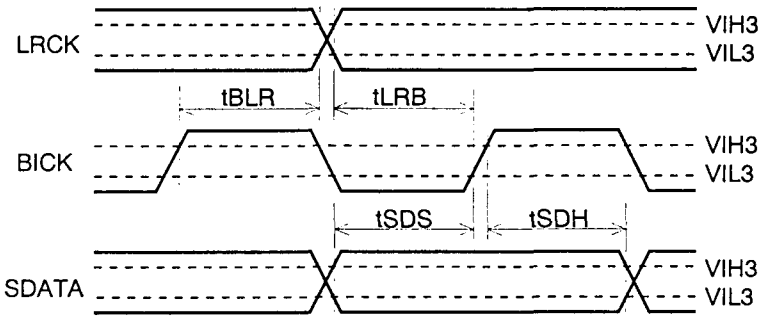
33. SCLK rising edge must not occur at the same time as L/R edge.

34. The AK4321 can be reset by bringing PD "L" to "H" only upon power up.

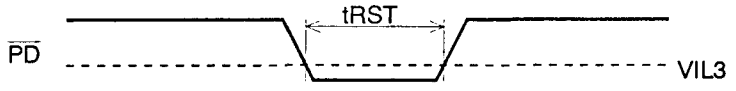
■ Timing Diagram



Clock Timing



Serial Interface Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4321 are XTI, LRCK, BICK. The master clock(XTI) should be synchronized with LRCK but the phase is free of care. The XTI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of XTI is determined by the sampling rate (LRCK), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an XTI frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3) (Figure 1).

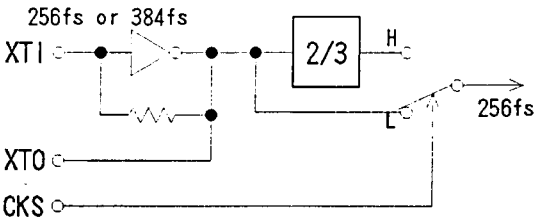


Figure 1. Internal Clock Circuit

The master clock can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. Not only CMOS clock but sine wave signal with 1Vp-p can be input to the XTI pin by AC coupling. Table 1 illustrates corresponding clock frequencies used in each speed.

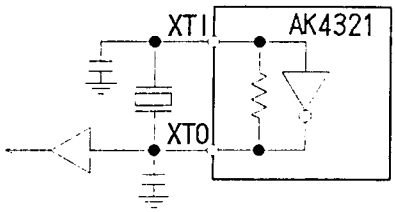


Figure 2. Crystal resonator connection

All external clocks(XTI,BICK,LRCK) should always be present whenever the AK4321 is in normal operation mode(PD="H"). If these clocks are not provided, the AK4321 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4321 should be in the power-down mode(PD="L").

Speed		Normal DFS="L"	Double DFS="H"
LRCK		fs 20k ~ 48kHz	fs 64k ~ 96kHz
BICK		~ 64fs	~ 64fs
XTI	CKS="L"	256fs	128fs
	CKS="H"	384fs	192fs

Table 1. System Clock

■ Serial Data Interface

Data is input to the AK4321 via three serial input pins(SDATA, BICK, LRCK). The AK4321 supports four serial data formats which can be selected via DIF0 and DIF1 pins(Table 2). Format 0 is compatible with existing 16-bit DACs and digital filters. Format 1 is an 20-bit version of format 0. Format 2 is similar to AKM ADCs and many DSP serial ports. Format 3 is compatible with the I ^{2} S serial data protocol. Format 2 and 3 support 20-bit input, 18-bit input followed by two zeros or 16-bit followed by four zeros. In all serial input modes, the serial data is MSB-first and 2's complement format.

DIF1	DIF0	Mode	Fig
0	0	0: LSB Justified,16bit	3
0	1	1: LSB Justified,20bit	3
1	0	2: MSB Justified,16-20bit	4
1	1	3: I ^{2} S Compatible	5

Table 2. Digital Input Formats

*The use of 64fs clock is recommeded as BICK.

*Mode 0 should be used if BICK is 32fs.

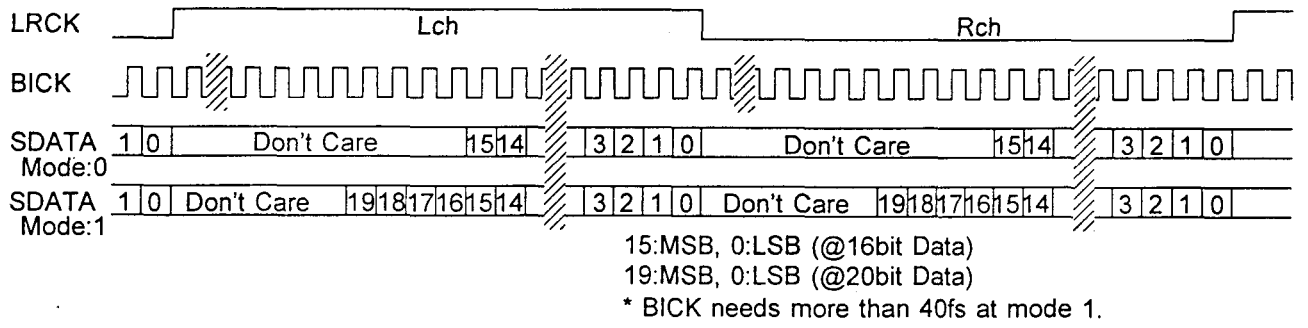


Figure 3. Digital Input Formats 0 & 1

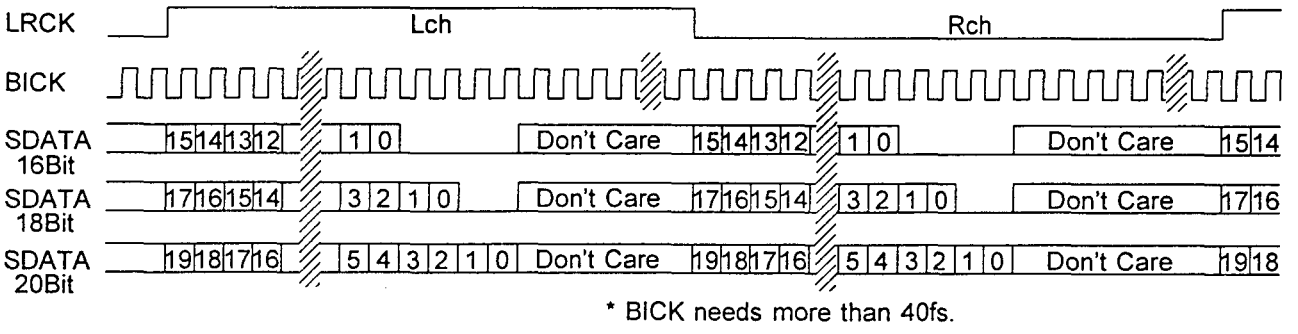


Figure 4. Digital Input Format 2

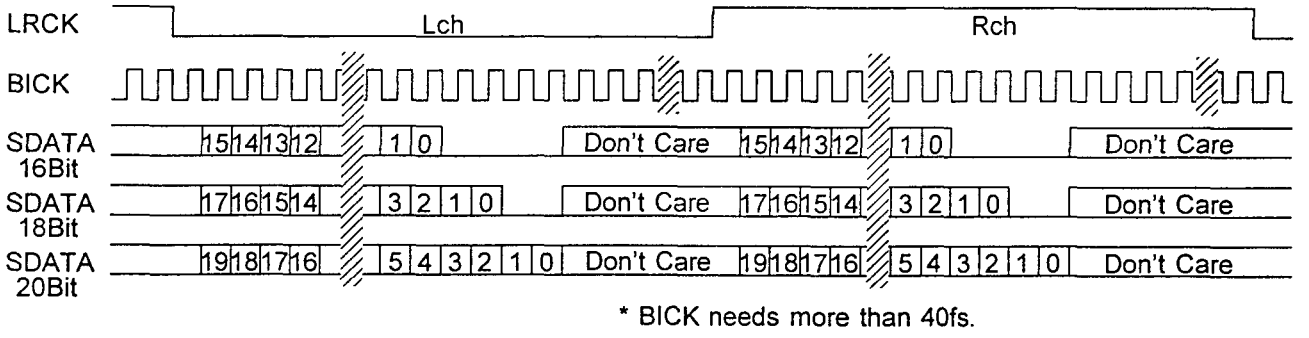


Figure 5. Digital Input Format 3

■ De-emphasis filter

The AK4321 includes the digital de-emphasis filter(tc=50/15us) by IIR filter.This filter corresponds to three sampling frequencies(32kHz,44.1kHz,48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 1. De-emphasis filter control

■ Zero detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes to "L" if input data are not zero after DZF "H".

■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by - ∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

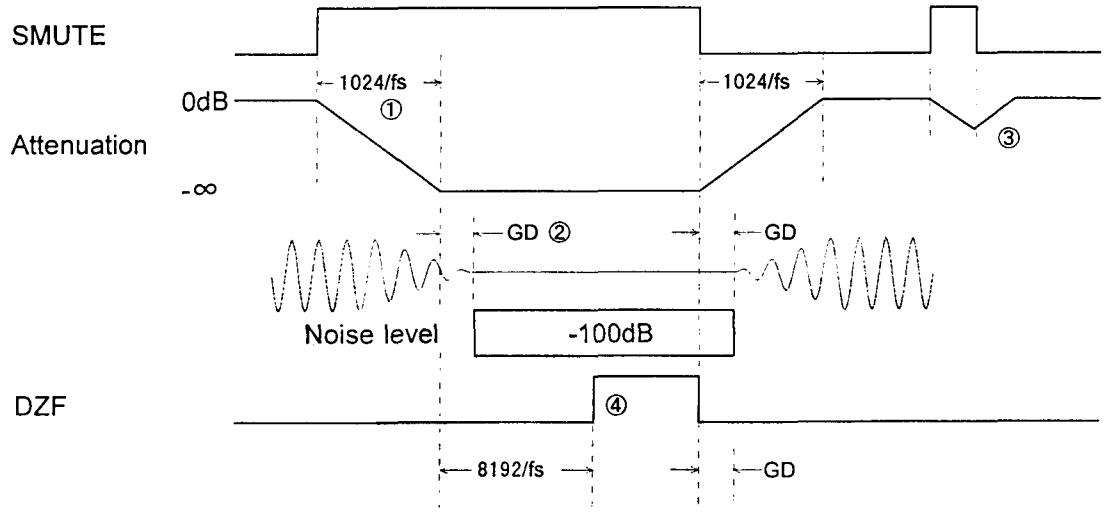


Figure 6. Soft mute and zero detection

Notes:

① The output signal is attenuated by - ∞ during 1024 LRCK cycles(1024/fs).

② Analog output corresponding to digital input have the group delay(GD).

③ If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

④ When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes to "L" if input data are not zero after DZF "H".

■ Power-Down

The AK4321 are placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 7 shows an example of the system timing at the power-down and power-up.

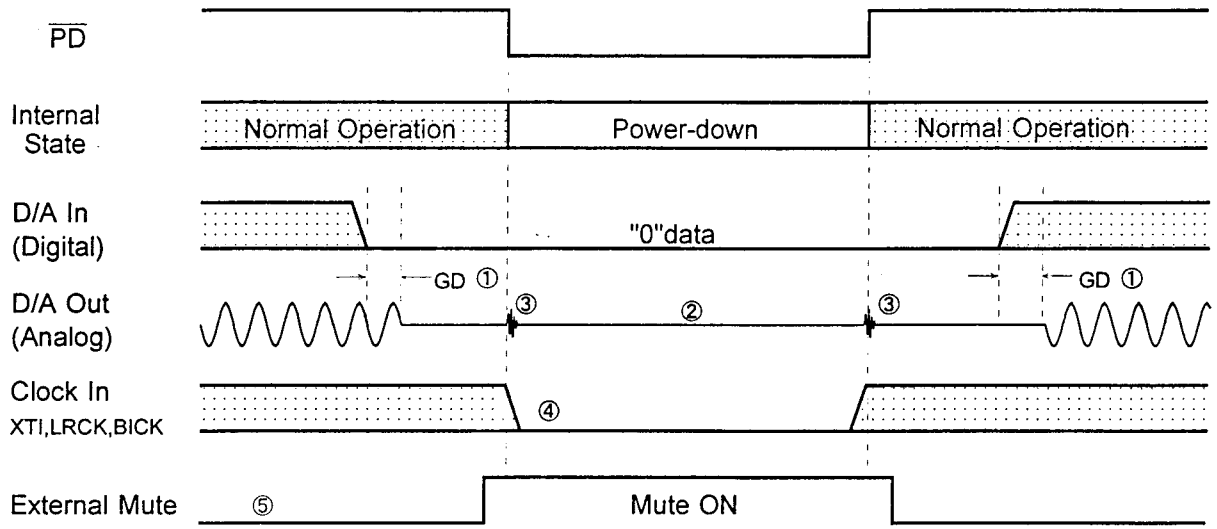


Figure 7. Power-down/up sequence example

Notes:

① Analog output corresponding to digital input have the group delay(GD).

② Analog outputs are floating(Hi-Z) at the power-down mode. The output noise level is about -110dB.

③ Click noise about -50dB occurs at the edges(" ↑ ↓ ") of $\overline{PD}$ signal.
This noise is output even if "0" data is input.

④ When the external clocks(XTI,BICK,LRCK) are stopped, the AK4321 should be in the power-down mode.

⑤ Please mute the analog output externally if the click noise(③) influences system application.
The timing example is shown in this figure.

■ System Reset

The AK4321 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking by LRCK " ↑ " upon exiting reset.

SYSTEM DESIGN

Figure 8 shows the system connection diagram. An evaluation board[AKD4321] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

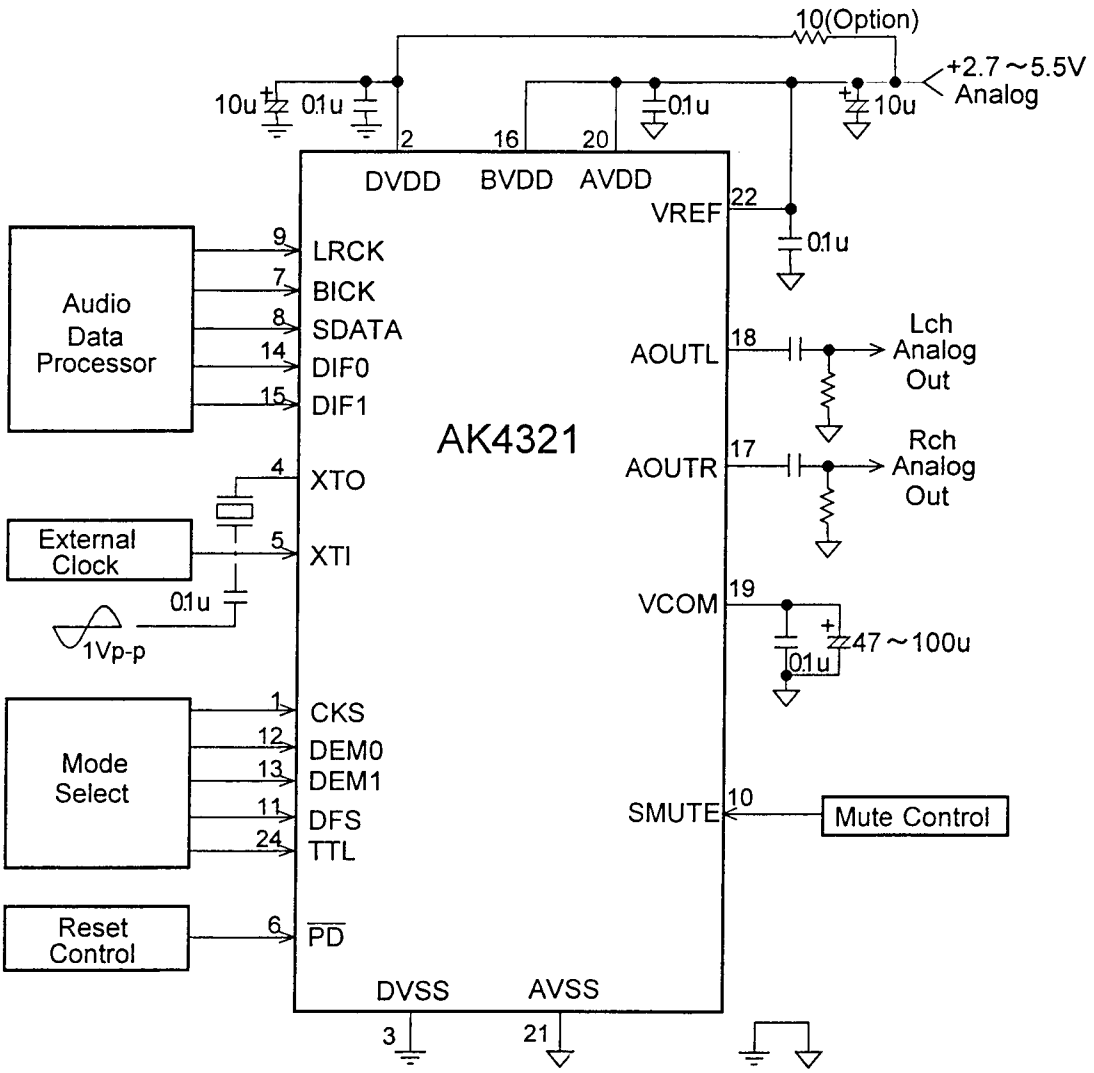


Figure 8. Typical Connection Diagram

Notes:

- LRCK=fs, BICK=64fs or 48fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

■ System design

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, BVDD and DVDD, respectively. AVDD,BVDD is supplied from analog supply in system and DVDD is supplied from AVDD,BVDD via 10 Ω resistor. Alternatively if AVDD,BVDD and DVDD are supplied separately, AVDD,BVDD and DVDD should be powered at the same time or AVDD,BVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage reference

The differential Voltage between VREF and AVSS set the analog output range. VREF pin is normally connected to AVDD with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor around 47uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4321.

3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.8Vpp(1Vrms@AVDD=5V). AC coupling capacitors of larger than 1uF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. However, as the outband noise more than 40kHz is not so small in case of double sampling mode, some application may require external filter. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV. Figure 9 shows the example of external op-amp circuit with 6dB gain. The output signal is inverted by using the circuit in Figure 9.

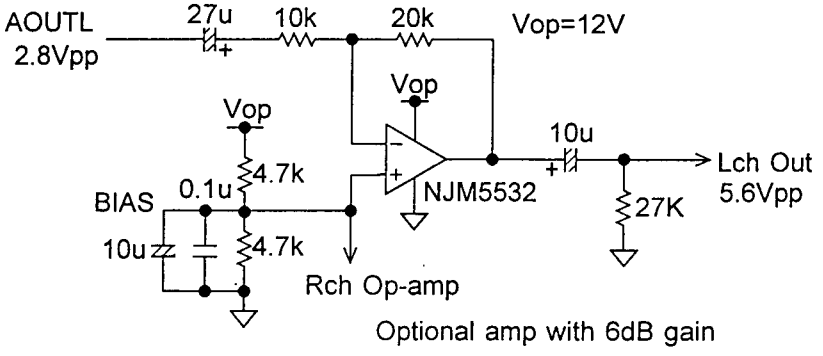
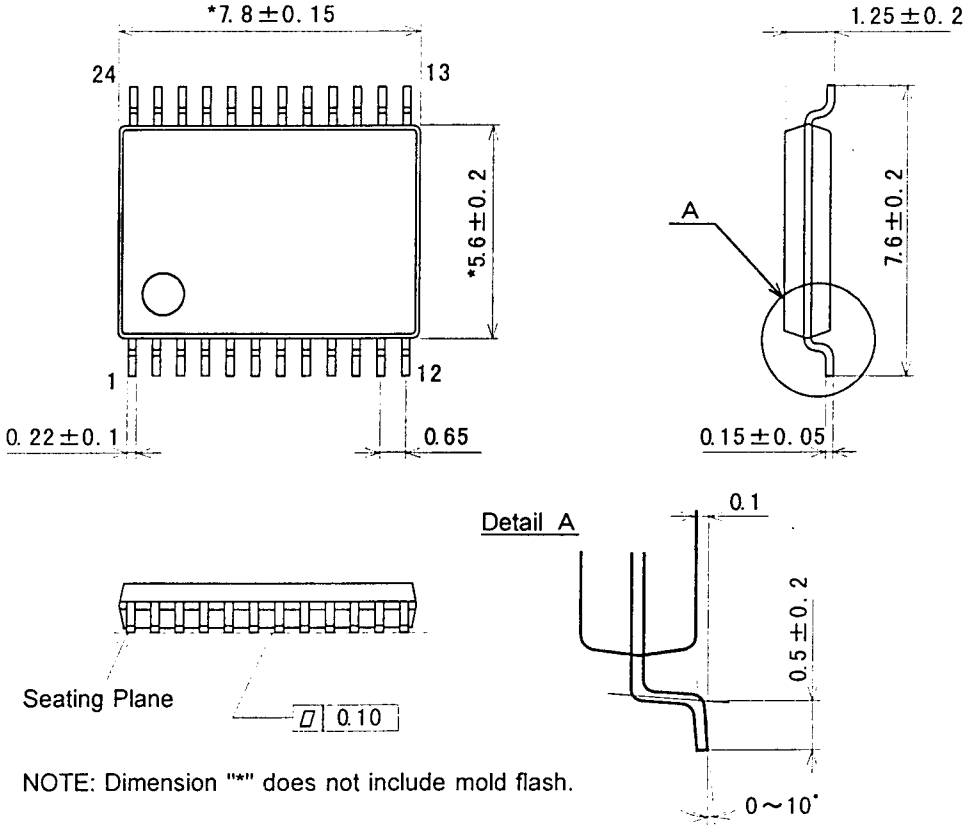


Figure 9. External analog circuit example(gain=6dB)

PACKAGE

● 24pin VSOP (Unit: mm)

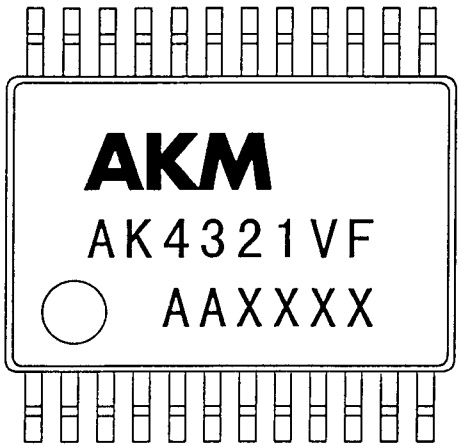


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound : Epoxy
Lead frame material : Cu
Lead frame surface treatment: Solder plate

MARKING



Contents of A A X X X X

A A : Lot#

X X X X : Date Code

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